

Topology and Control for MHz High Efficiency High Density DC-DC Converter

仅限PMIC会员单位内部使用，不得外传

Xinke Wu Ph. D



Applications of High Density High Efficiency Power Converters



Space & Satellite



More/Full Electric Aircraft



Supercomputing/AI



EV/HEV Autopilot

**High Density
High Efficiency**



Radar Power supply



5/6G Base station



Portable Devices

1. Introduction of power supply architecture of internet datacenter and popular high density high efficiency applications.

2. Topology for MHz high efficiency 380V-48V/12V power conversion

2.1 Unregulated DC-DC techniques

2.2 EMI design considerations of planar PCB transformer

2.3 Tight regulated 380V-48V&12V conversion

3. MHz high efficiency 48/12V/XV power converters

3.1 Low power DCX converter for intermedia bus application.

3.2 Tight regulated DC-DC converter for 48V-12V in server

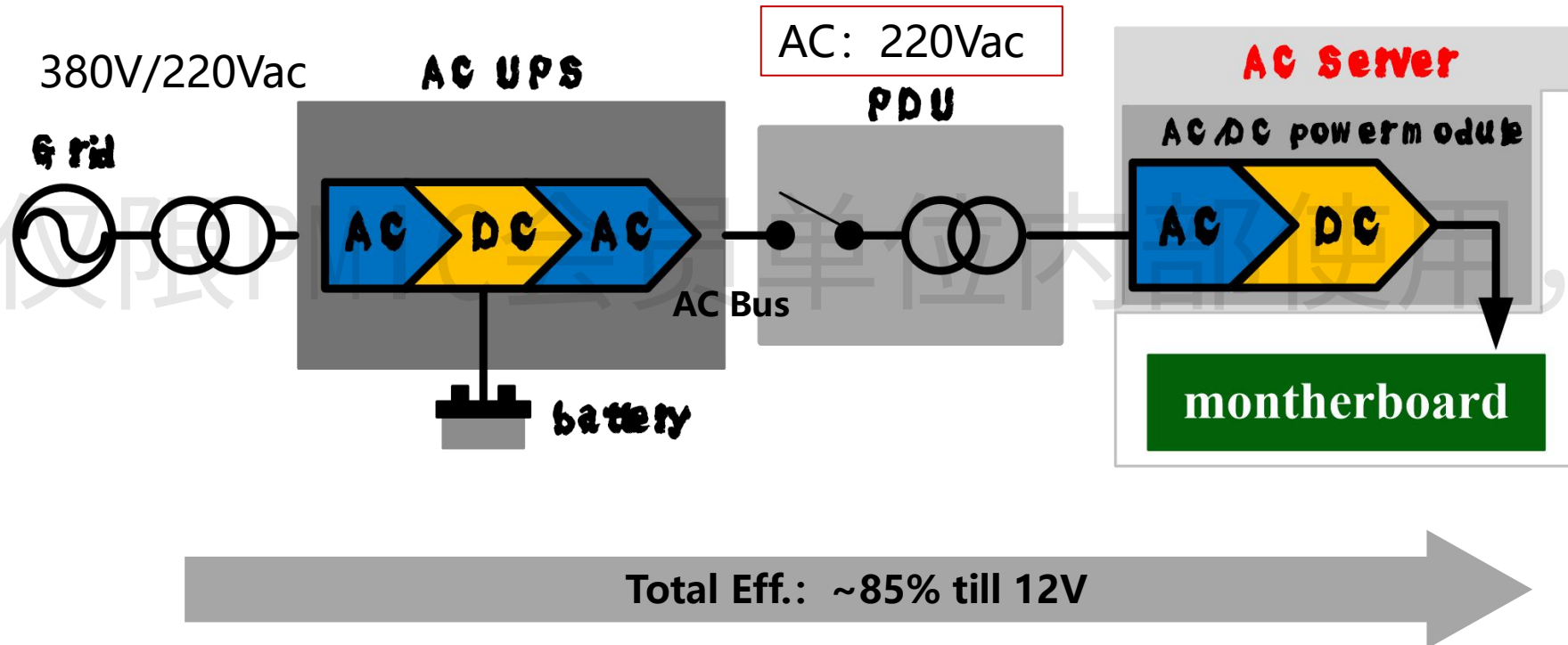
3.3 High Density Transformer Design for 48V MHz DC-DC converter

4. Conclusions



Power Architectures of Internet Data Center (IDC)

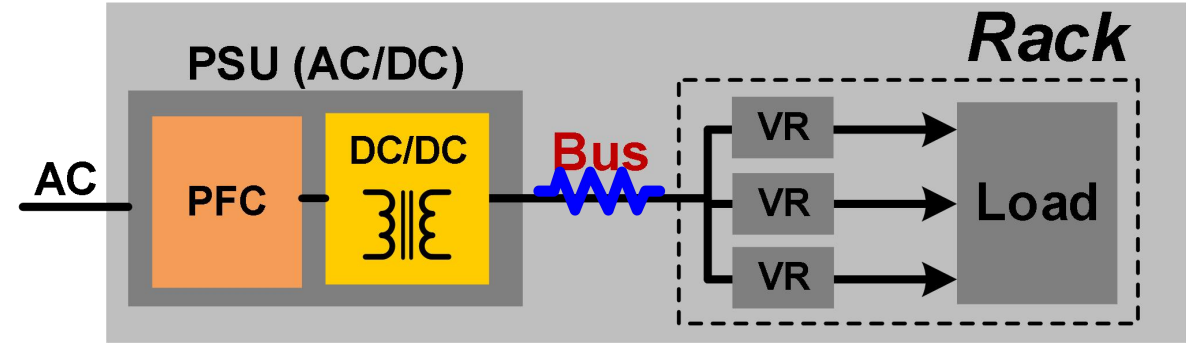
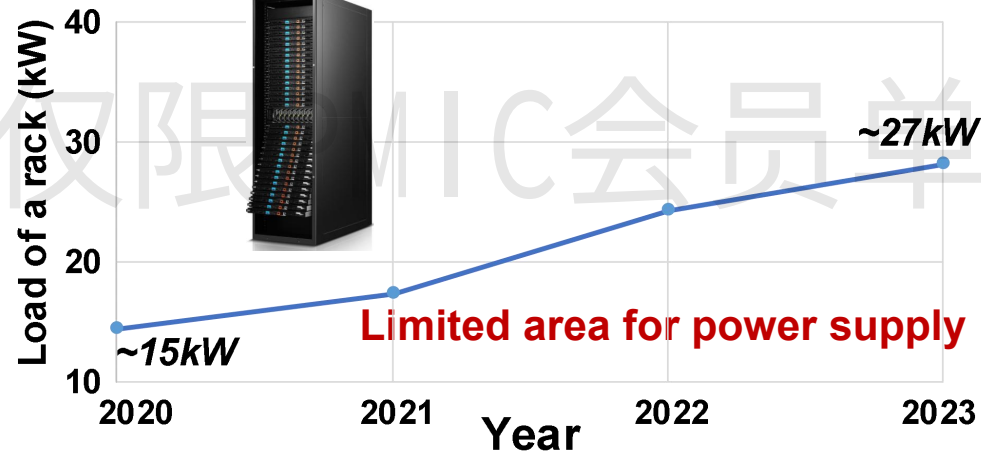
□ Conventional 220V AC structure



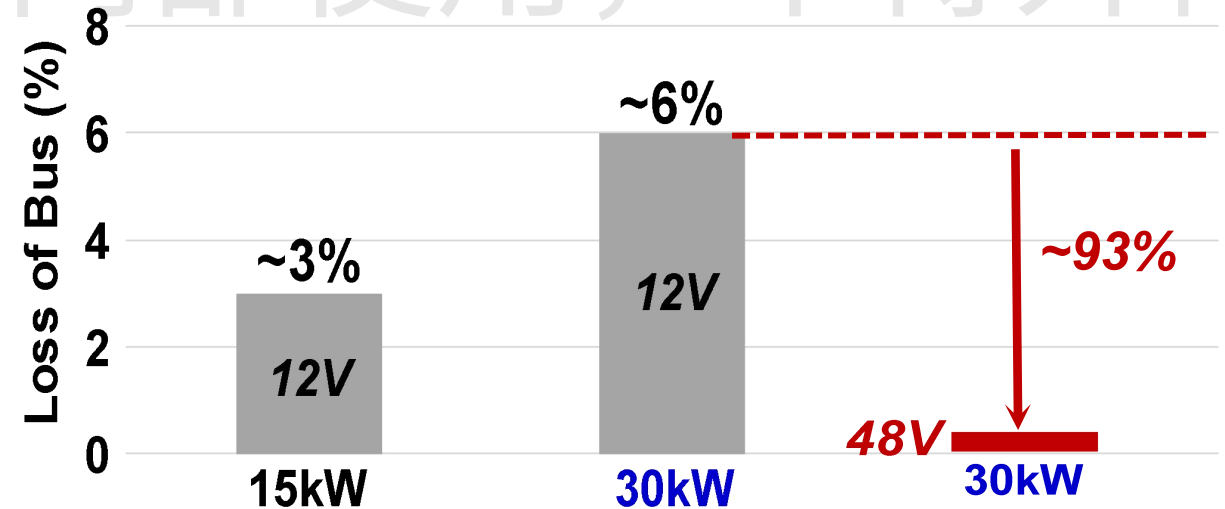
48V DC Bus for IDC

- High power density
- High efficiency

Load increase of racks:



Power architecture of rack

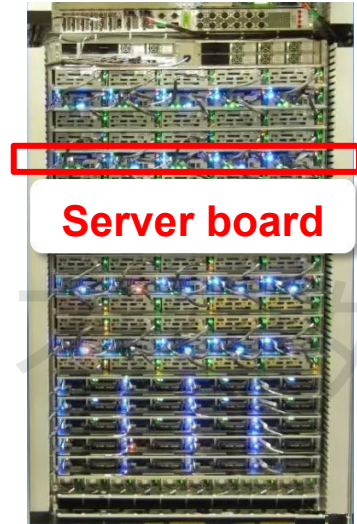
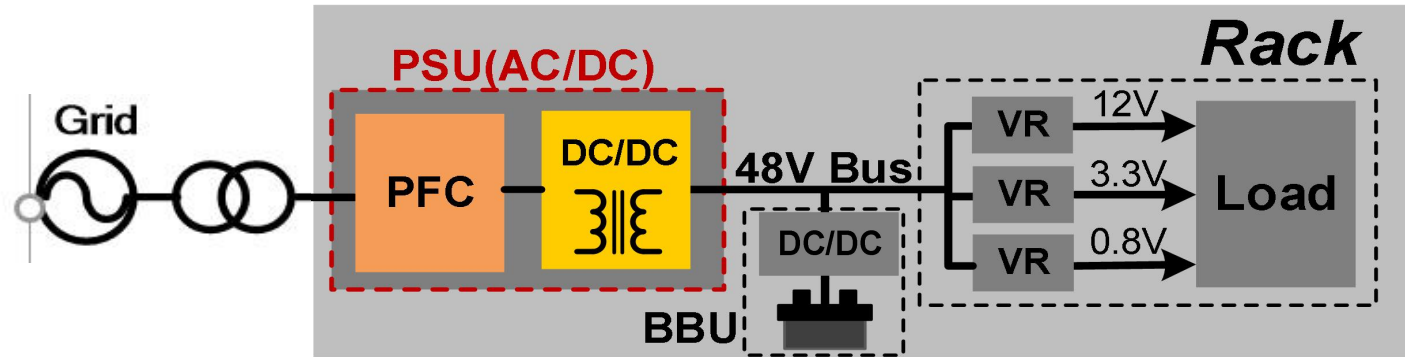


Bus loss at different input voltage

Power Architectures of Internet Data Center

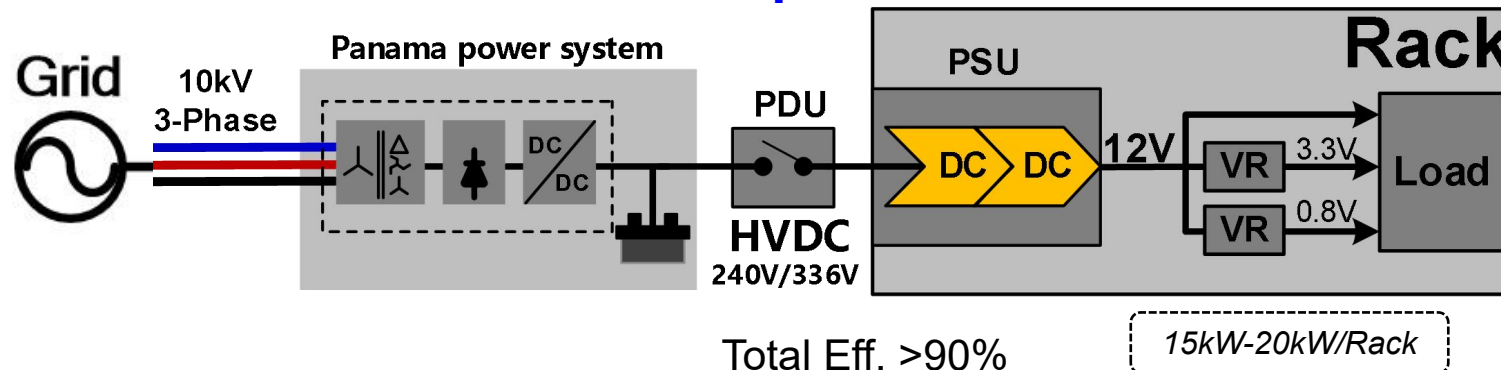
□ HVDC

48V intermedia Bus



Rack
More than 15kW

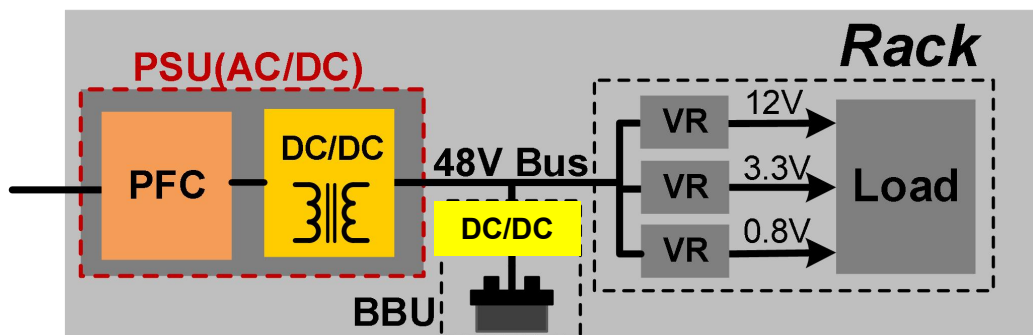
10kV Panama power architecture



Increasing Efficiency Requirement of AC/DC for 48V Bus

Power Management Innovation Consortium

Rack power architecture:



OCP:



OPEN
Compute Project®

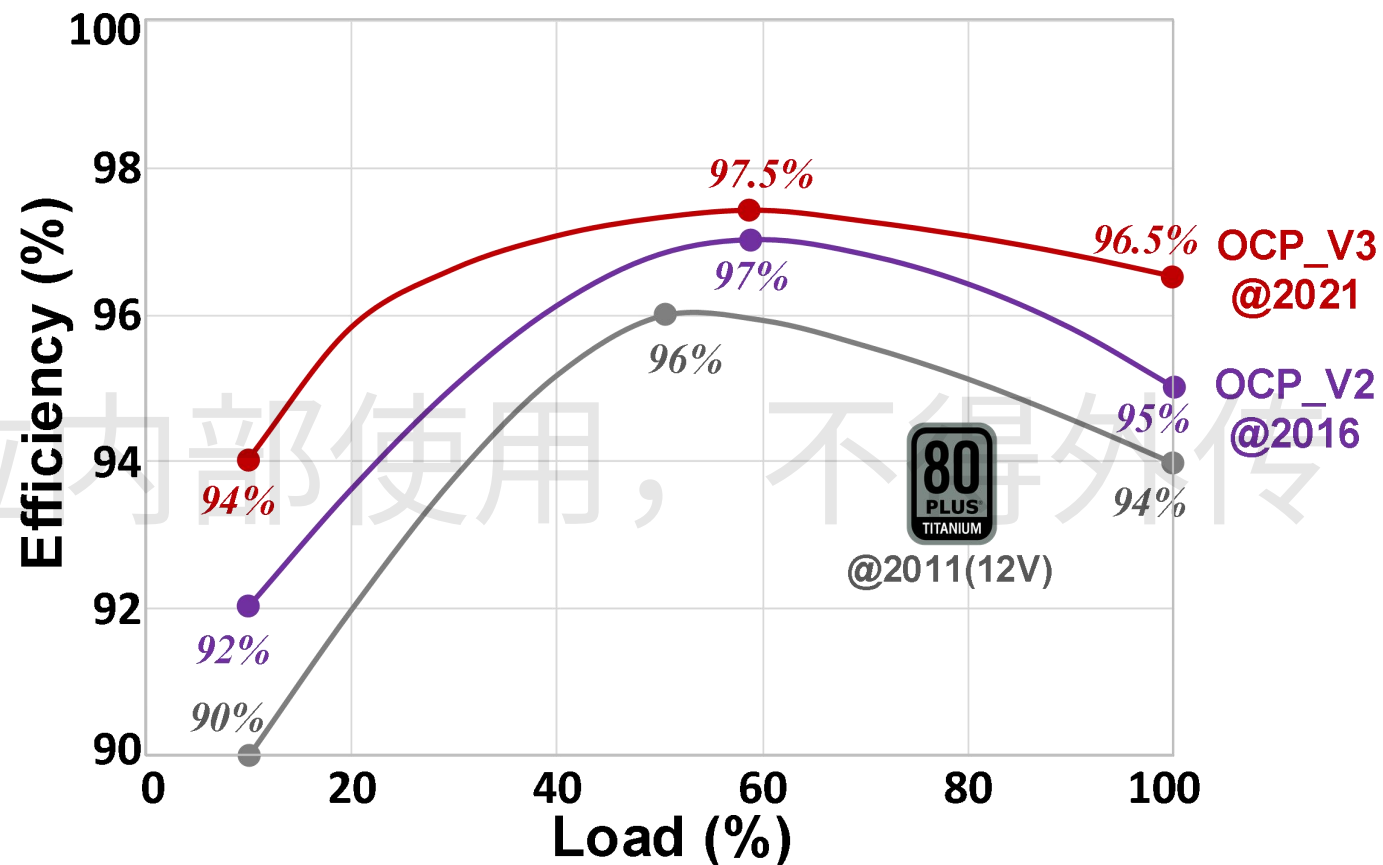
Sub-project:



Members:



Rack & Power



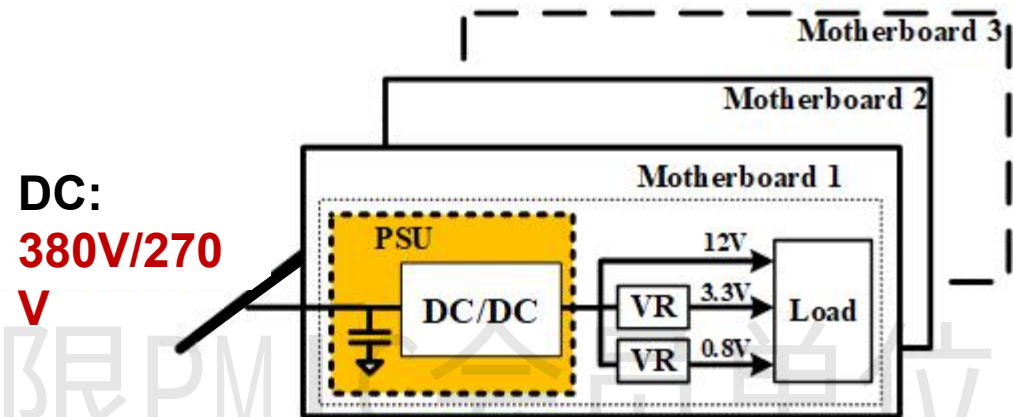
Higher efficiency of AC/DC is required



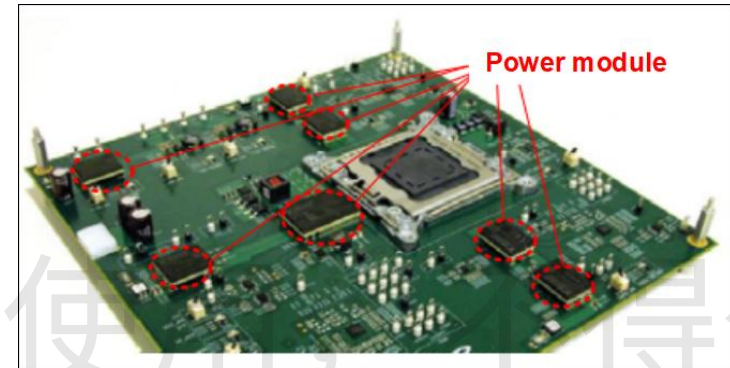
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ZJU-Hangzhou Global Scientific and Technological Innovation Center

- [1] Titanium, 80PLUS, 2011;
- [2] Open rack V2, 2016;
- [3] Open rack V3.0, 2021;

HDVC Feeding Server Board Requires High Density Embedded DC/DC Module



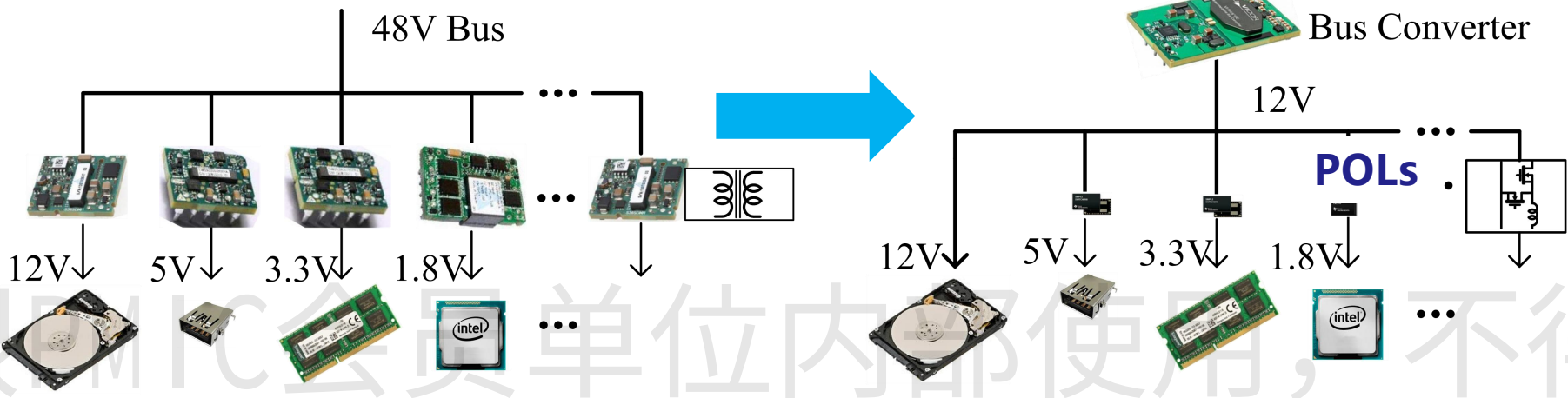
Embedded high voltage bus dc/dc module



Motherboard
380V-12V DC/DC

- ❑ Ultra high density
- ❑ Ultra high efficiency

48V Power Delivery Solution Comparison

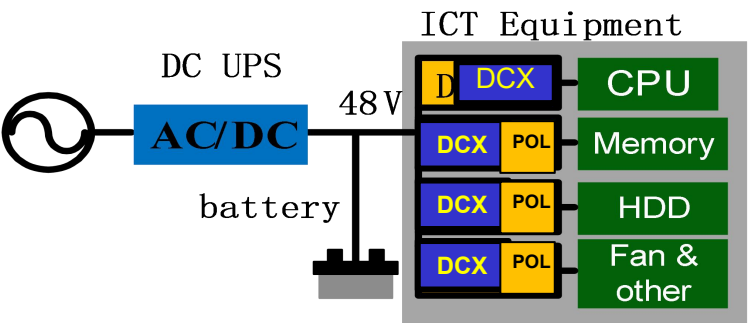


Conventional isolated D2Ds

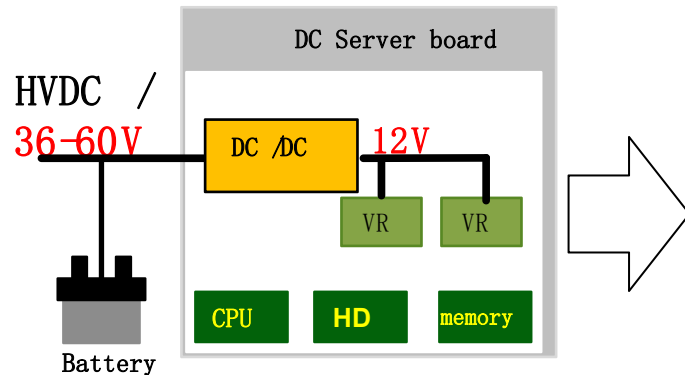
Intermedia bus



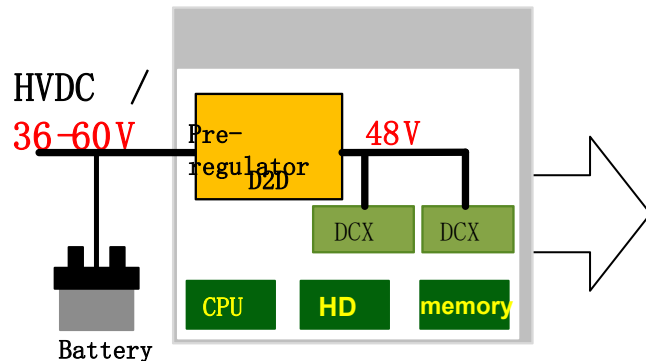
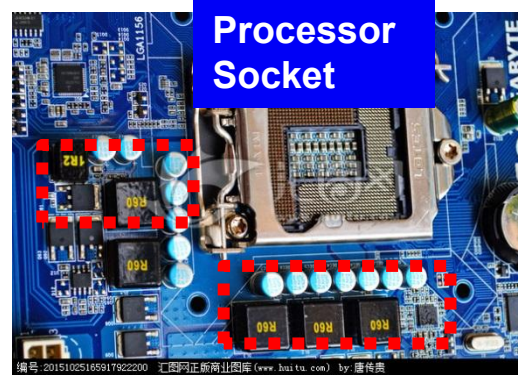
Server racks



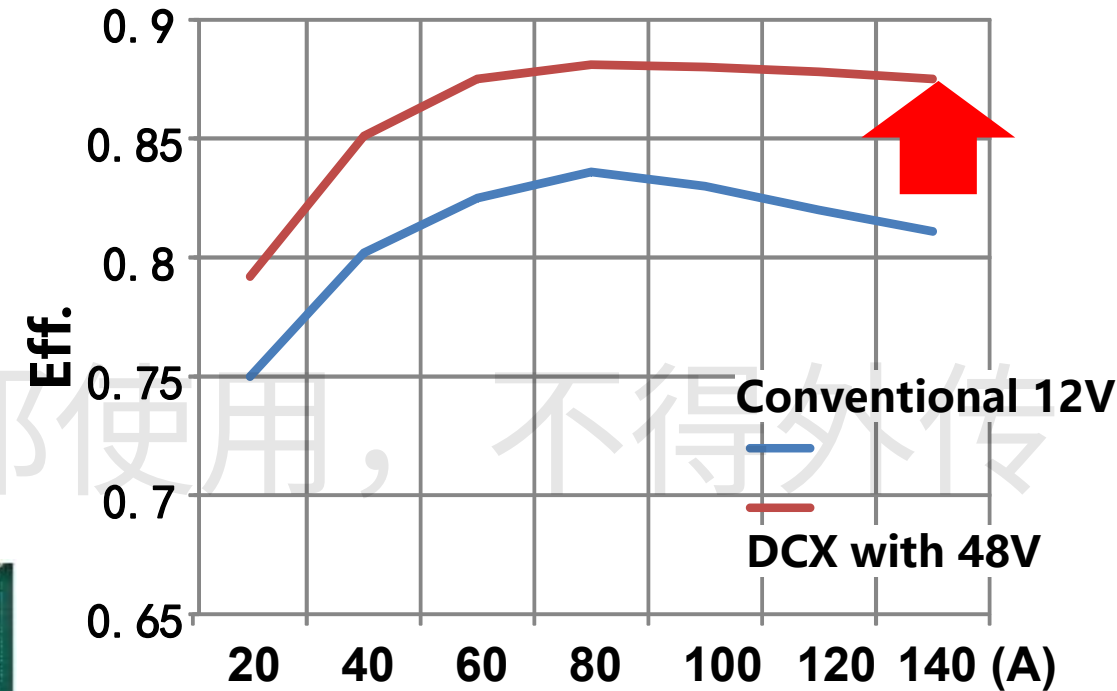
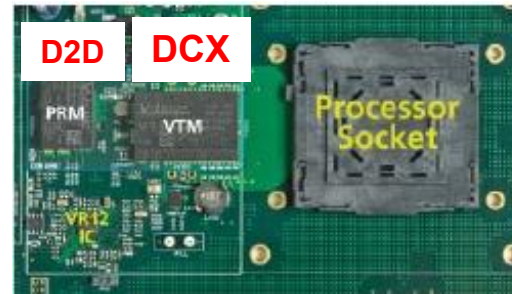
48V DC Bus Feeding the server Board Requires High Density Embedded DC/DC Module



12V Bus two stage (2012)



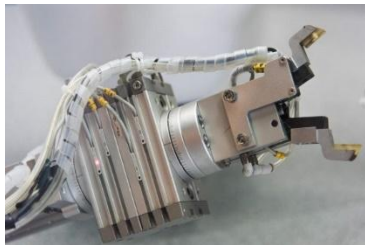
DCX two stages (2013)



- Higher Efficiency
- Higher Density

48V with Intermediate Bus for Low power low profile isolated power supply system

Industry robotics



Unregulated Intermediate Bus Architecture (IBA)

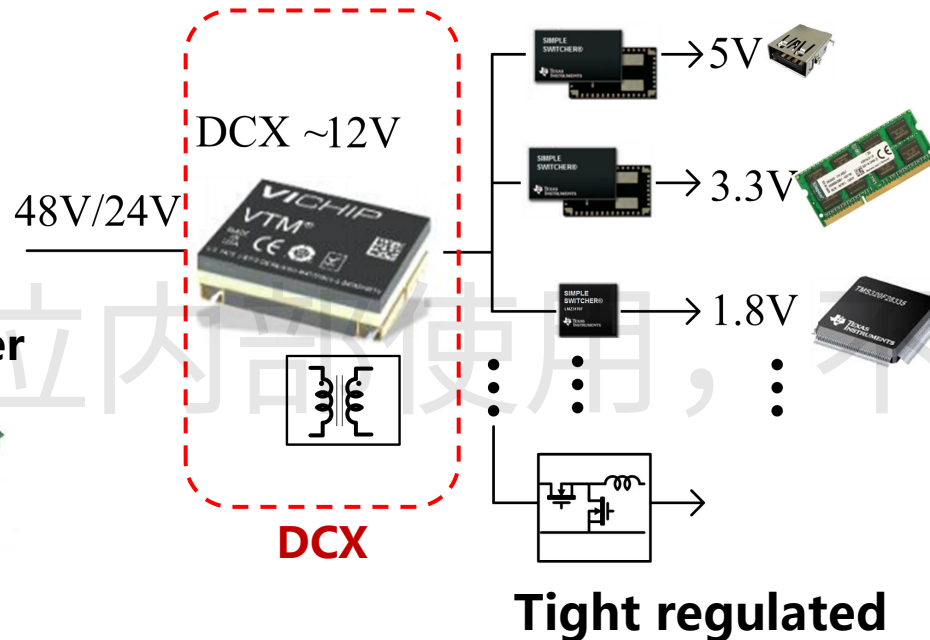
Telecom exchanger



Bias & driver



Portable instruments



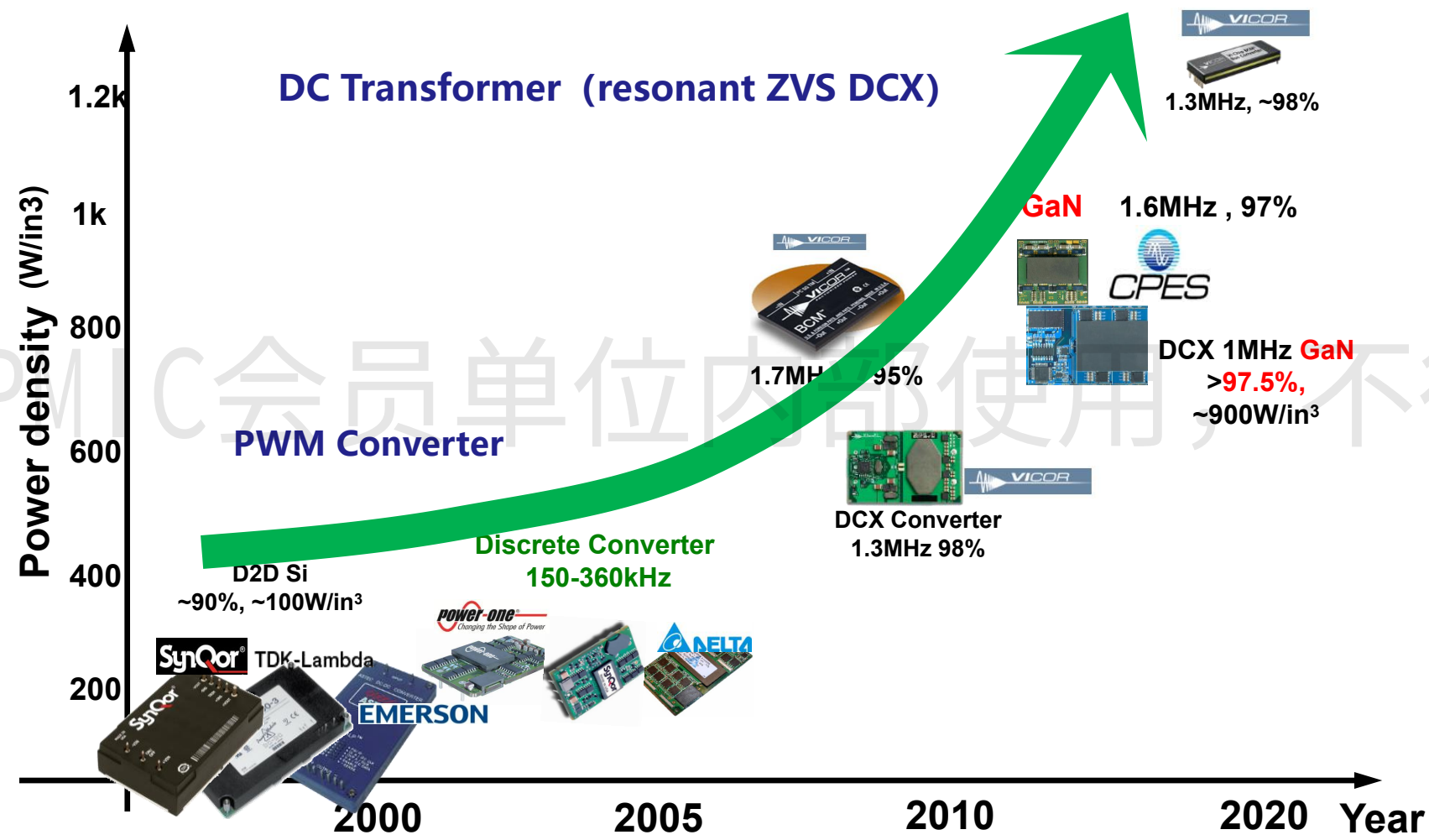
- ✓ Easy control
- ✓ Optimized magnetic components
- ✓ High efficiency

1. Introduction of power supply architecture of internet datacenter and popular high density high efficiency applications.
2. **Topology for MHz high efficiency 380V-48V/12V power conversion**
 - 2.1 **Unregulated DC-DC (DCX) techniques**
 - 2.2 EMI design considerations of planar PCB transformer
 - 2.3 Tight regulated 380V-48V&12V conversion
3. **MHz high efficiency 48/12V/XV power converters**
 - 3.1 Low power DCX converter for intermedia bus application.
 - 3.2 Tight regulated DC-DC converter for 48V-12V in server
 - 3.3 High Density Transformer Design for 48V MHz DC-DC converter

4. Conclusions



Trends of Isolated 380V DC-DC Power Modules



Unregulated ZVS Resonant DCX Topologies



Si
~ 1 MHz,
~98%

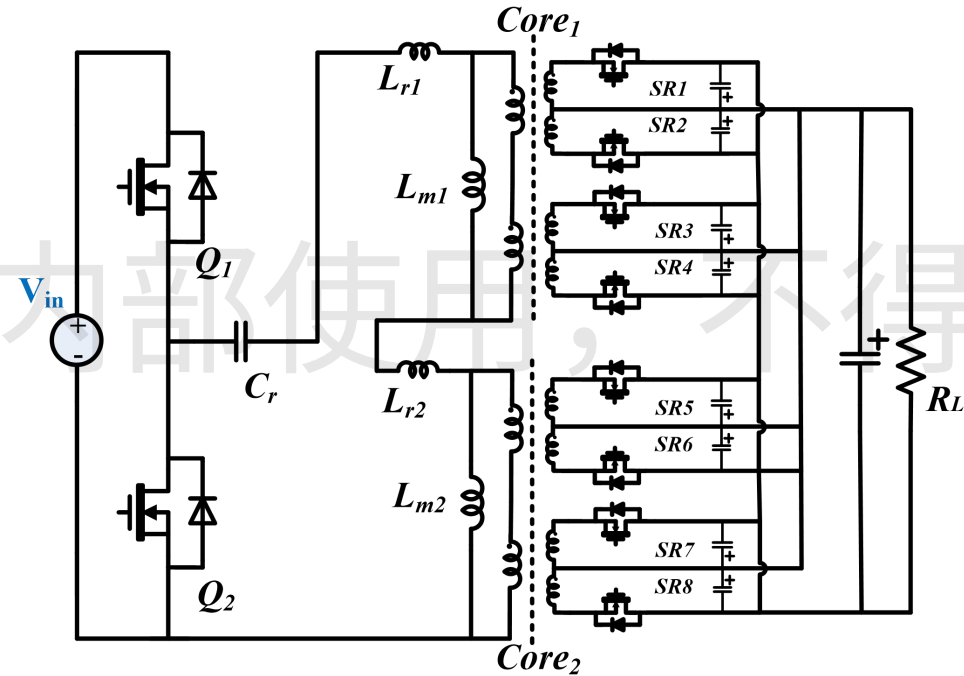


GaN
DCX 1MHz GaN
6 Layer PCB
97.5%, 900W/in³
(2017)



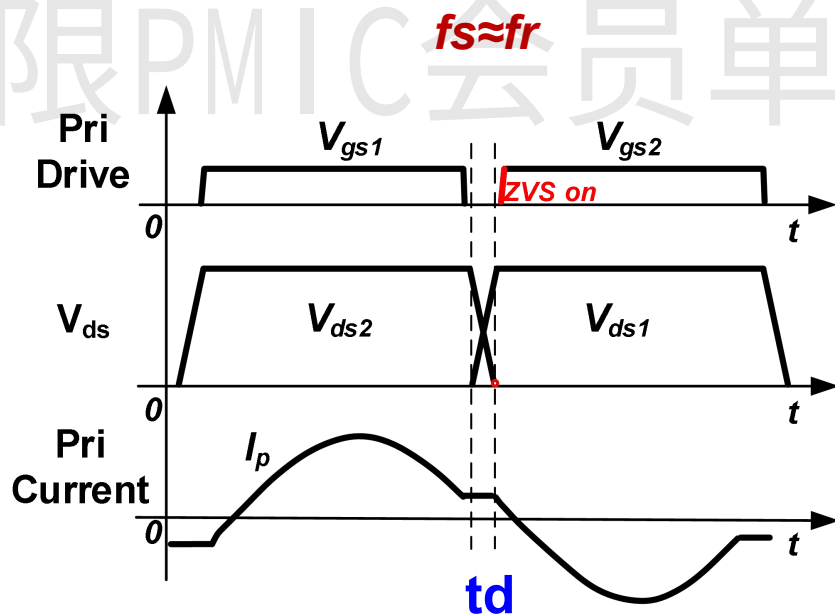
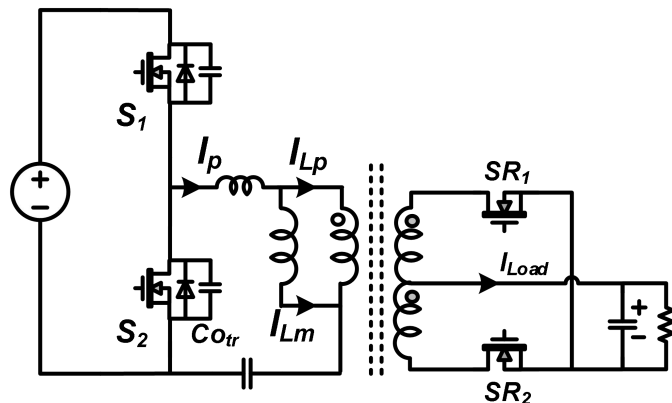
48V-12V
1MHz, >98%
(2019)

- LC series resonant topology
- Matrix transformer

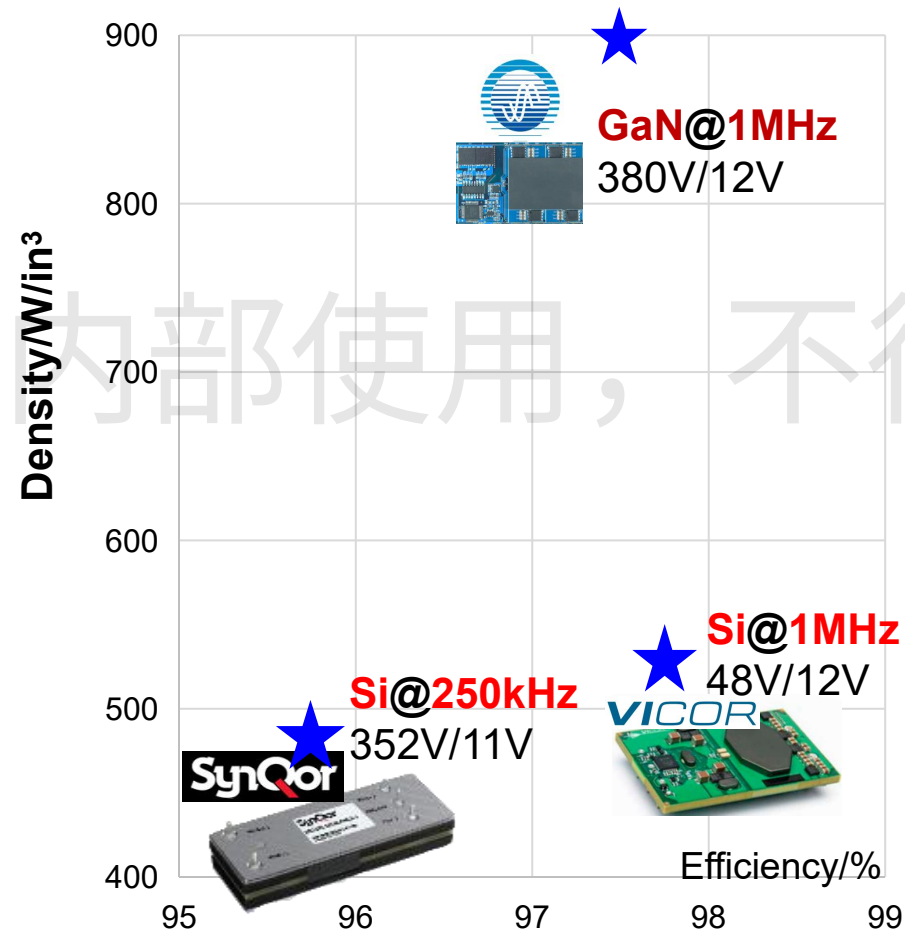


- ☺ ZVS On
- ☺ ZCS Off
- ☺ No Reverse Recovery

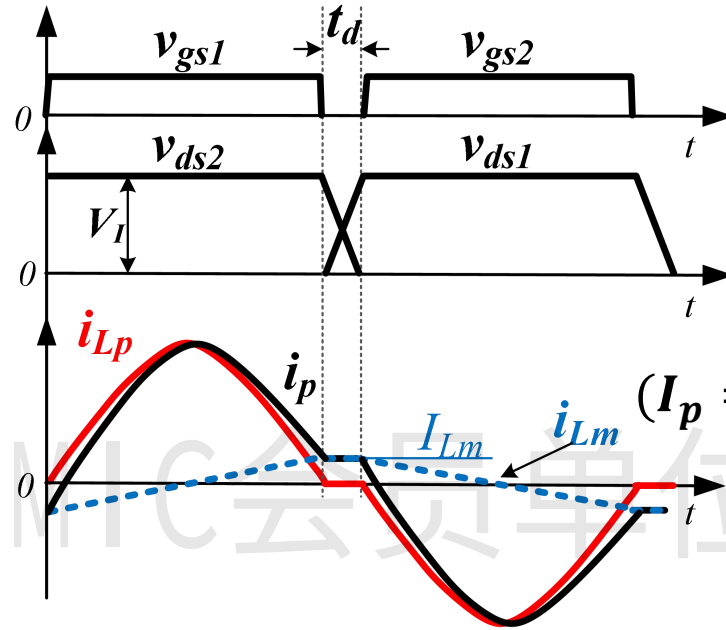
Comparison of High Frequency DCX



State of the art of DCX Module



Conduction loss of Primary Switches Makes the Major Difference



Primary Conduction loss:

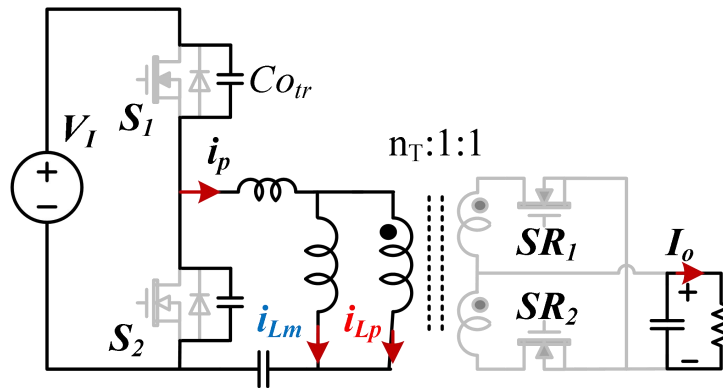
$$P_{Con} = I_{prms}^2 R_{dson}$$

1. Load current

$$I_{Lp} = \frac{I_o}{n_T}$$

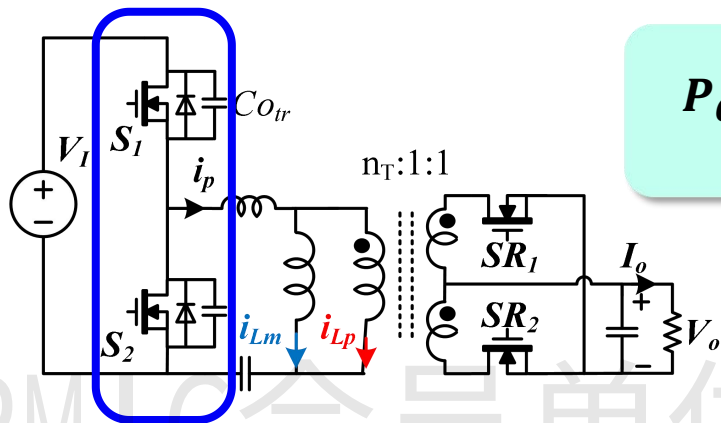
2. Magnetizing current

$$I_{Lm} = \frac{V_I \cdot 2C_{o_{tr}}}{t_d}$$



ZVS Transition in dead time

Primary Switches Loss model



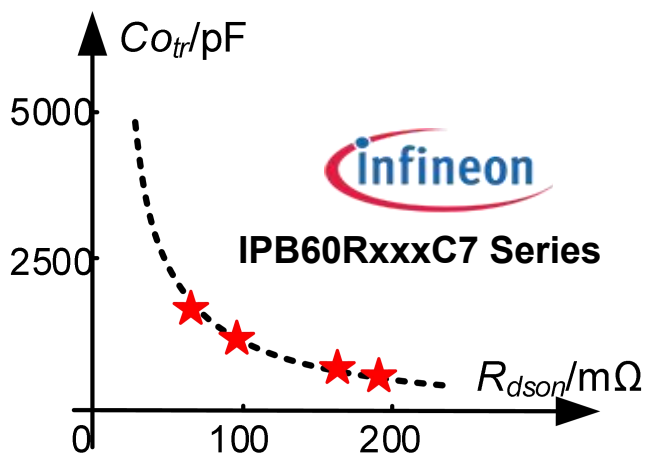
$$P_{Con}(R_{dson}, C_{otr}) = \left(\frac{8n_T^2 V_o^2 T_r \cdot C_{otr}^2}{t_d^2 T_s} + \frac{\pi^2 T_s \cdot I_o^2}{8n_T^2 T_r} \right) \cdot R_{dson}$$

Variable elimination

$$C_{otr} = \frac{NFoM}{R_{dson}}$$

Constant:

$$NFoM = R_{dson} \cdot C_{otr}$$



Simplified Conduction loss model

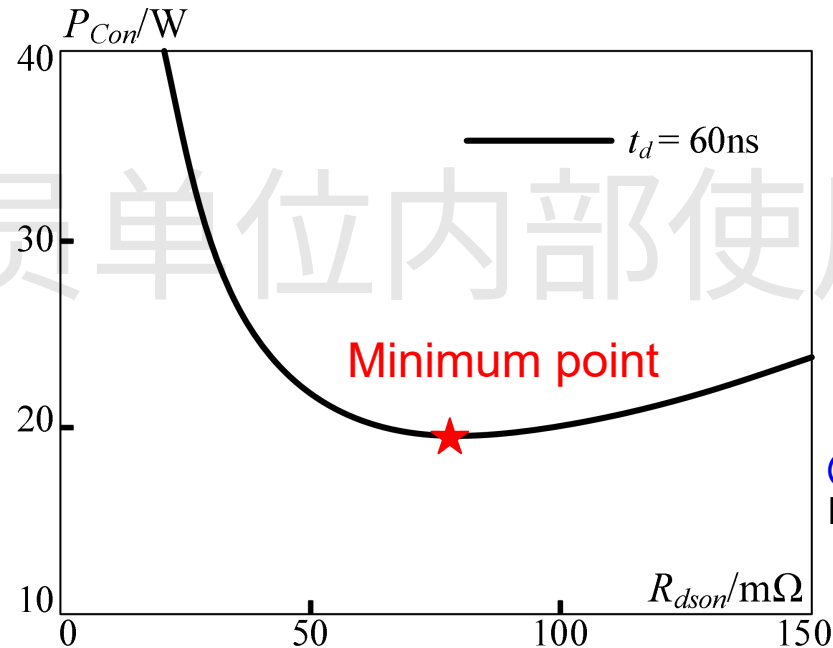
Conduction Loss
model

$$P_{Con}(R_{dson}) = A \cdot \frac{1}{R_{dson}} + B \cdot R_{dson}$$

A and B: Constant

$$A = \frac{8n_T^2 V_o^2 T_r * NFoM^2}{t_d^2 T_s}$$

$$B = \frac{\pi^2 I_o^2 T_s}{8n_T^2 T_r}$$



$$P_{Con}(R_{dson}) \geq 2\sqrt{AB} = P_{Cmin} = \frac{2\pi P_o \cdot NFoM}{t_d}$$

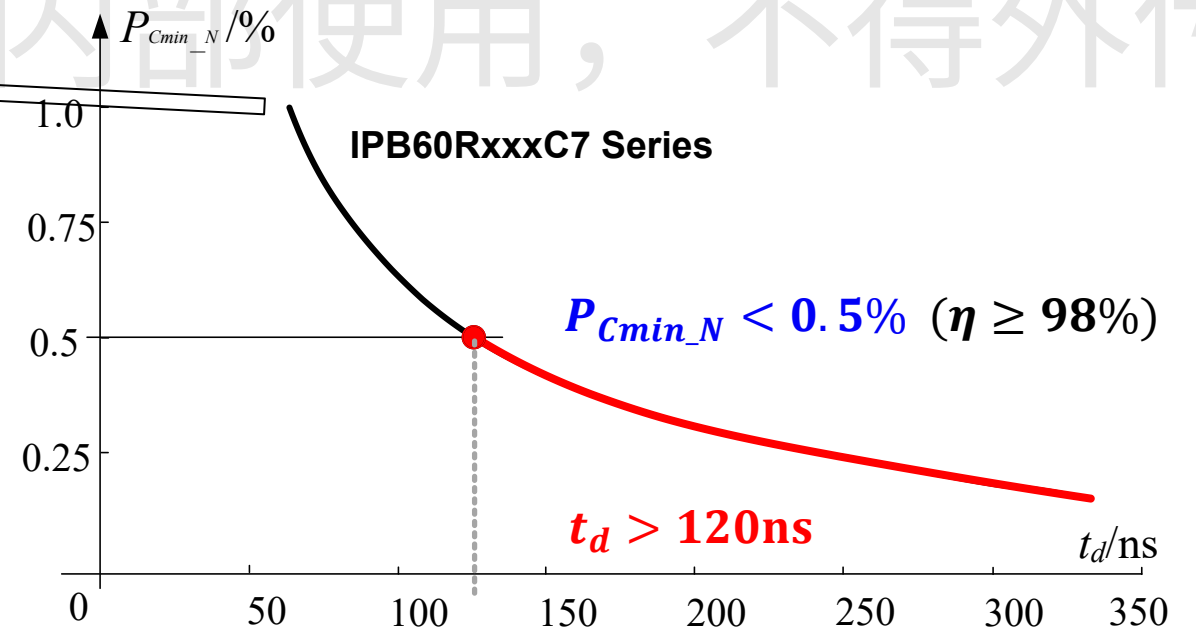
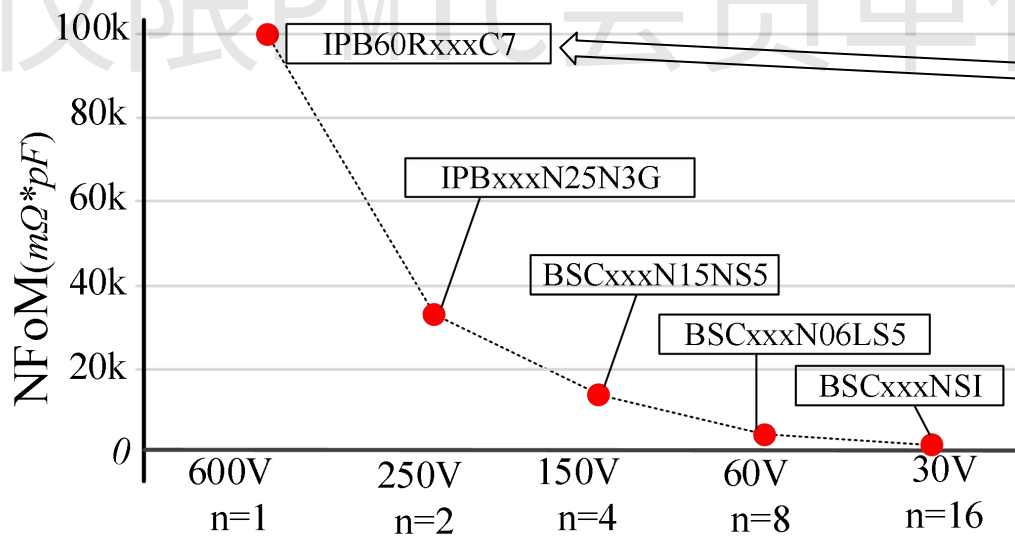
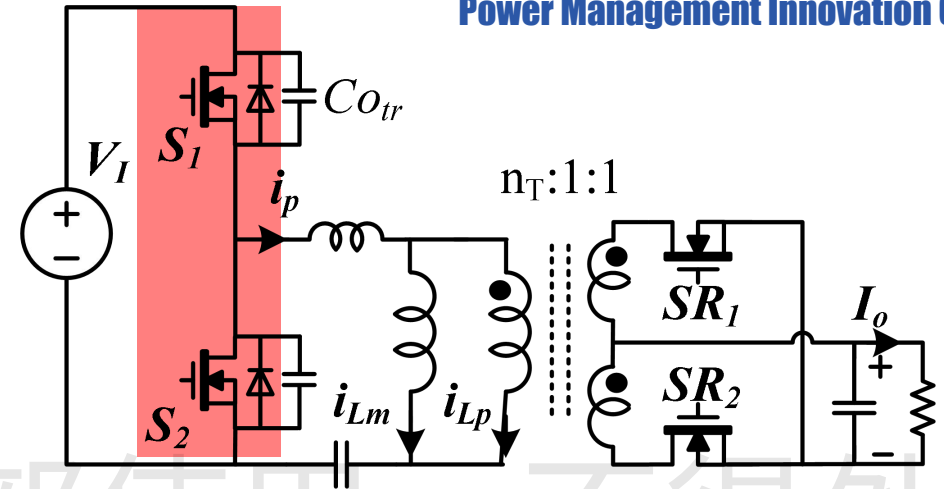


Primary Side High Voltage Si with Large NFoM Requires Large t_d

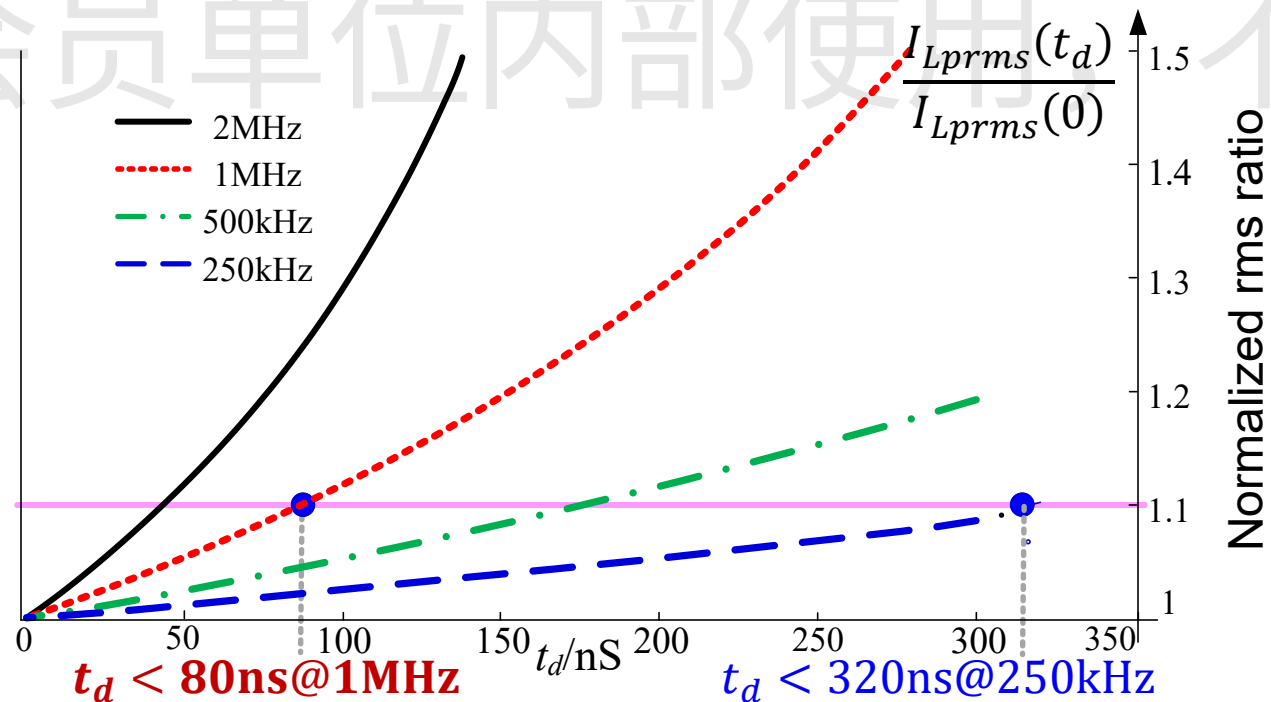
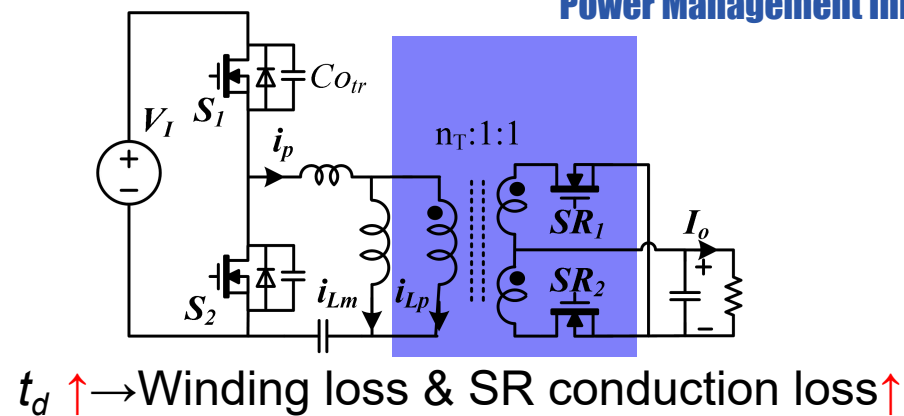
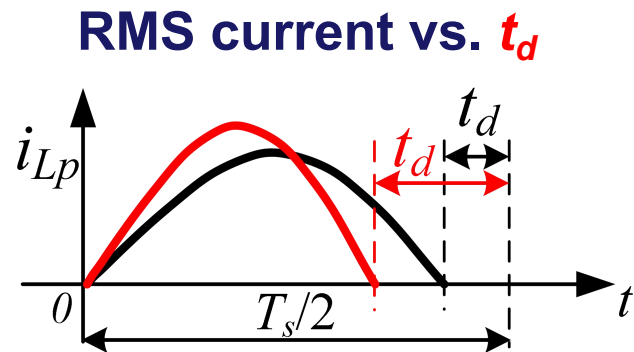
Normalized primary switch conduction loss:

η : efficiency

$$P_{Cmin_N} = \frac{P_{Cmin}}{P_o} = \frac{2\pi\eta * NFoM}{t_d}$$

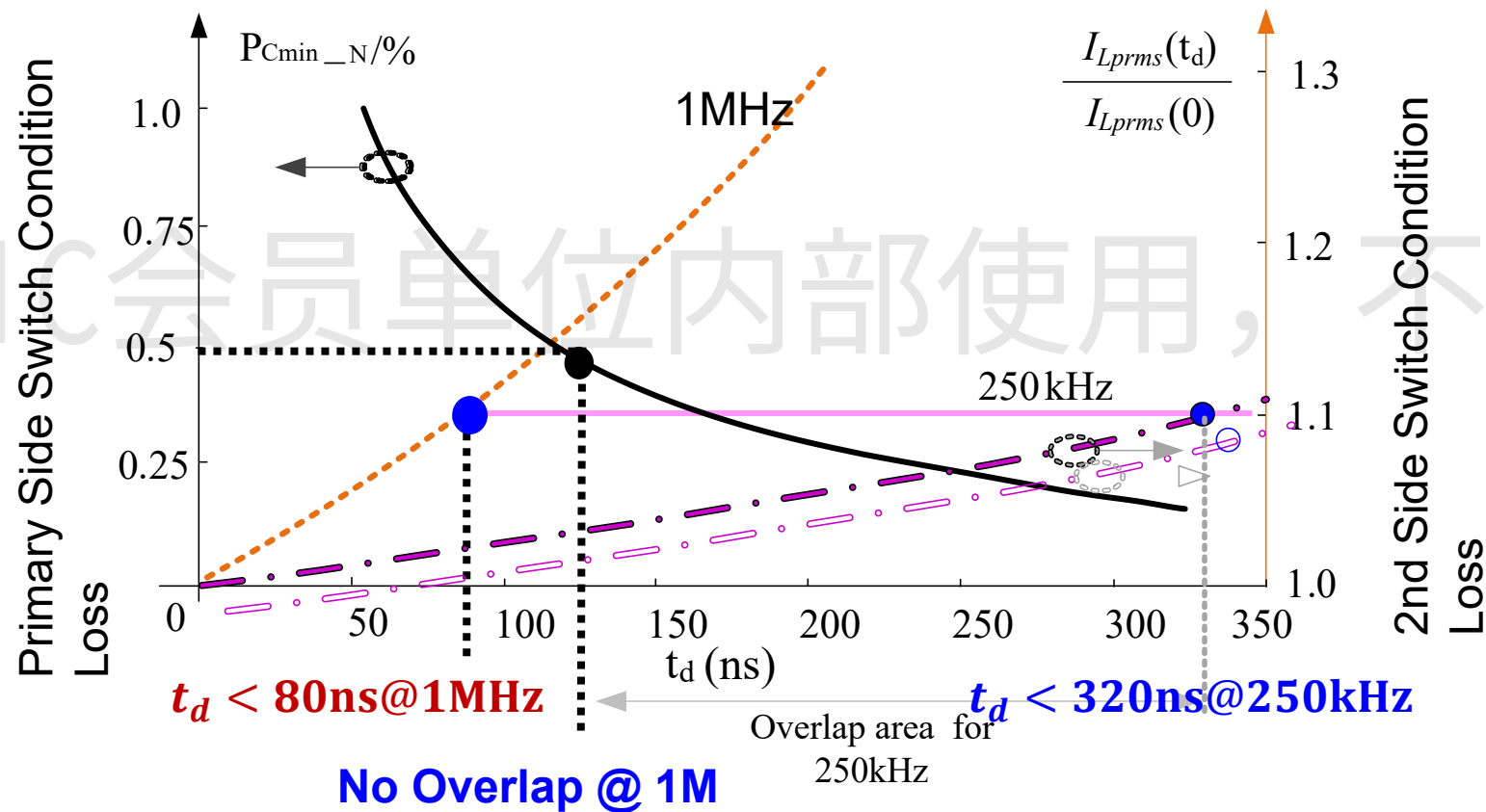


2nd Side High Frequency Design Requires Low t_d



P_{Cmin} and t_d @ given NFoM Devices

$$P_{Cmin_Normalized} = \frac{2\pi * \eta * NFoM}{t_d}$$

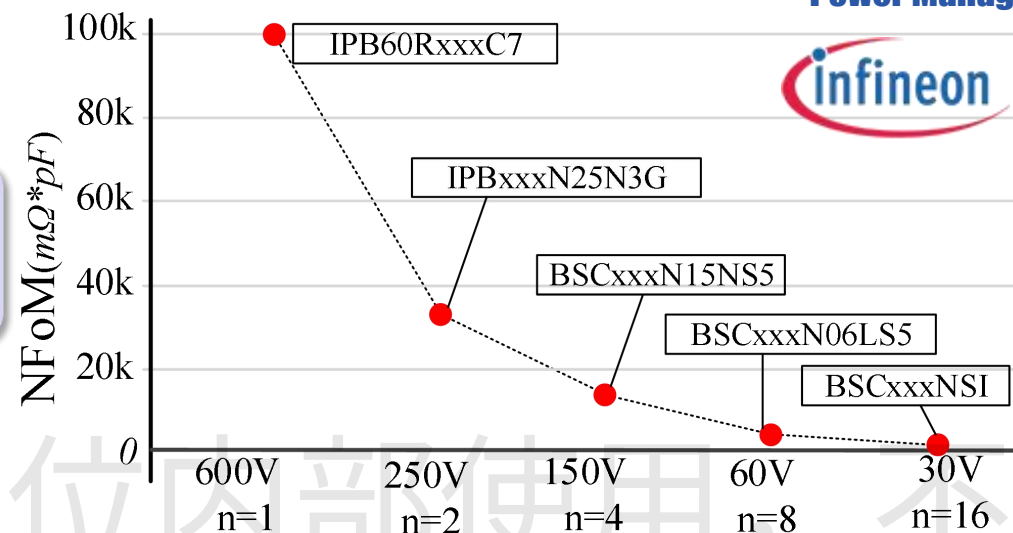


Series-connected Low Voltage Devices = Single Device NFoM

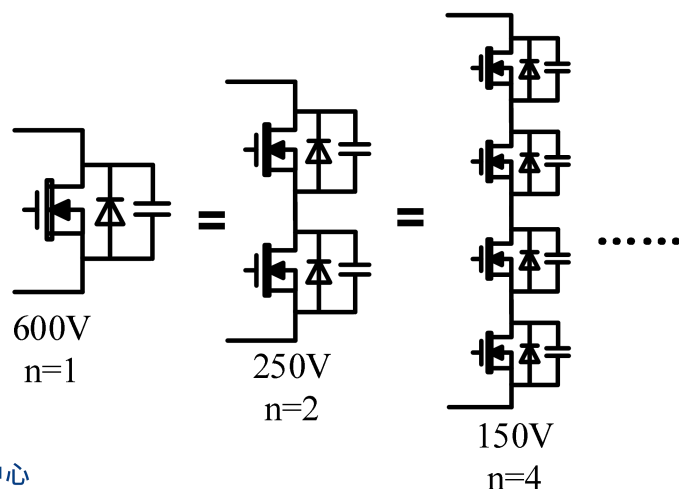
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Low $V_{(BR)DSS}$ = Low NFoM

$$P_{Cmin} = \frac{2\pi * P_o * NFoM}{t_d}$$



Series-connected low $V_{(BR)DSS}$ devices

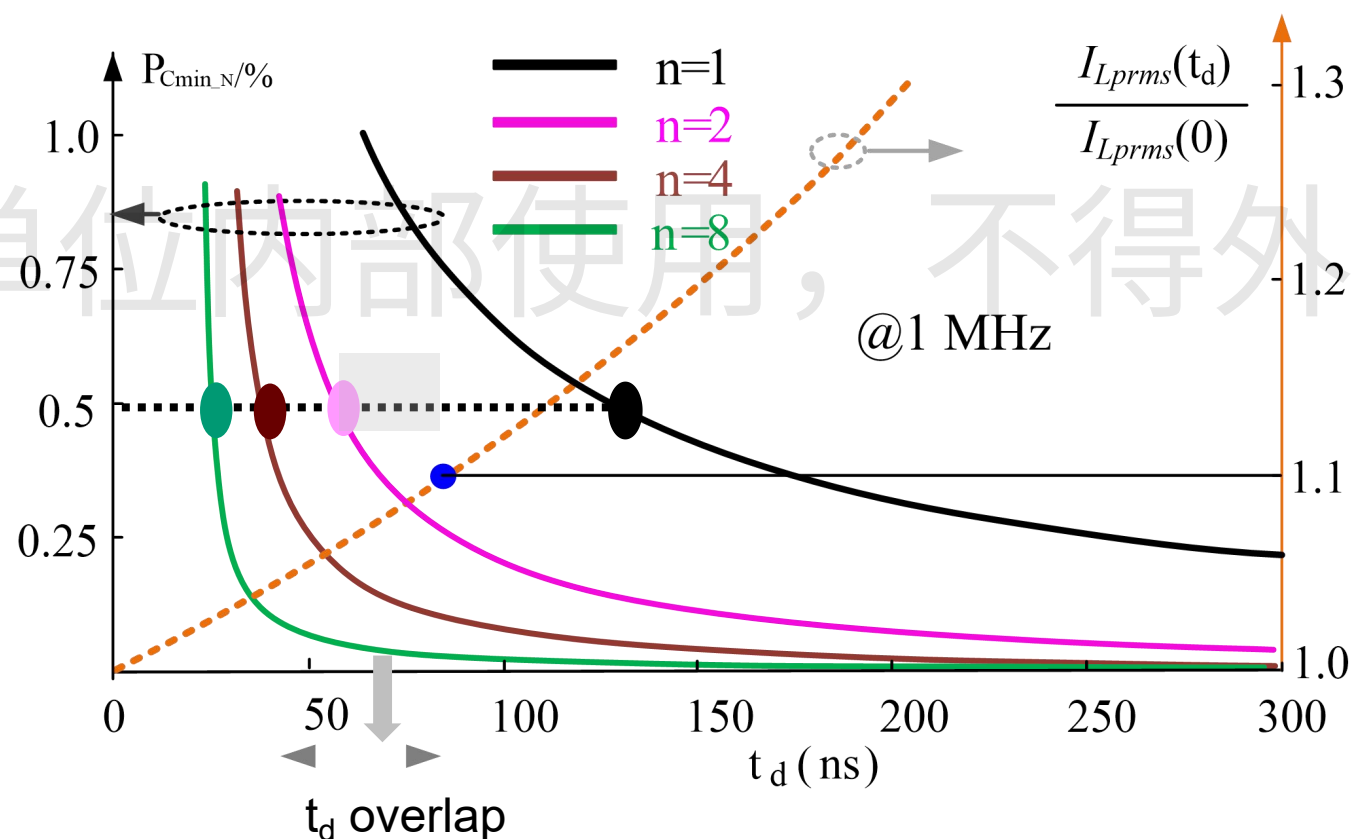
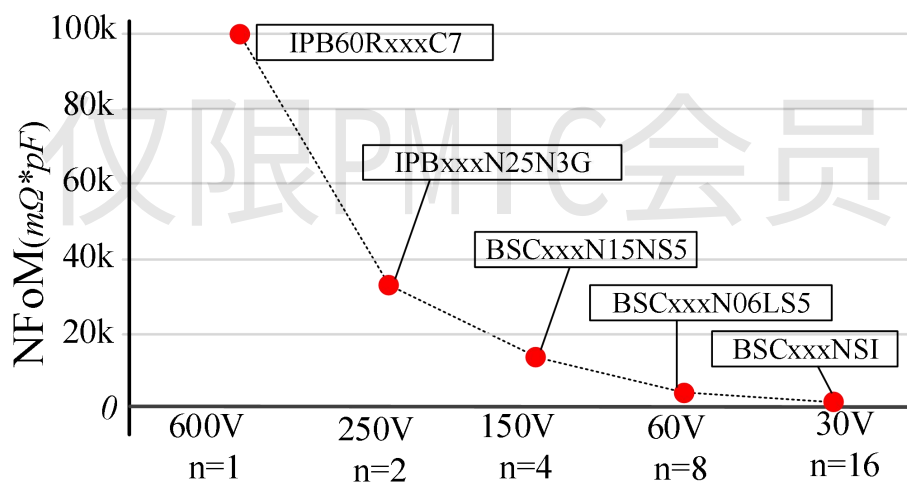


$$NFoM = (\cancel{n}R_{dson}) \cdot \frac{C_{otr}}{\cancel{n}}$$



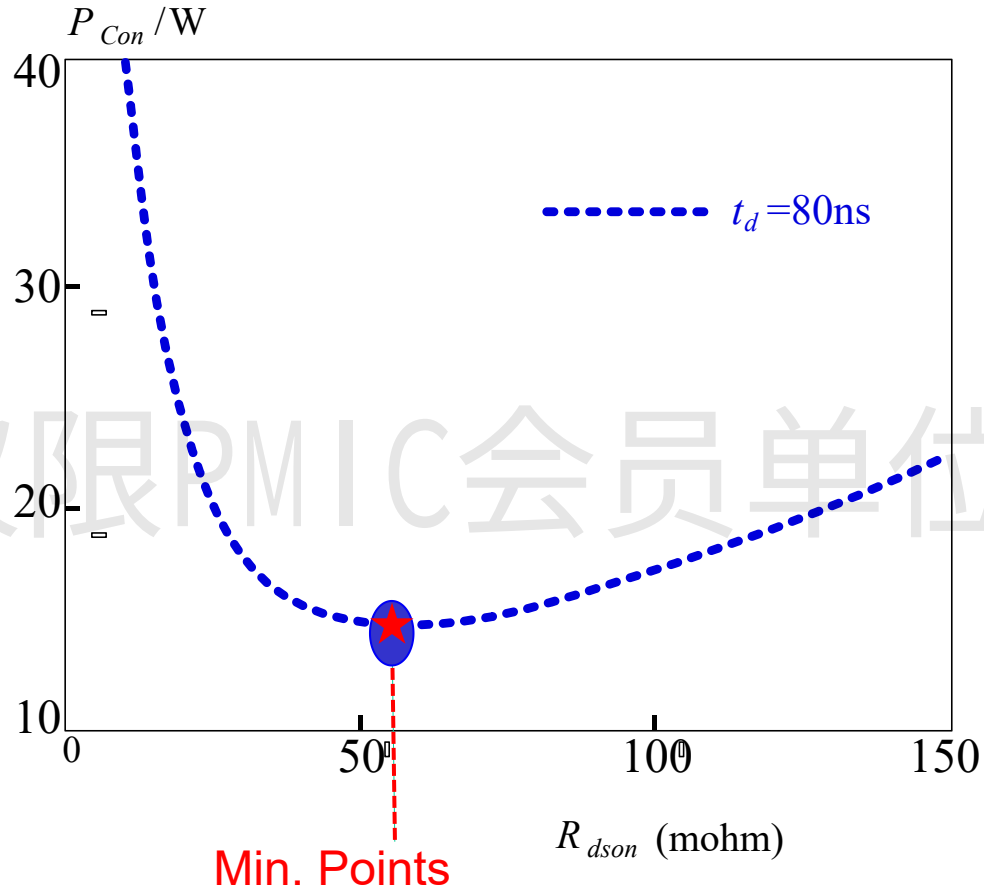
P_{Cmin} and t_d @ Different NFoM Devices

$$P_{Cmin_Normalized} = \frac{2\pi * \eta * NFoM}{t_d}$$



Primary Side Device selection @ given power with 1MHz

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Conduction loss model

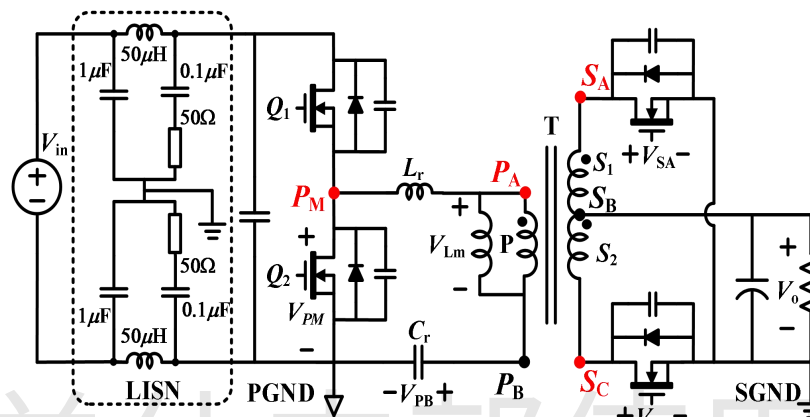
$$P_{Con}(R_{dson}) = A \cdot \frac{1}{R_{dson}} + B \cdot R_{dson}$$

$$A = \frac{8n_T^2 V_o^2 T_r * NFoM^2}{t_d^2 T_s} \quad B = \frac{\pi^2 I_o^2 T_s}{8n_T^2 T_r}$$

$$R_{dson@min} = \sqrt{\frac{A}{B}} = \frac{8n_T^2 V_o T_r \cdot NFoM}{\pi t_d I_o T_s}$$

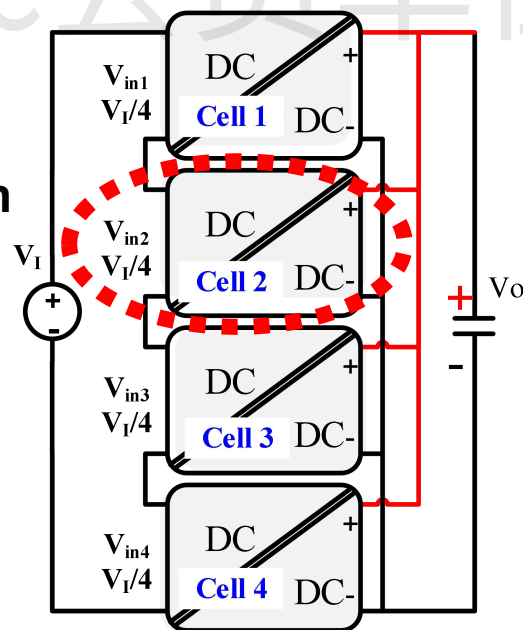
MHz DCX Topology Based on Low NFoM Devices

High voltage switch scheme

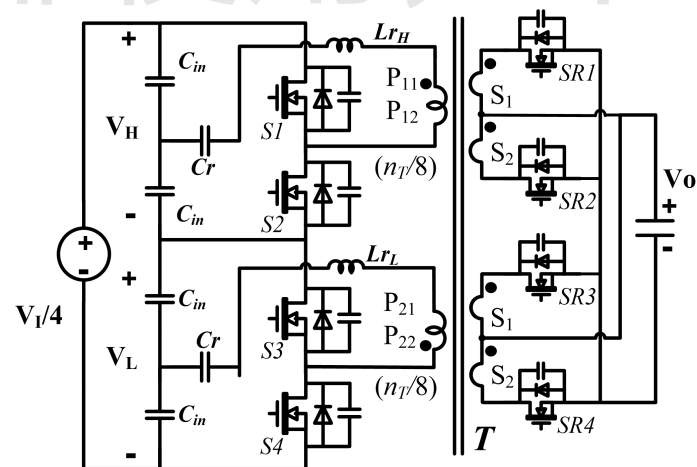


V_{in} : 380
 V_o : 12V/150A

Low voltage switch scheme



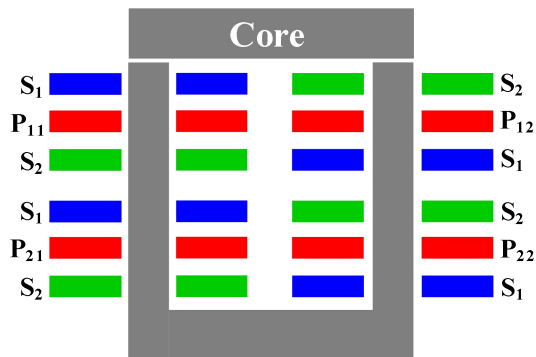
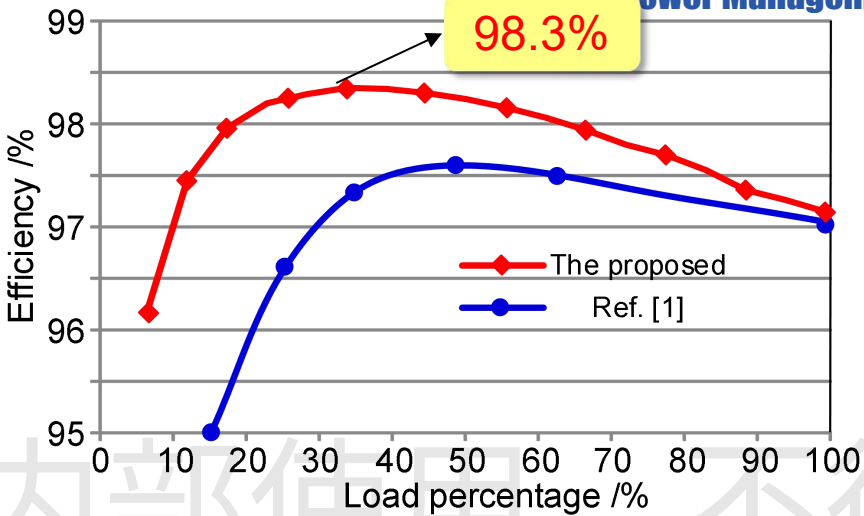
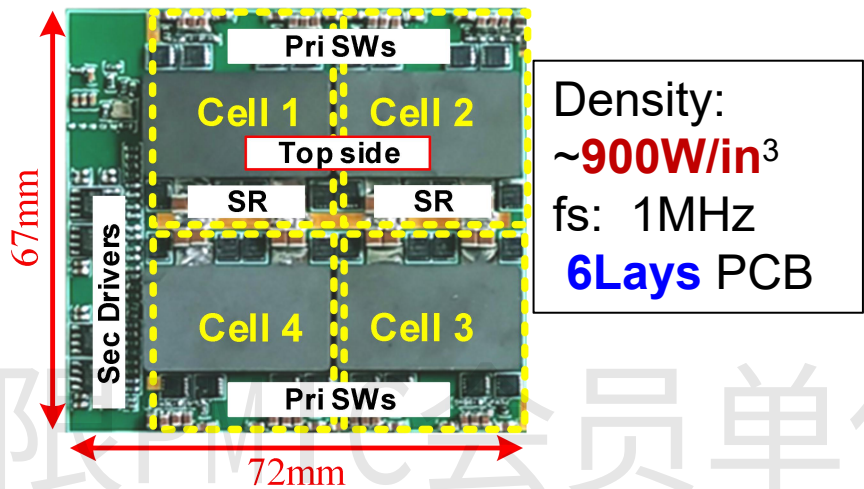
$n = 8$



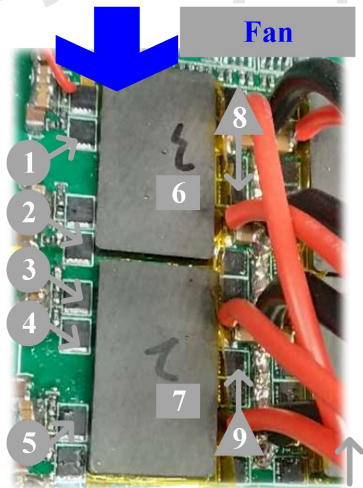
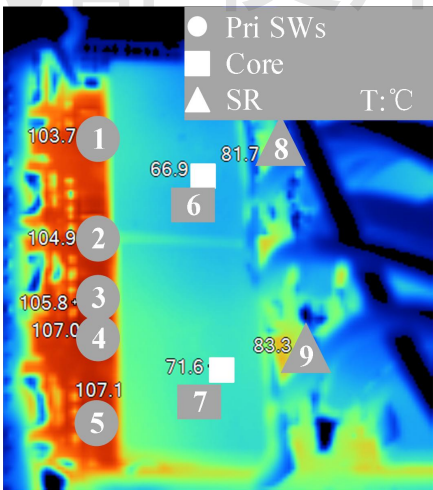
Cell circuit

SRC DCX

Verification: 380V-12V/150A DCX Prototype



Cell Transformer winding structure

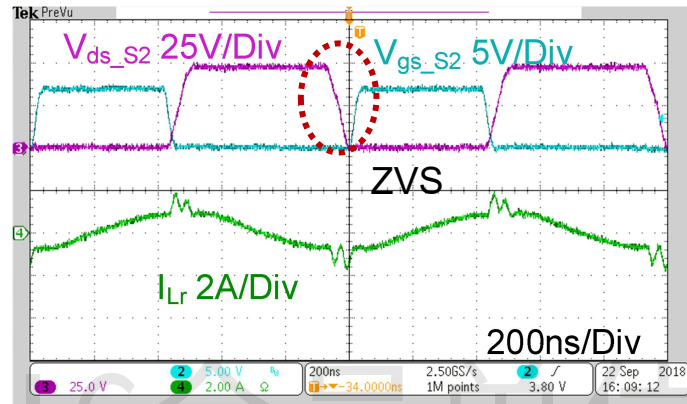


[1].C. Fei, F. C. Lee and Q. Li, "High-Efficiency High-Power-Density LLC Converter With an Integrated Planar Matrix Transformer for High-Output Current Applications," in IEEE Transactions on Industrial Electronics, vol. 64, no. 11, pp. 9072-9082, Nov. 2017.

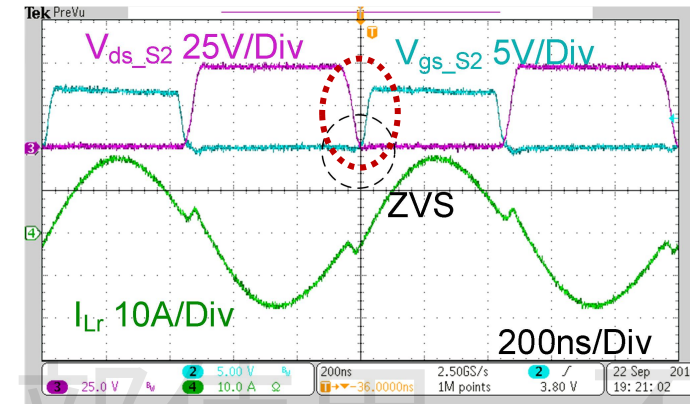
[propose] Xinke Wu. Hongbo Shi. "High Efficiency High Density 1 MHz 380–12 V DCX With Low FoM Devices" IEEE TIE 2019. pp1648-1656

Measured Key waveforms of the prototype

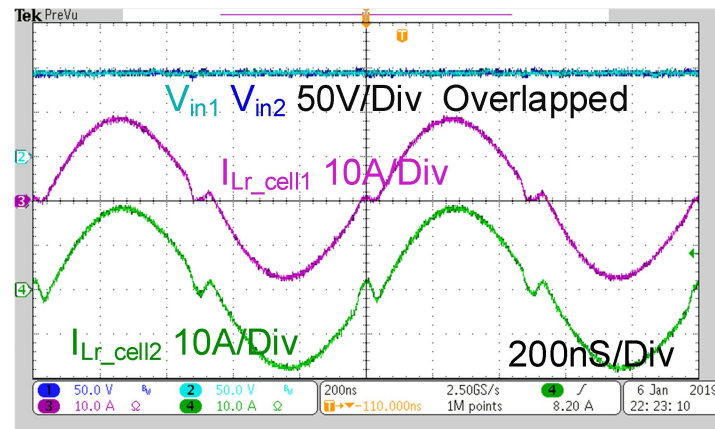
➤ Waveforms at full load range



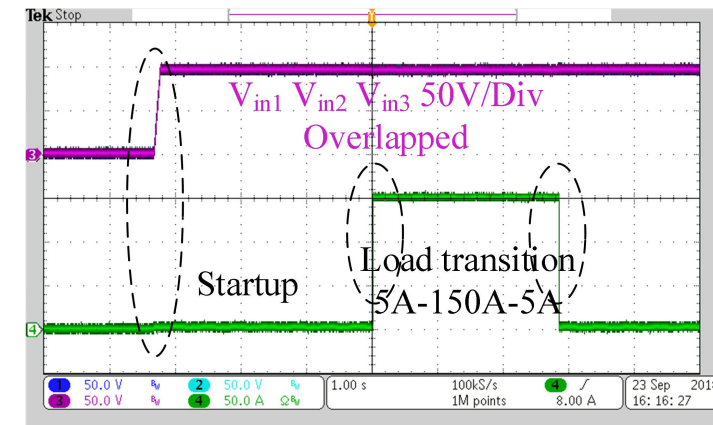
380V_{in}@null load



380V_{in}@full load



Voltage and current sharing



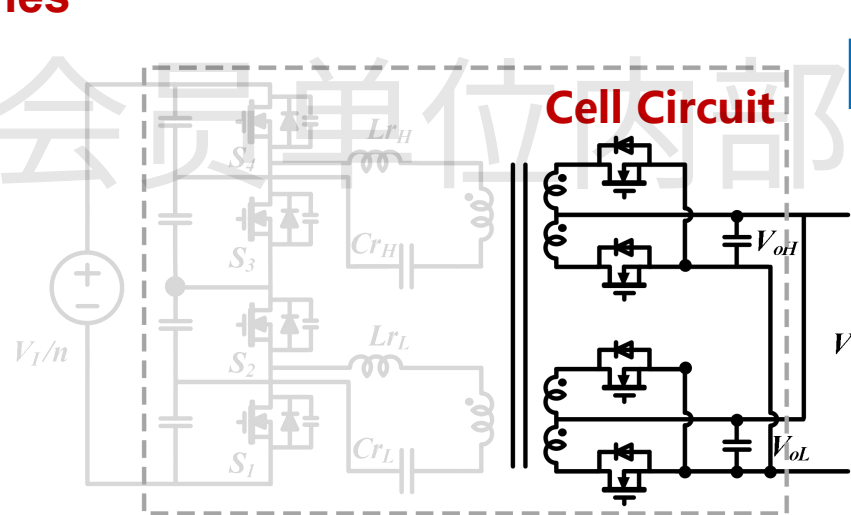
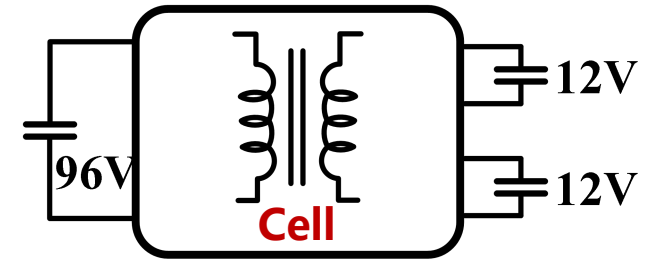
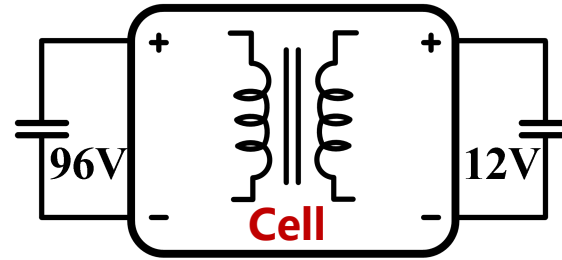
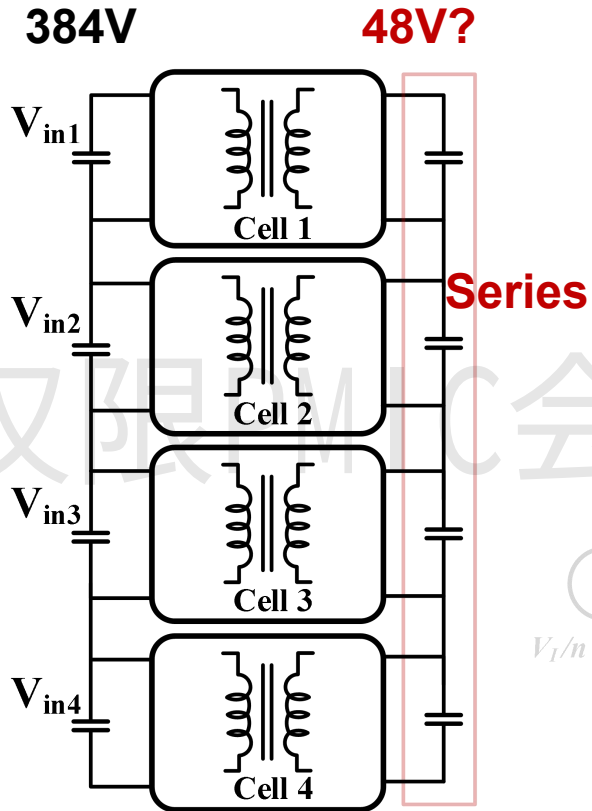
Start up and load transition

Cell Circuit Structure with Output Voltage Adaptation

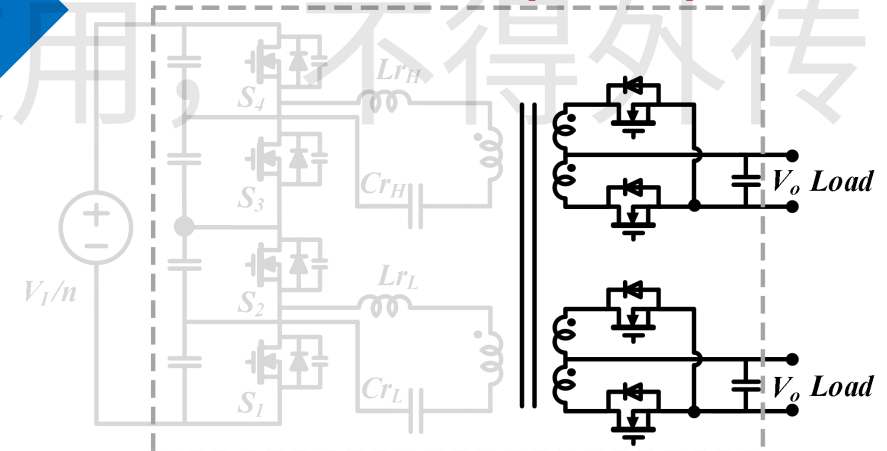


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- For wide output voltage adaptation



Cell Circuit with split outputs



☹ Imbalance for voltage sharing

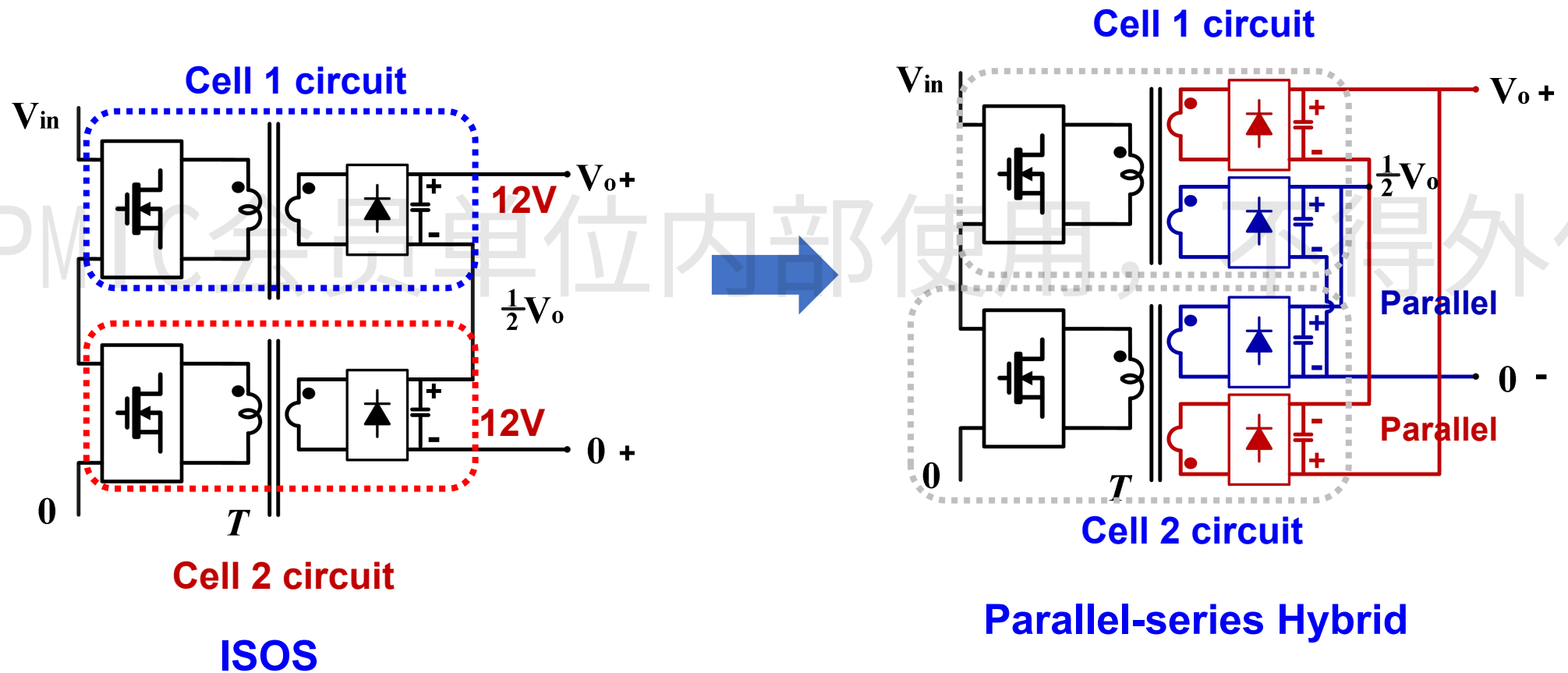


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380V-48V Output DCX Input-series Output-series (ISOS)

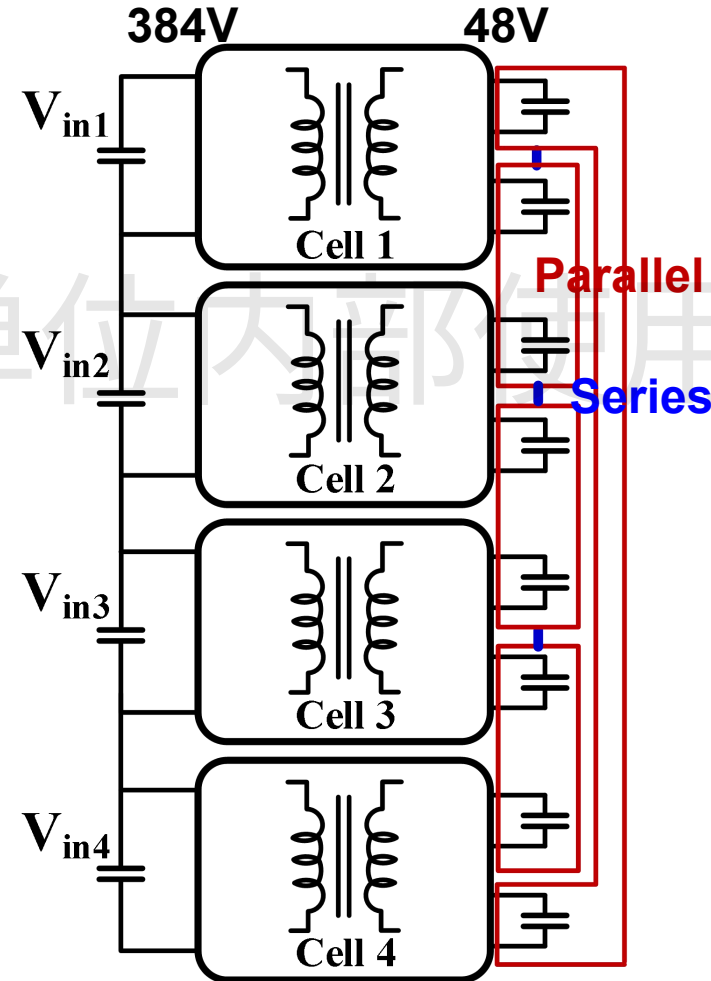
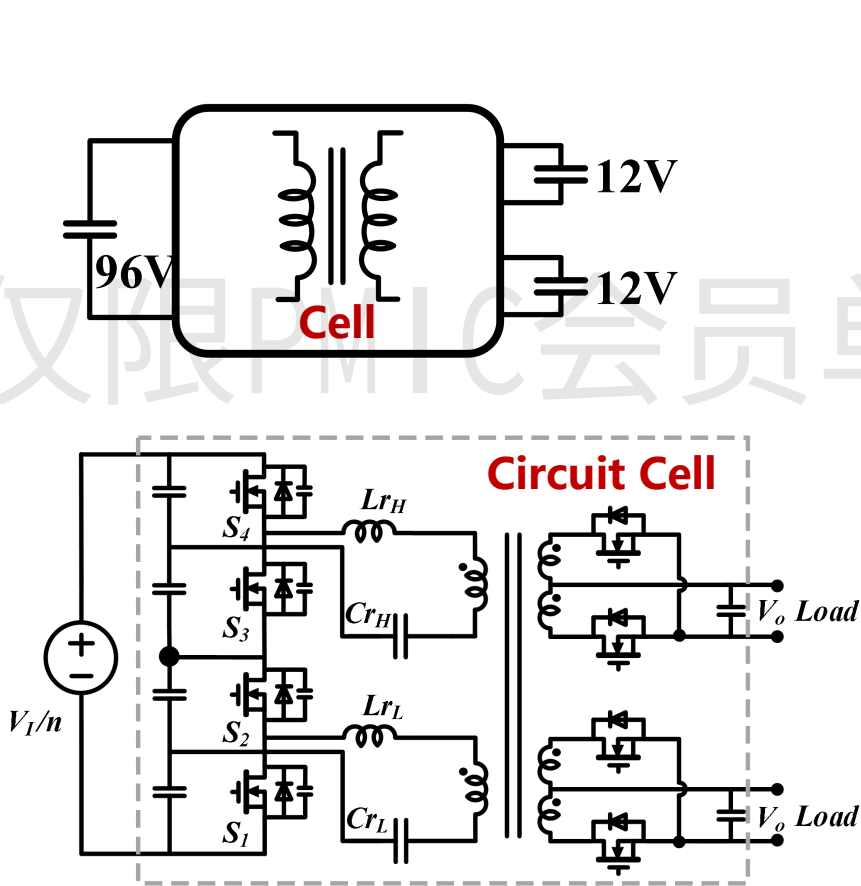
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- voltage sharing of series connected cell circuit



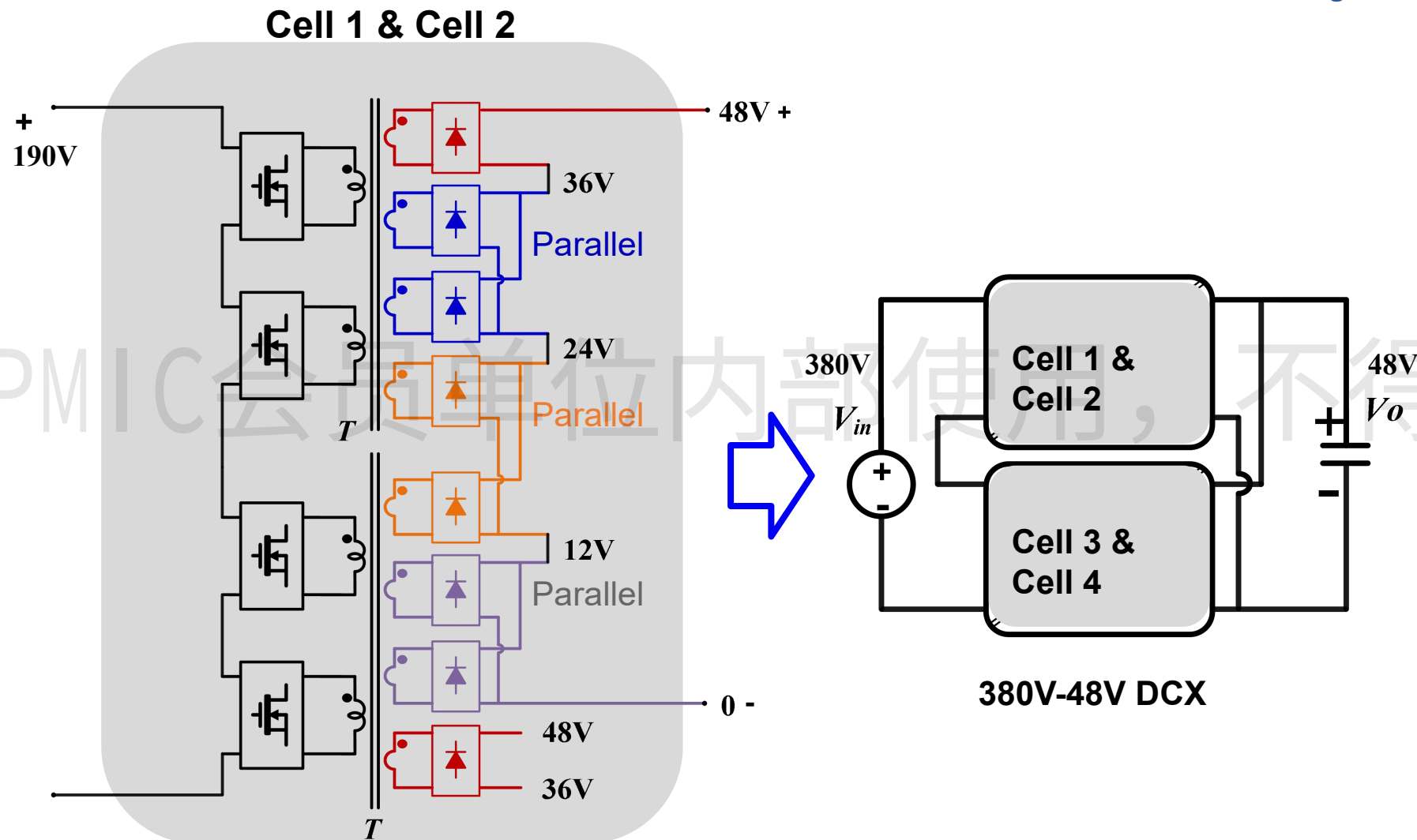
380V/48V SRC Based on Low Voltage Si Devices

- Chain structure with balanced voltage sharing ability



- With low voltage low NFoM devices
- Scalable structure with balanced voltage sharing

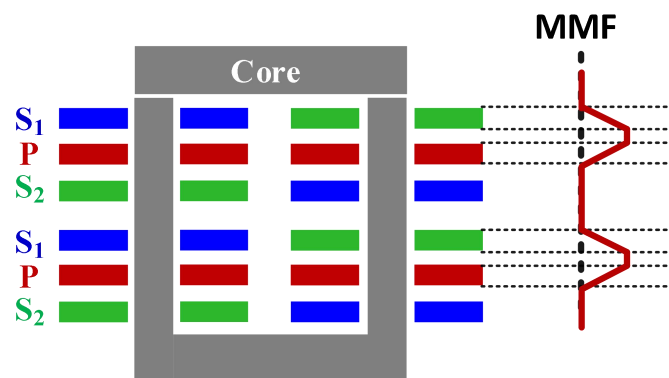
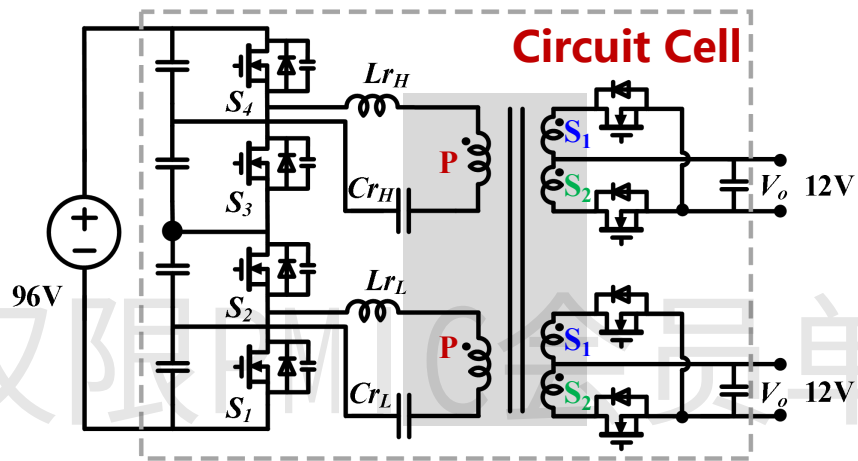
Daisy Chain Structure for 48V output



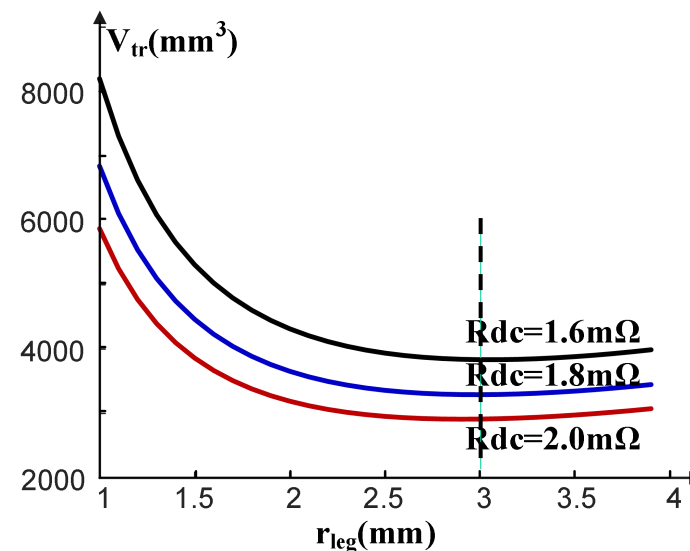
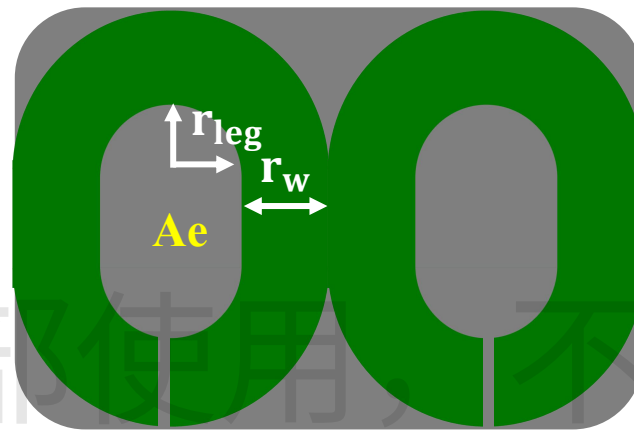
Design of the PCB transformer

□ Winding arrangement

□ Design @12V/turn, 60mT $B_{\max}$



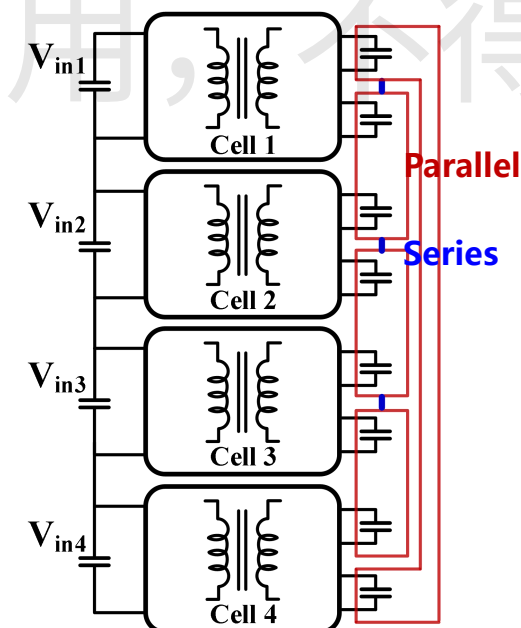
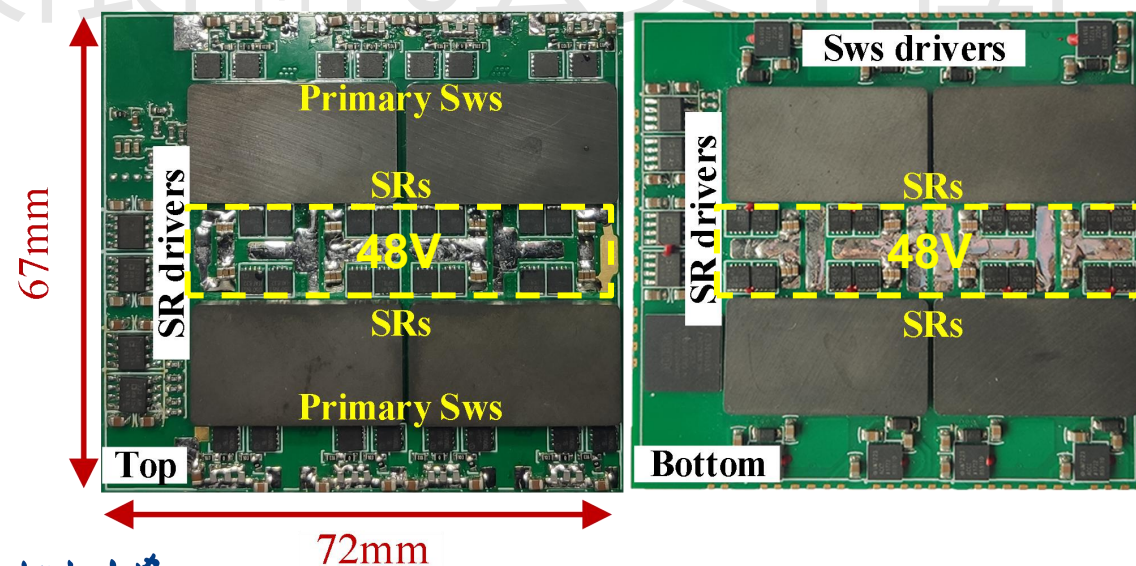
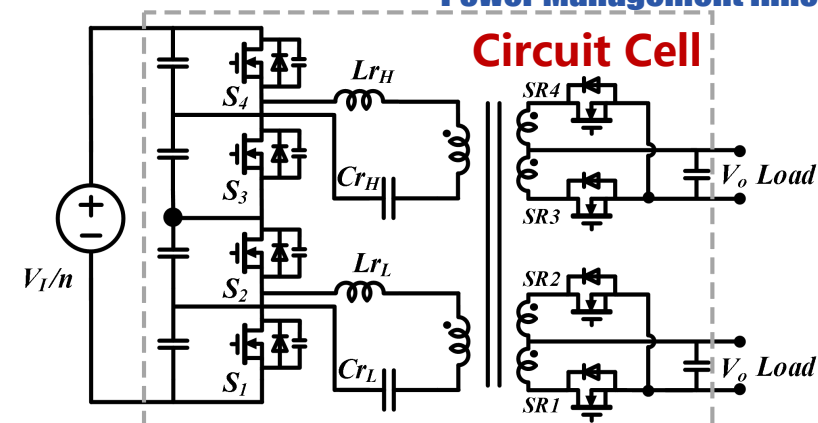
Fully interleaved



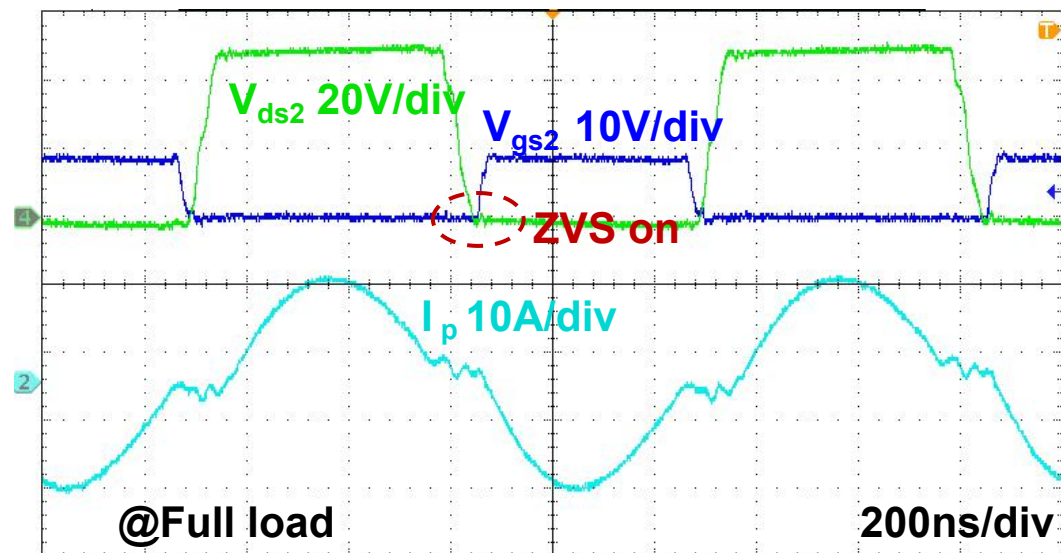
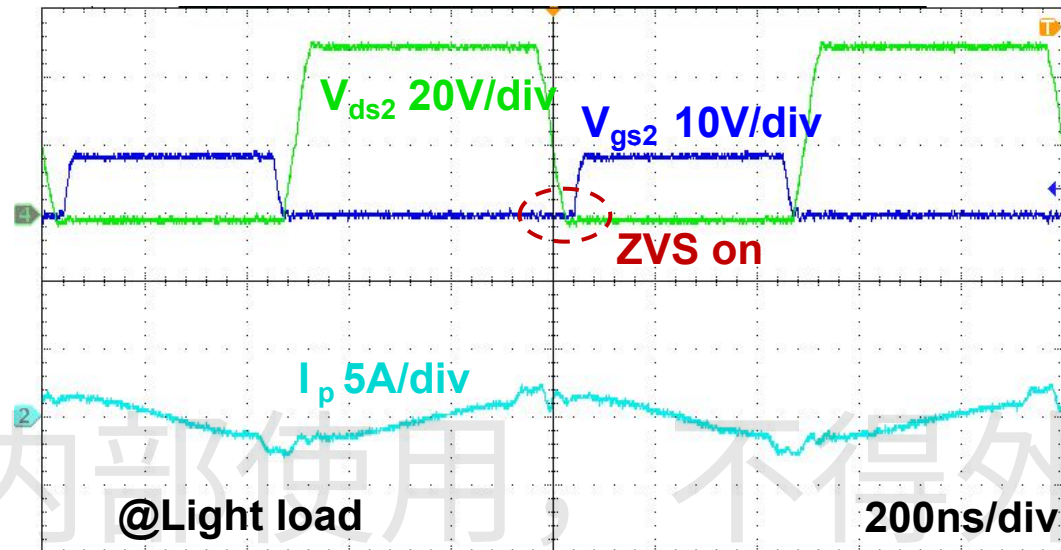
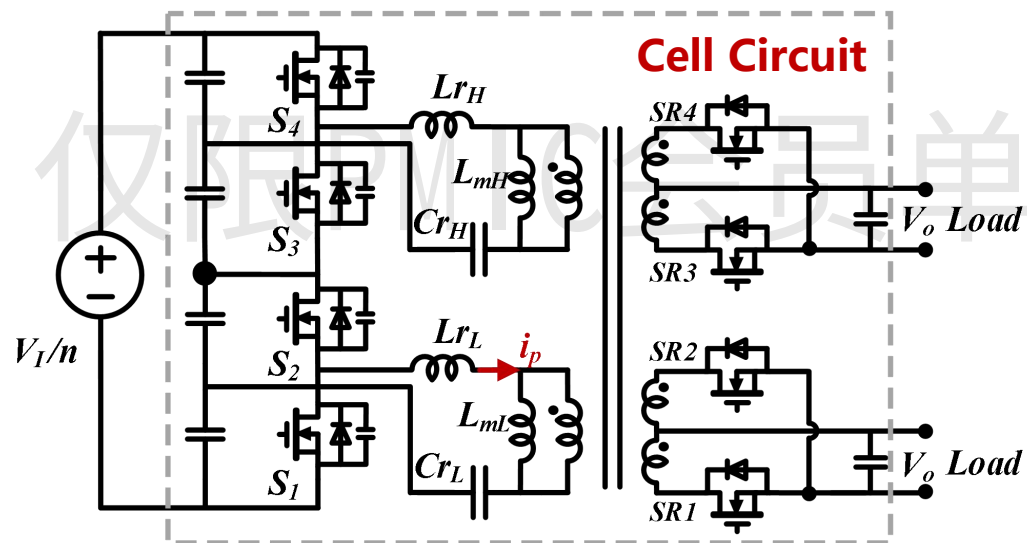
Key parameters and topology

➤ Key parameters

V_{in}	380V	V_o	48V
I_o	37.5A	f_s	1MHz
$S1 \sim S4$	BSZ040N06LS5	T	4:1:1
$SR1 \sim SR4$	BSZ0501NSI *2	Core	DMR51W/P61



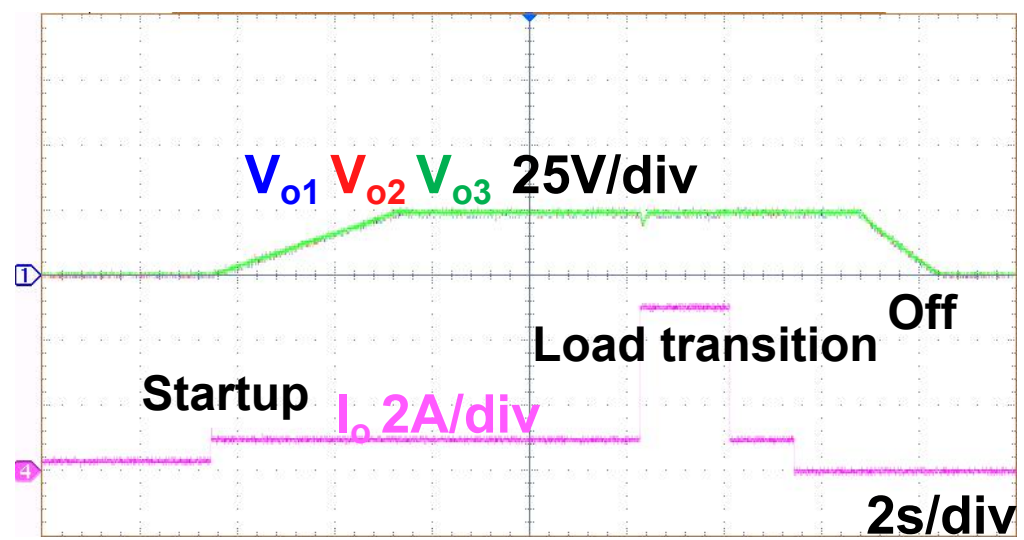
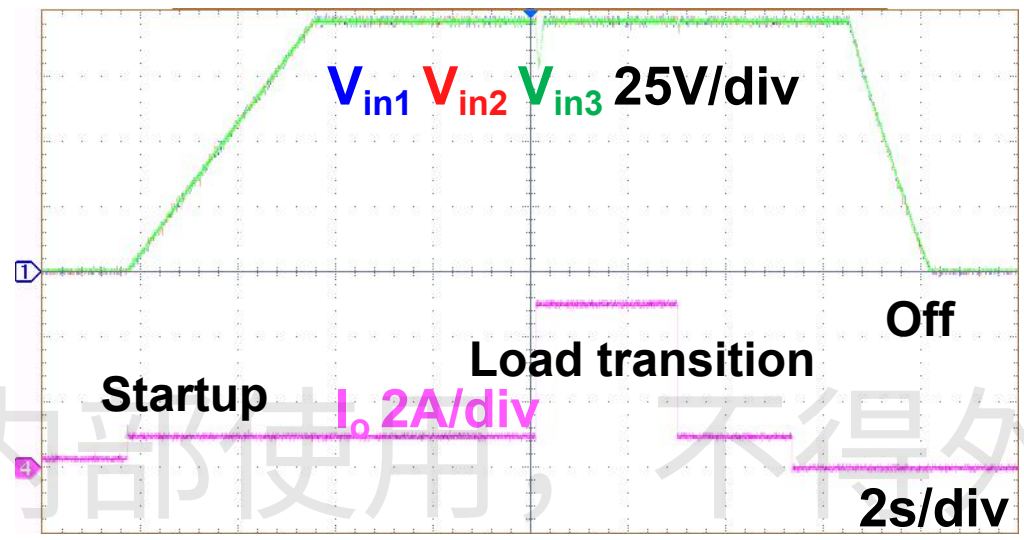
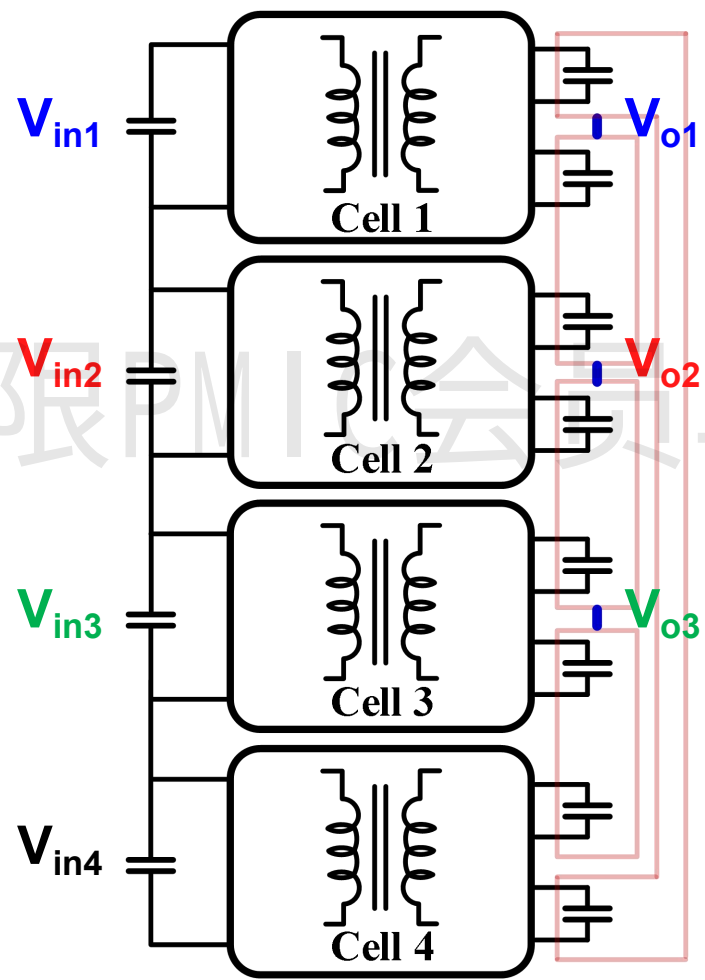
Primary voltage and current waveforms



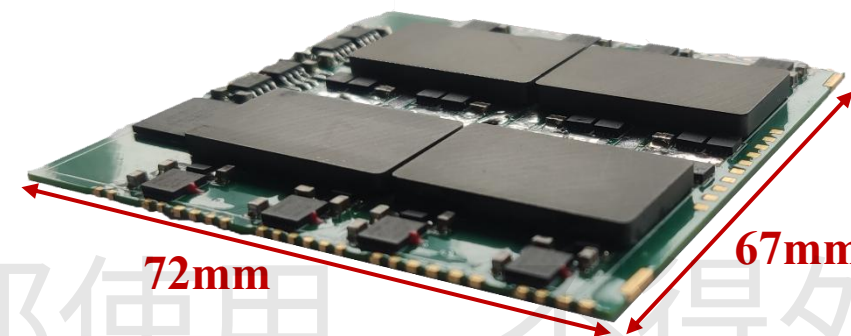
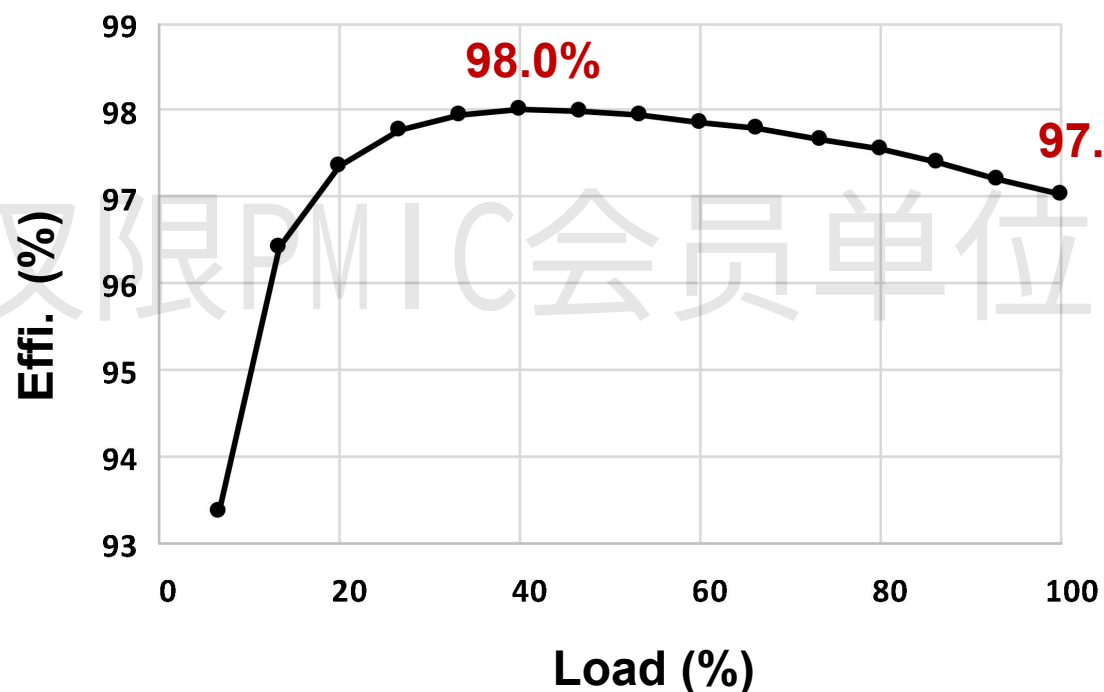
Input and Outputs voltage sharing capability at dynamic



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Efficiency and Power density of the Prototype

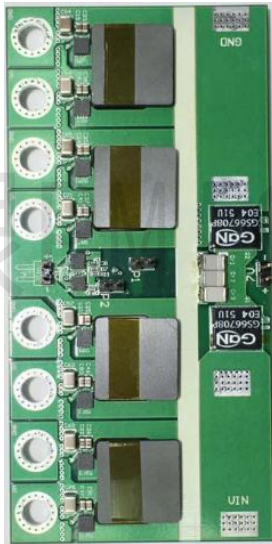


Input: 380Vdc
Output: 48Vdc – 1800W
Frequency: 1MHz
Peak efficiency: **98.0%**
Power density: **900W/in³**

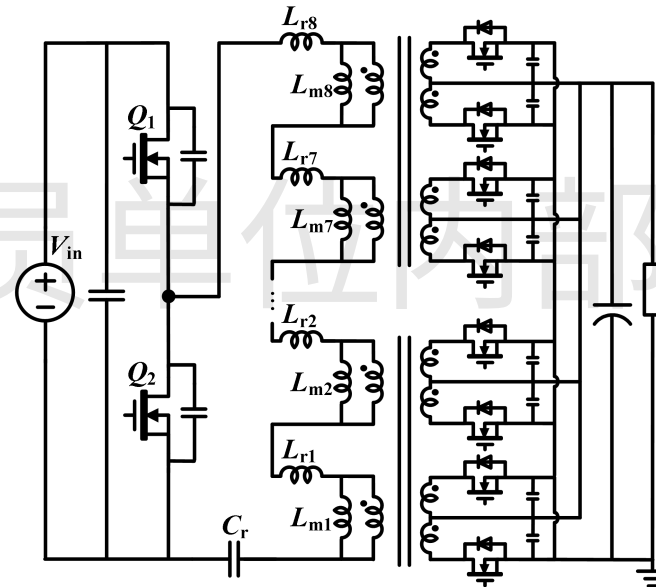
1. Introduction of power supply architecture of internet datacenter and popular high density high efficiency applications.
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 - 3.3 High Density Transformer Design for 48V MHz DC-DC converter
4. Conclusions



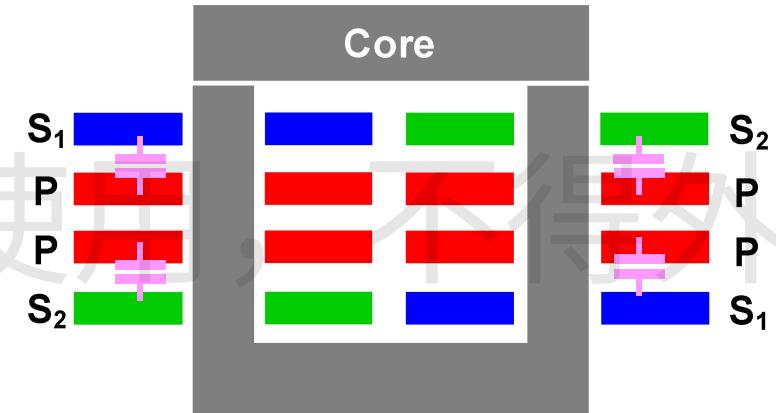
□ Large Inter-winding capacitance



97% 700W/in³



4-core matrix transformer



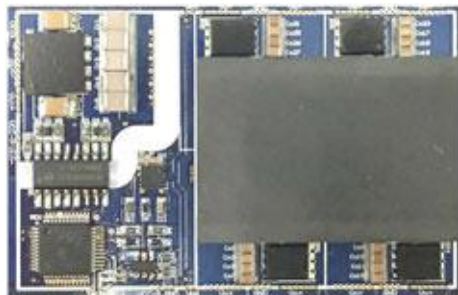
- ◆ small termination loss
- ◆ slight proximity effect
- ◆ **serious CM noise**

[1] M. Mu and F. C. Lee, "Design and Optimization of a 380–12 V High-Frequency, High-Current LLC Converter With GaN Devices and Planar Matrix Transformers," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 854-862, Sept. 2016.

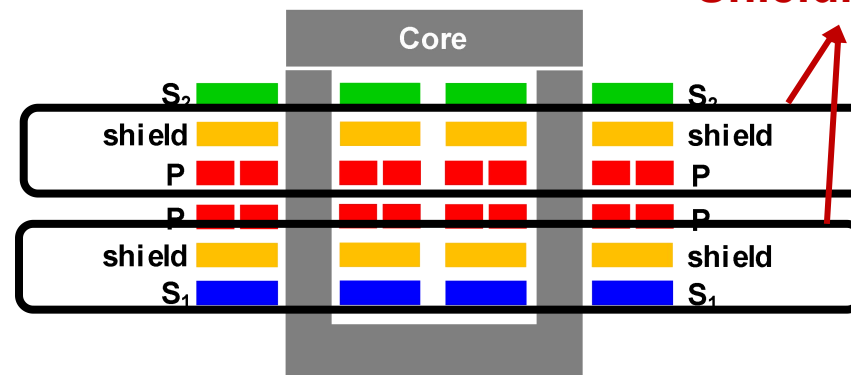


Matrix transformer with shielding layers

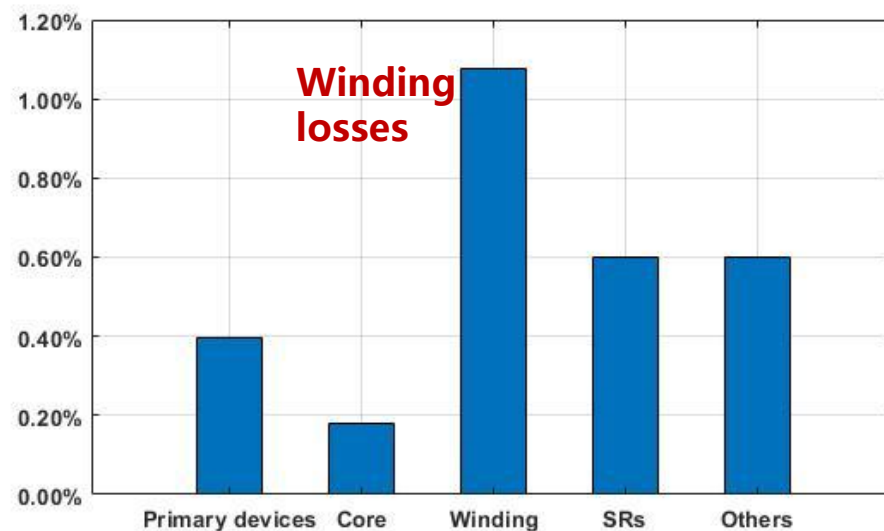
Matrix transformer with shielding



97.7% 900W/in³

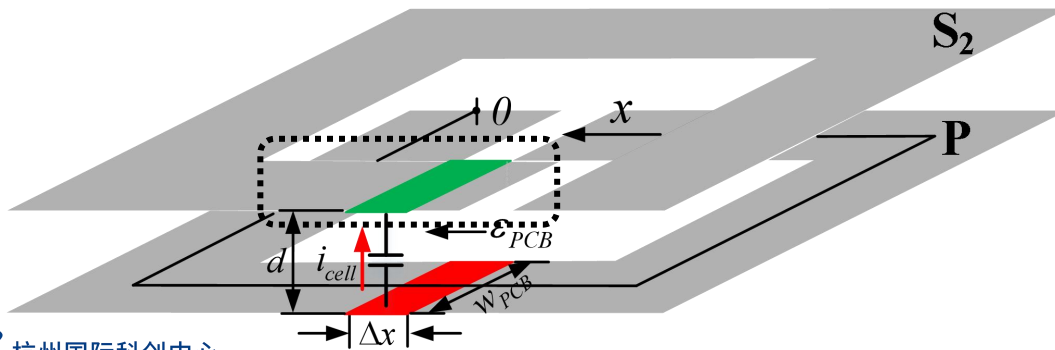
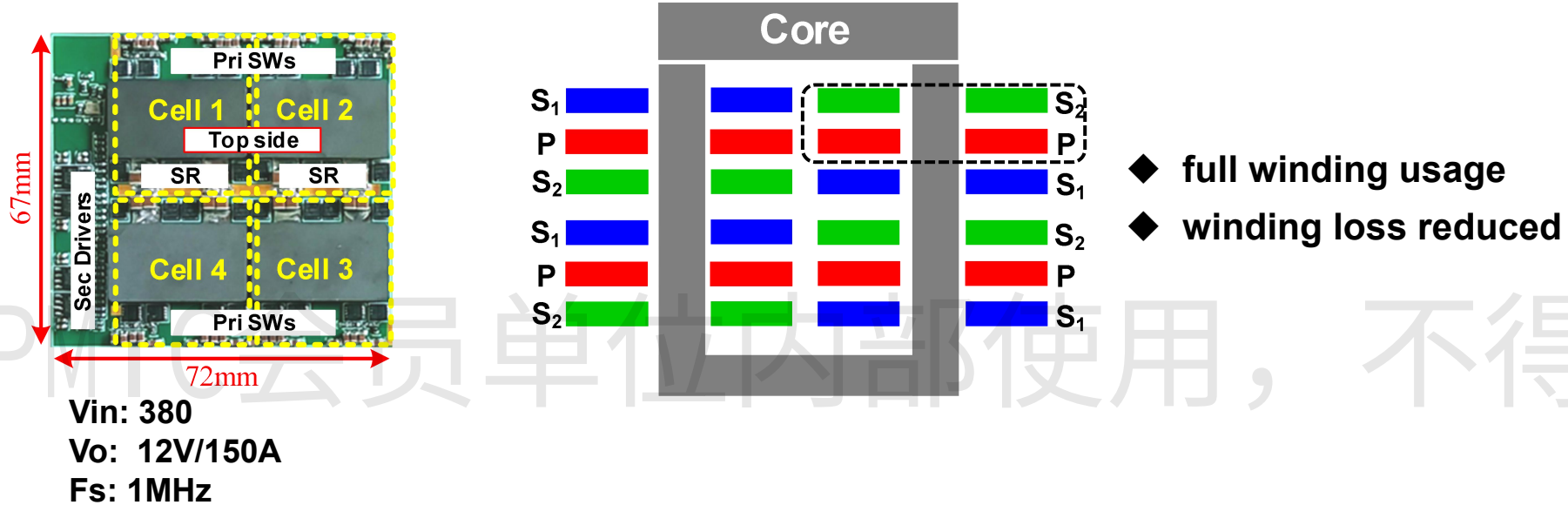


- ◆ small CM noise
- ◆ low winding usage



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6-layers matrix transformer



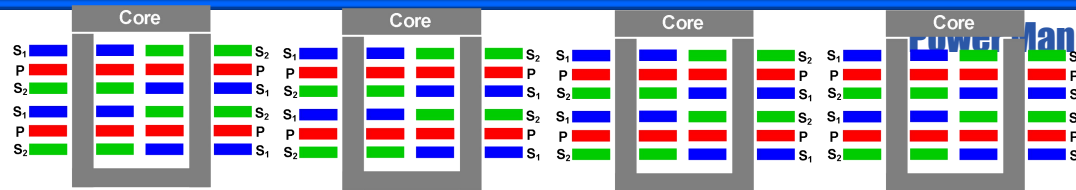
L : the length of winding

C: the physical layer-to-layer capacitance

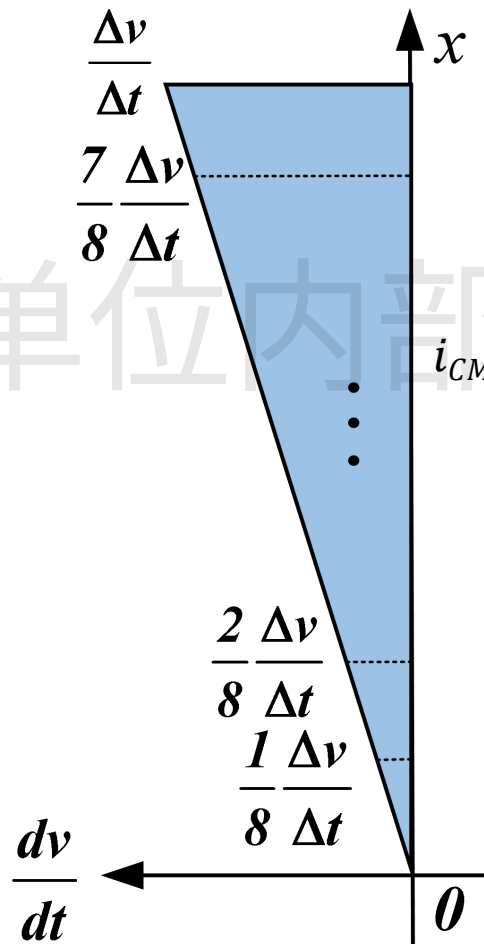
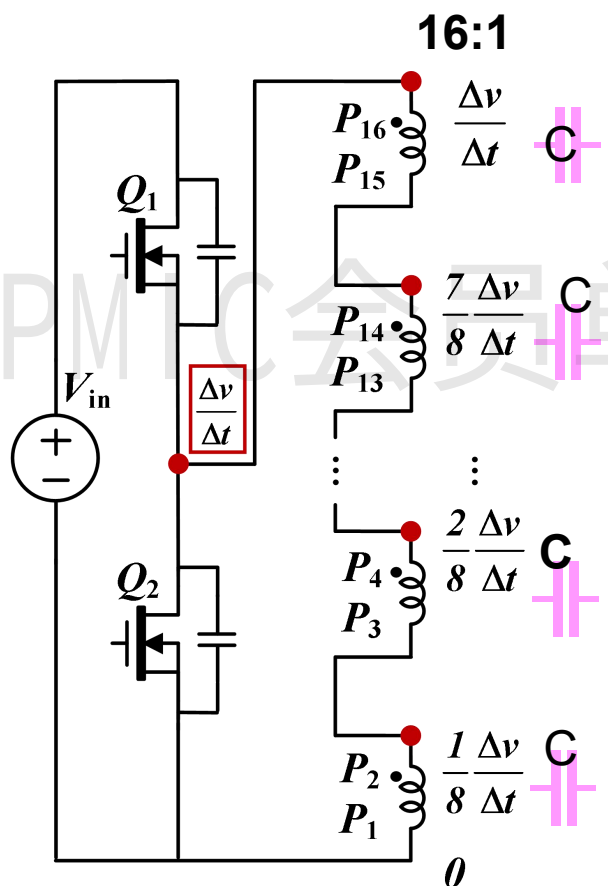
$$C_{cell} = \frac{\varepsilon_0 \cdot \varepsilon_{PCB} \cdot W_{PCB} \cdot \Delta x}{d} = \frac{C}{L} \Delta x$$

Common Current in Conventional High Voltage Scheme

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Conventional scheme



Total CM current

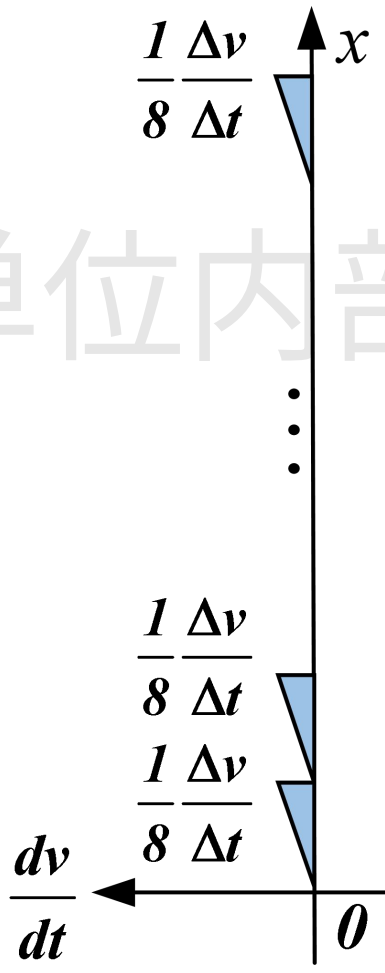
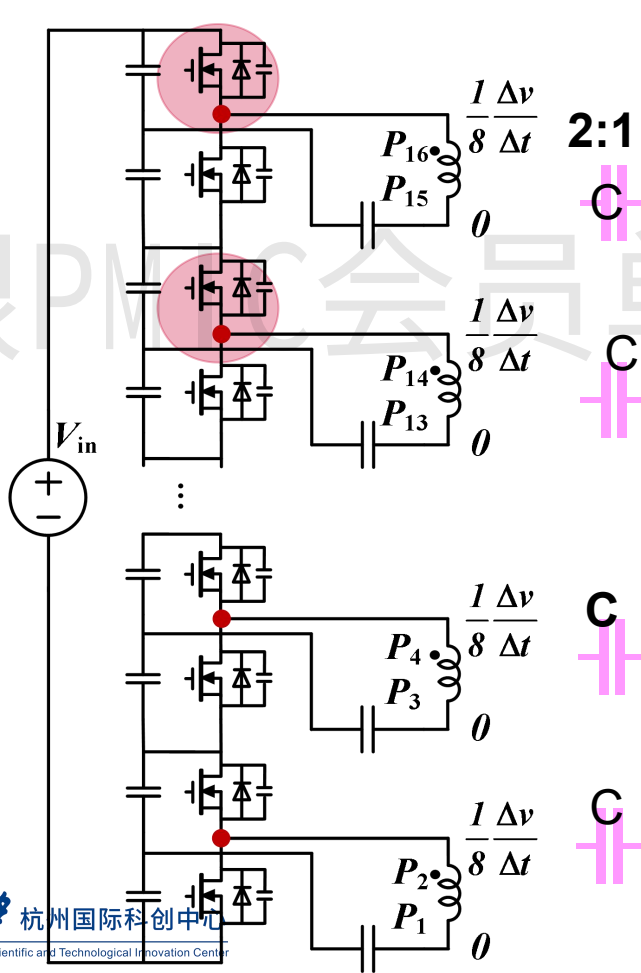
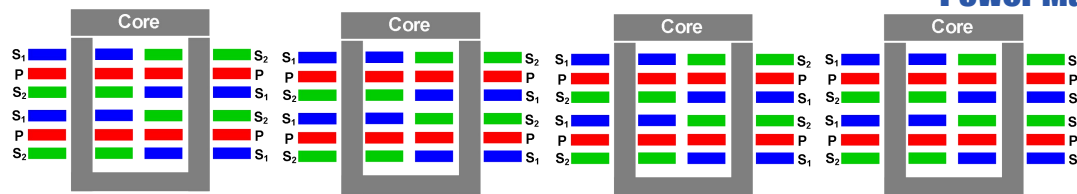
$$i_{CM} = \left(2C \cdot \frac{0 + \frac{1}{8} \frac{\Delta v}{\Delta t}}{2} + 2C \cdot \frac{\frac{1}{8} \frac{\Delta v}{\Delta t} + \frac{2}{8} \frac{\Delta v}{\Delta t}}{2} + \dots + 2C \cdot \frac{\frac{7}{8} \frac{\Delta v}{\Delta t} + \frac{\Delta v}{\Delta t}}{2} \right) \cdot 2$$

$$= 16C \cdot \frac{\Delta v}{\Delta t}$$



i_{CM} in input-series scheme

Input-series scheme



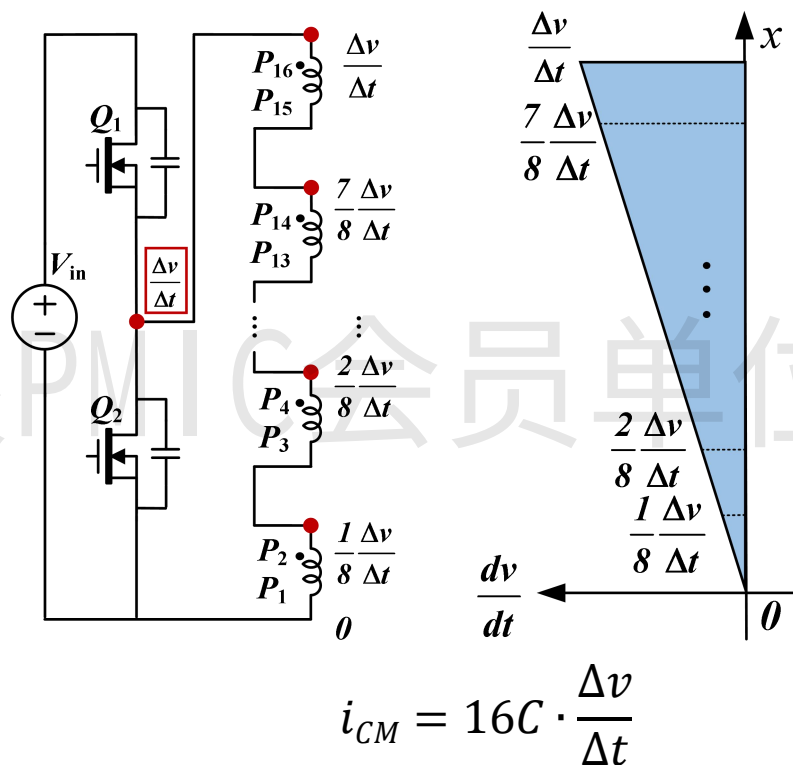
Total CM current

$$i_{CM}' = 2C \cdot \frac{0 + \frac{1}{8} \frac{\Delta v}{\Delta t}}{2} \cdot 8 \cdot 2$$

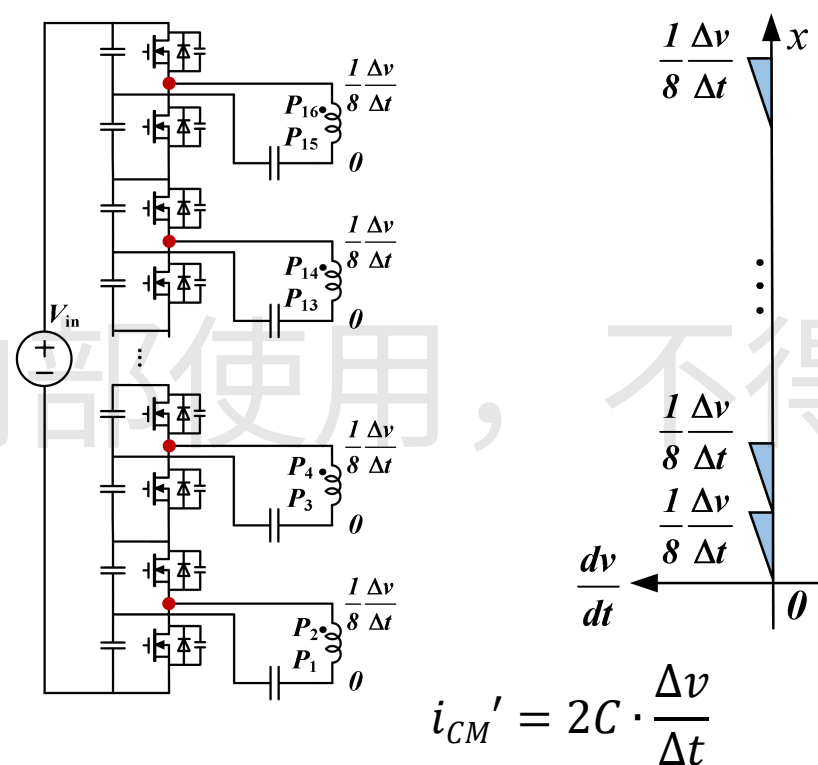
$$= 2C \cdot \frac{\Delta v}{\Delta t}$$

Single switch VS. input-series

single high switch scheme



Multi-switch Input-series scheme

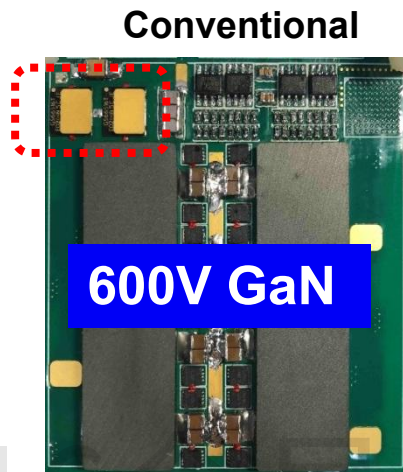


$$i_{CM}' = \frac{1}{8} i_{CM}$$

$$20 \log \left(\frac{i_{CM}'}{i_{CM}} \right) = -18 \text{ dB}$$

CM current has 18dB reduction

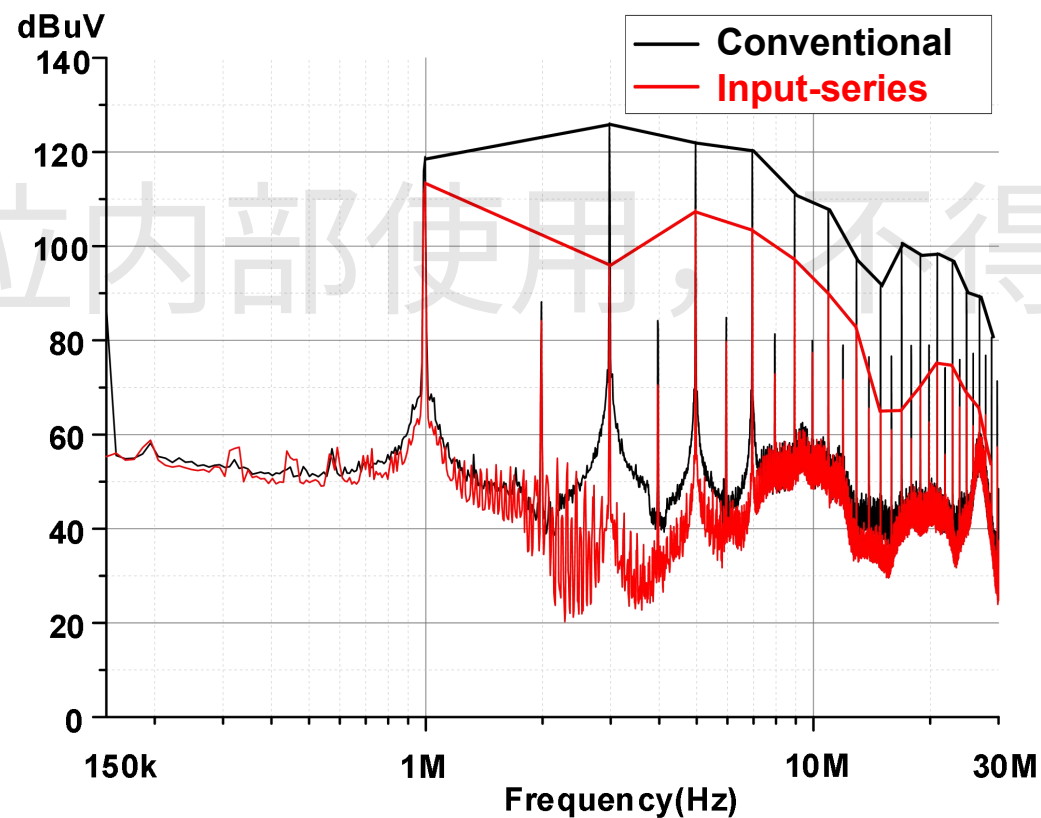
Experimental Comparison



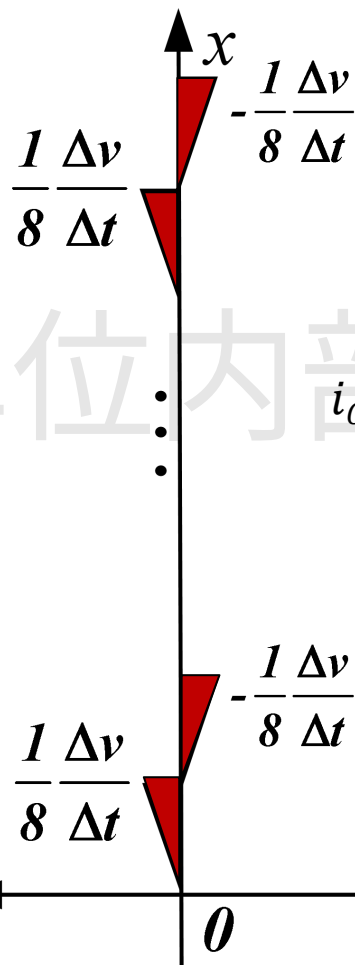
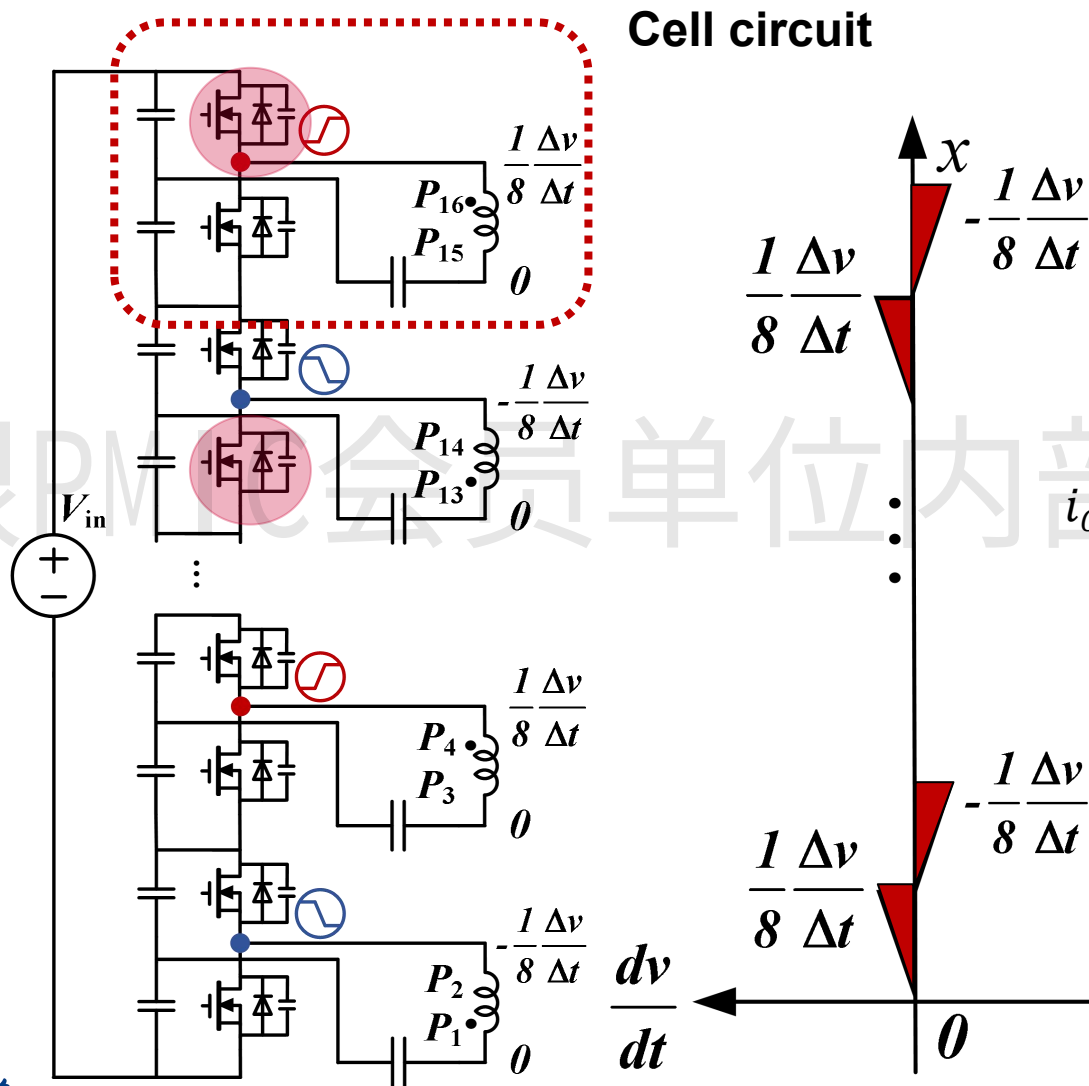
Identical PCB winding structure



Average **20dB** reduction
within test frequency range



Complementary control scheme in Cell



Total CM current

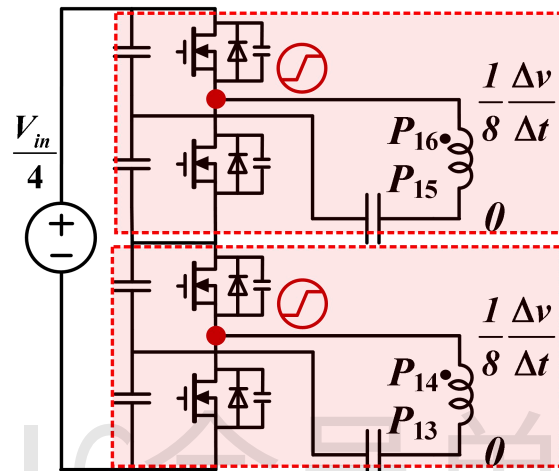
$$i_{CM'} = \left(2C \cdot \frac{0 + \frac{1}{8} \frac{\Delta v}{\Delta t}}{2} + 2C \cdot \frac{0 - \frac{1}{8} \frac{\Delta v}{\Delta t}}{2} \right) \cdot 4$$

?

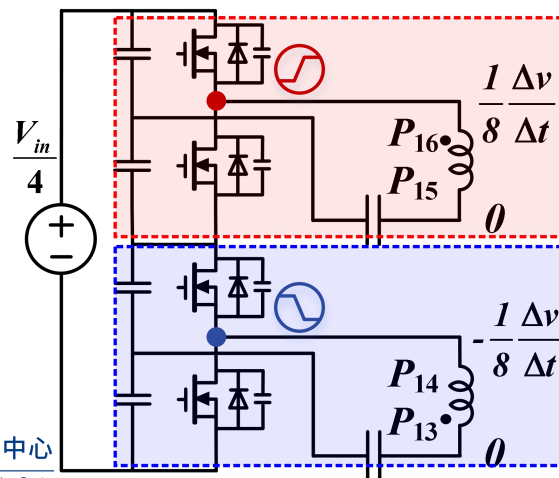
0

Cancellation?

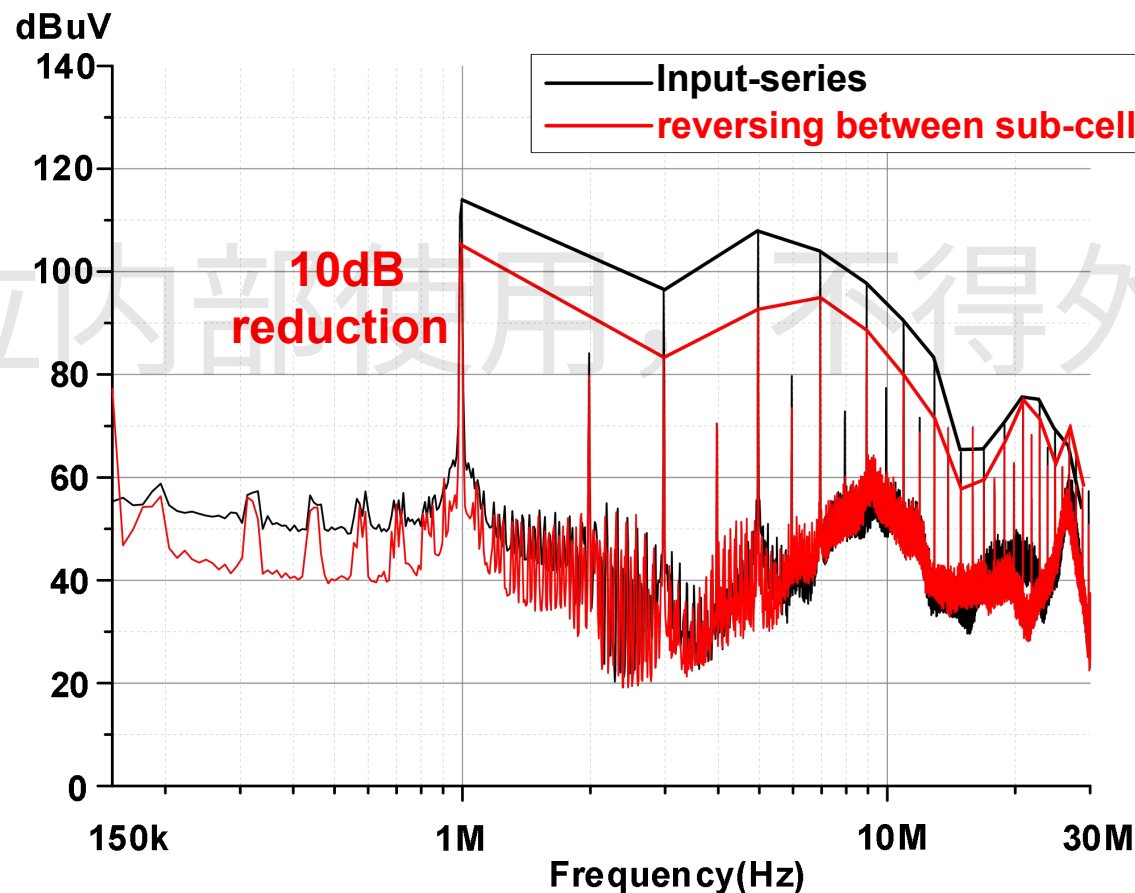
Input-series



interleave within each cell

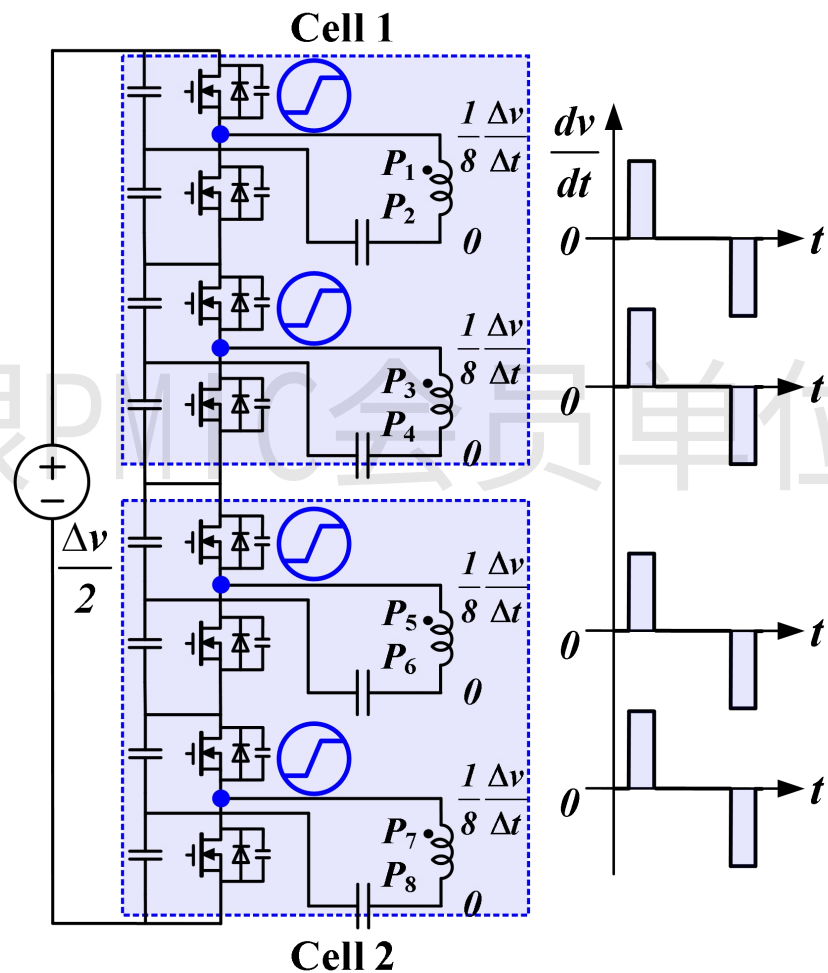


Asymmetry traces in cell PCB
transformer deteriorate the cancellation

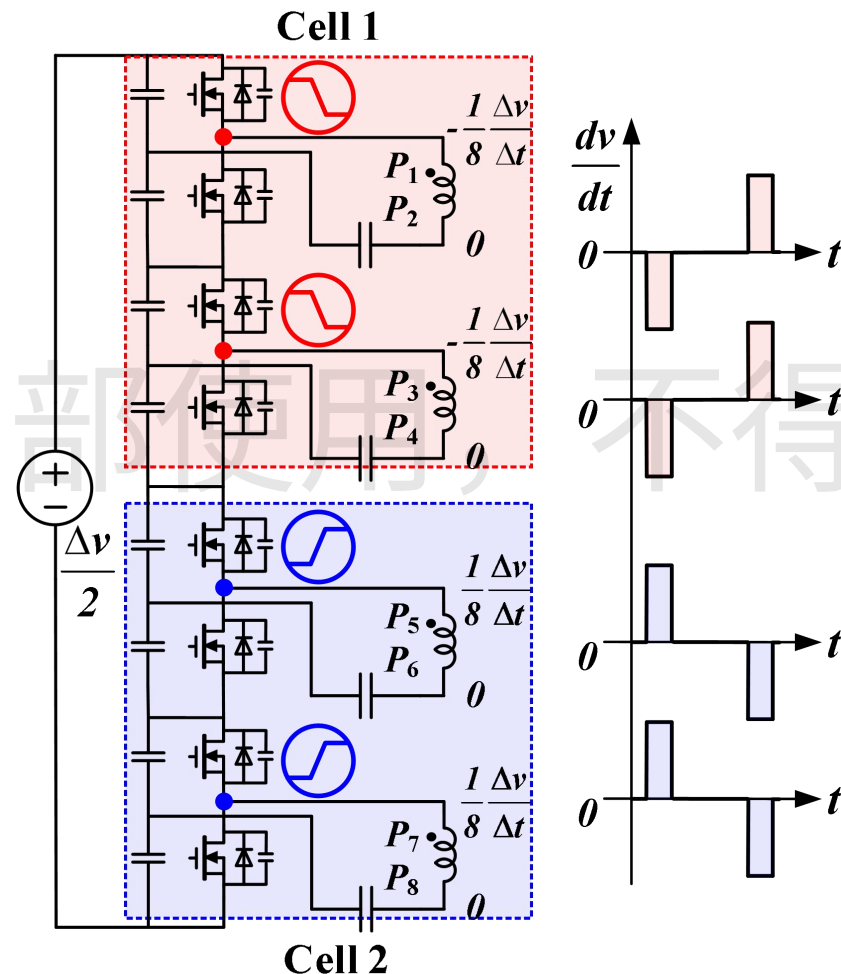


Optimization of control scheme (2)

Input series scheme

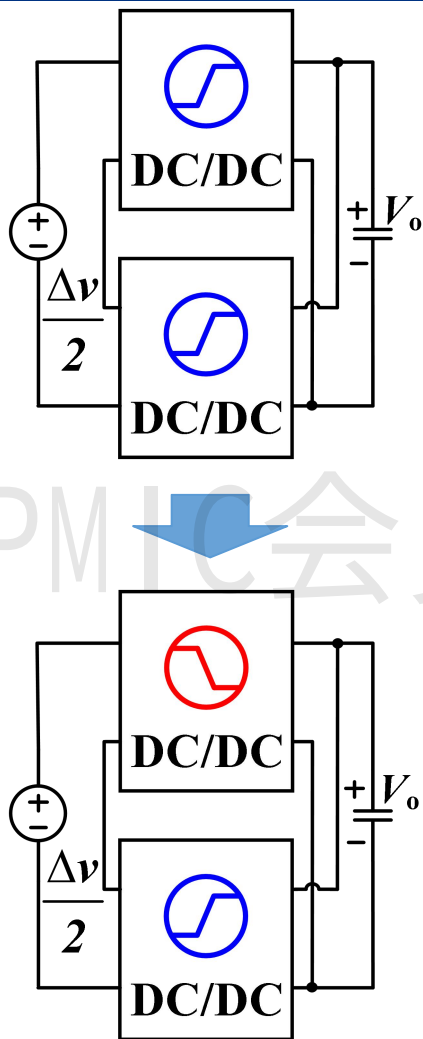


interleave between cells

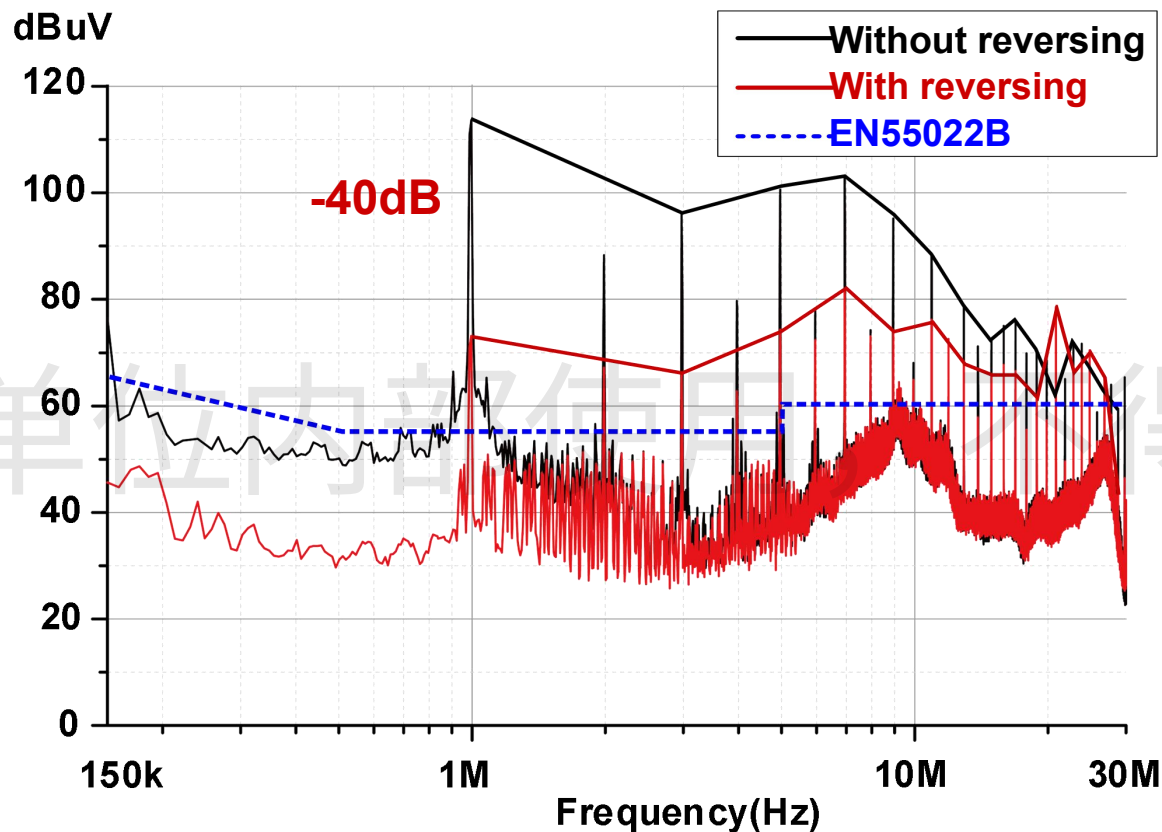


cancellation effect on CM noise

Experimental verifications



Symmetry PCB transformer of cells

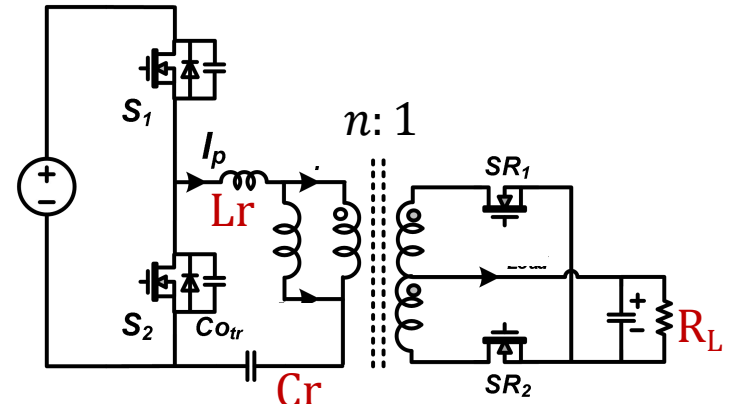


40dB reduction
at fundamental frequency

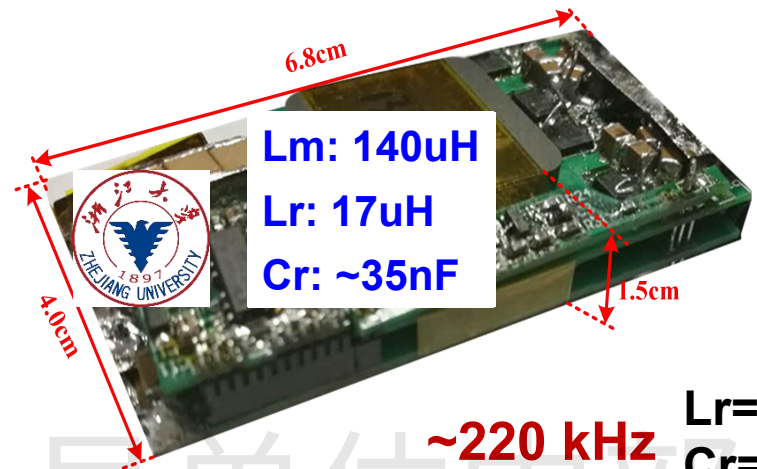
1. Introduction of power supply architecture of internet datacenter and popular high density high efficiency applications.
2. Topology for MHz high efficiency 380V-48V/12V power conversion
 - 2.1 Unregulated DC-DC (DCX) techniques
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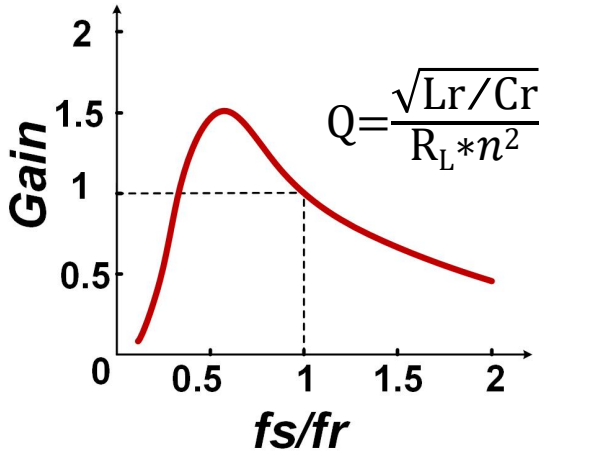
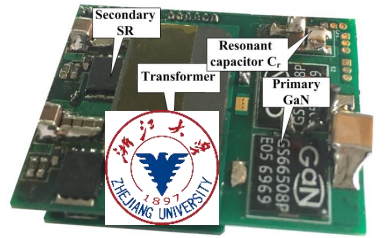
Frequency Modulation Control MHz LLC Resonant Converter



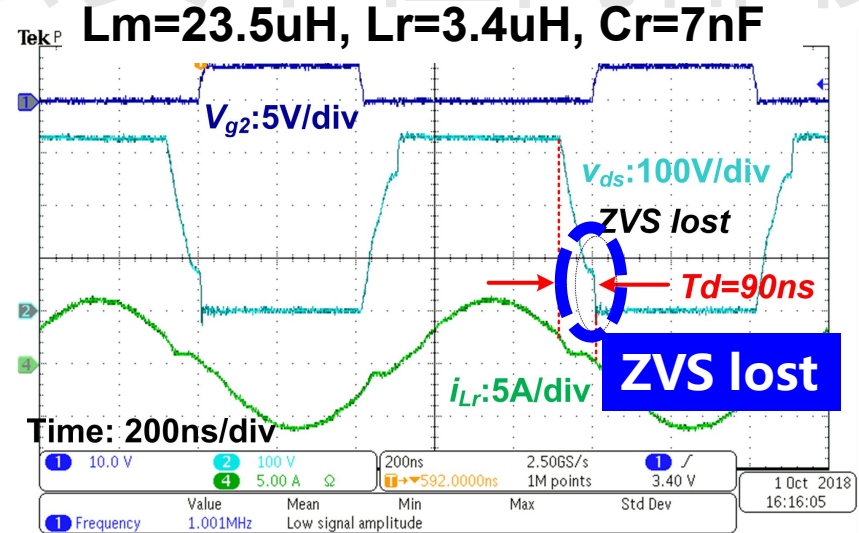
Conventional LLC Resonant half-bridge Converter



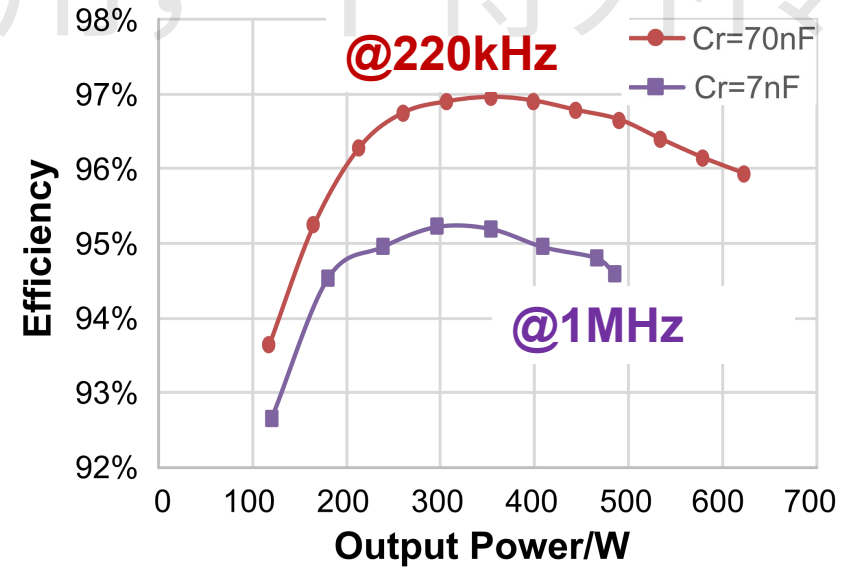
360-400V
input **12V/62A**
output **750W**
The Same Q



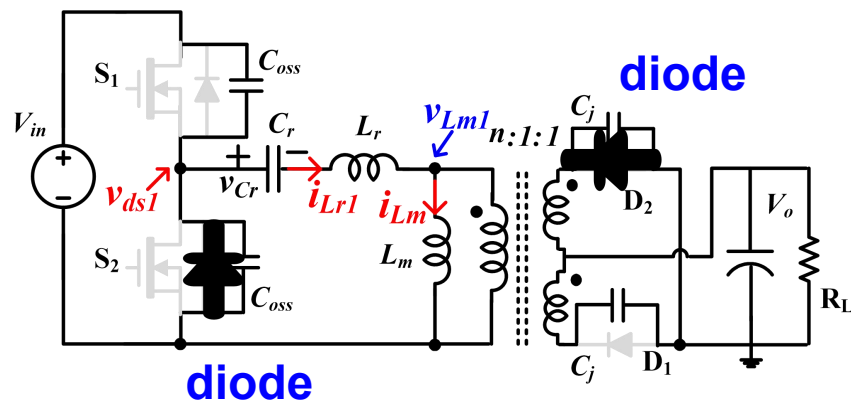
Voltage Gain vs fs/fr



@ 500W

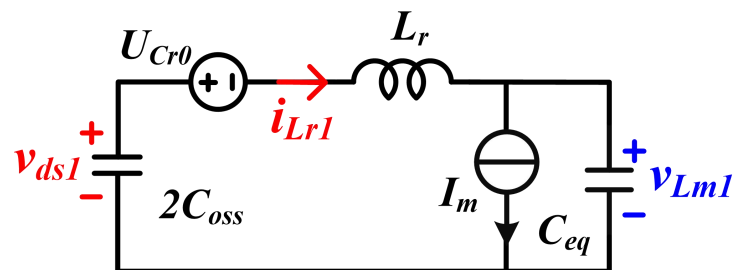


MHz Frequency LLC Leads to ZVS Difficulty at Heavy Load

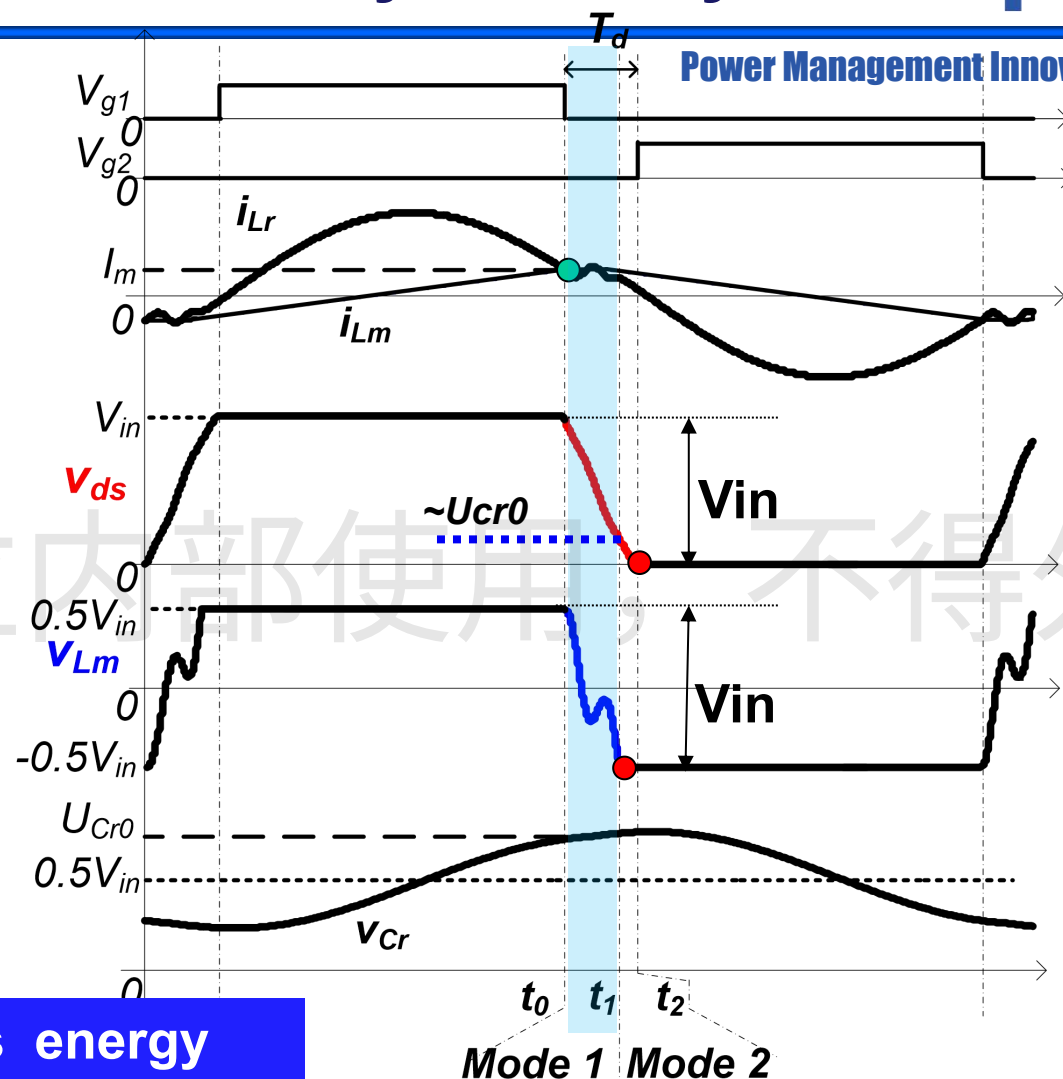


$$L_m \gg L_r$$

$$C_r \gg C_{oss} \text{ \& } C_{eq} \quad C_{eq} = 2C_j/n^2$$



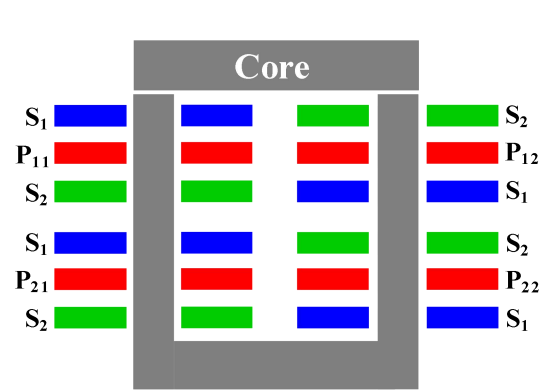
- ☹ Lower L_r (high f_s) leads to less energy
- ☹ High U_{Cr0} results in Difficulty of ZVS



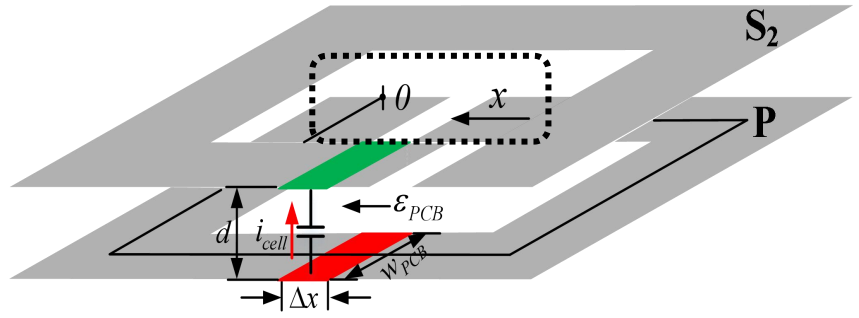
?

Inter-capacitance Sinking Magnetizing Current Deteriorate ZVS at MHz

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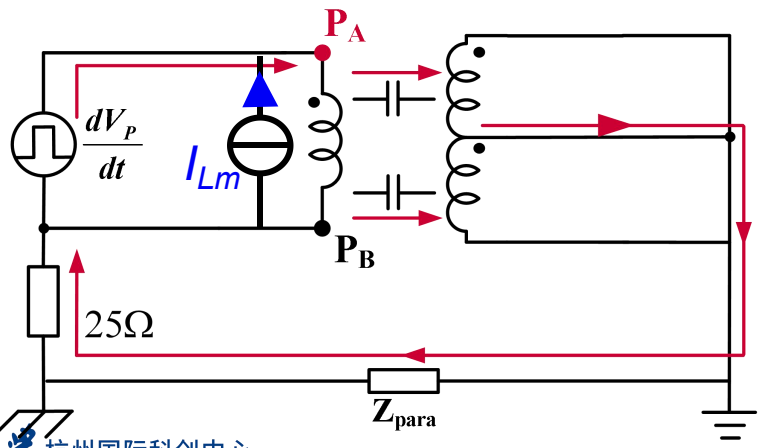
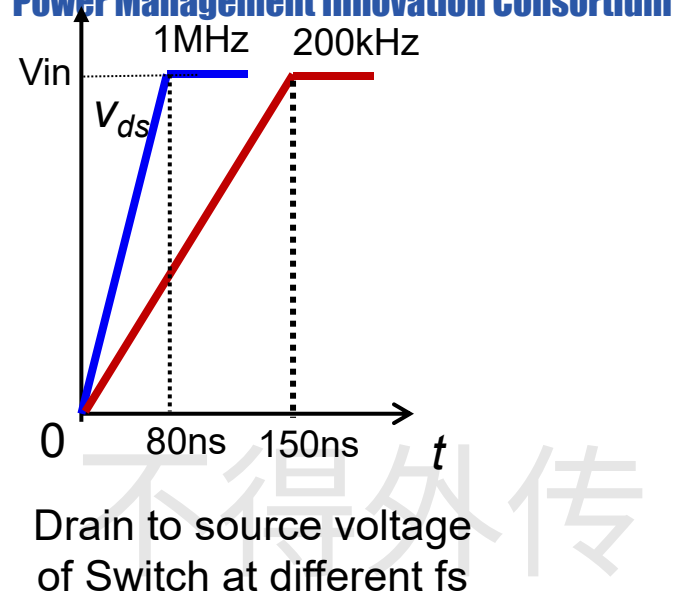


Common Mode current between PCB windings



L: the length of winding
C: the physical layer-to-layer capacitance

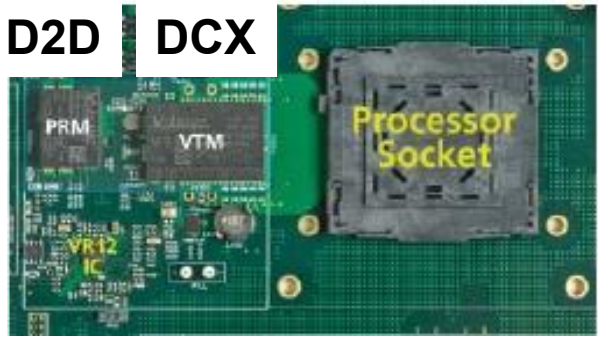
$$C_{cell} = \frac{\epsilon_0 \cdot \epsilon_{PCB} \cdot W_{PCB} \cdot \Delta x}{d} = \frac{C}{L} \Delta x$$



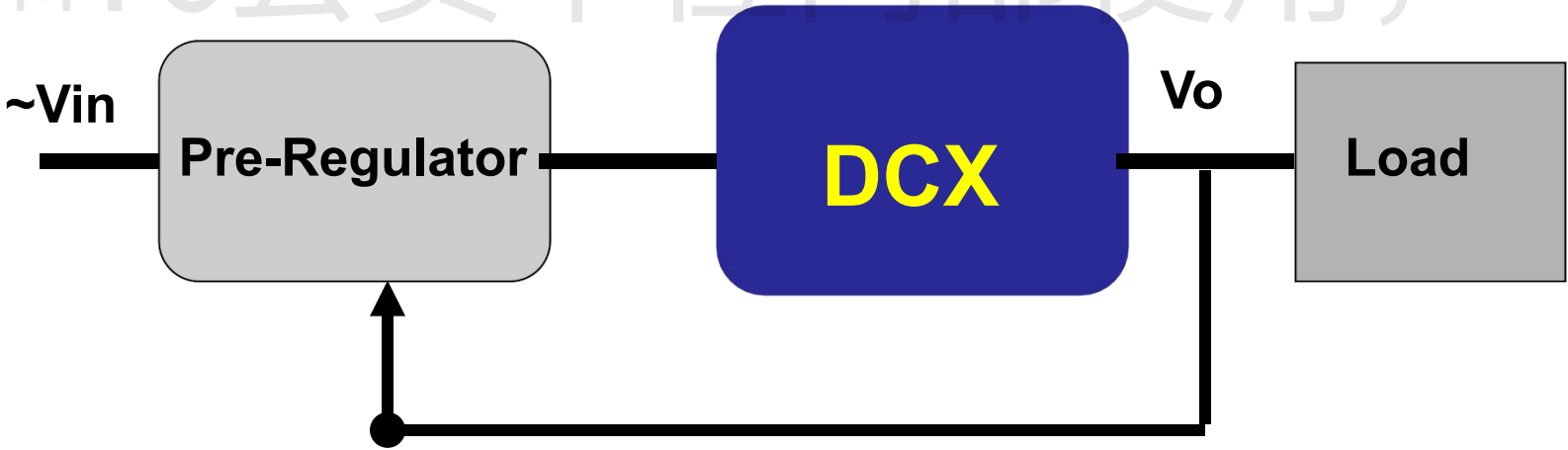
PCB inter-winding capacitance sinks magnetizing current much high at MHz because of the common mode current

Solution 1: Two stage DC-DC Scheme achieving Tight Regulation

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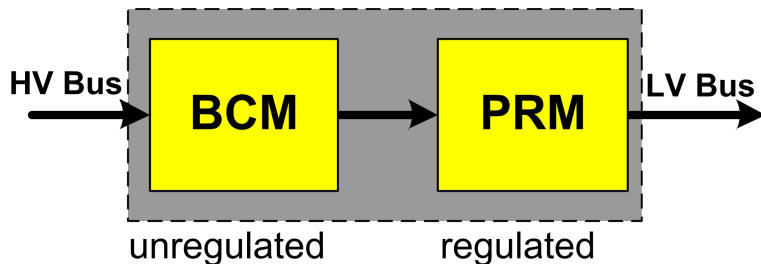
Two stage: **DC-DC**+**DCX**



Block of DC-DC system

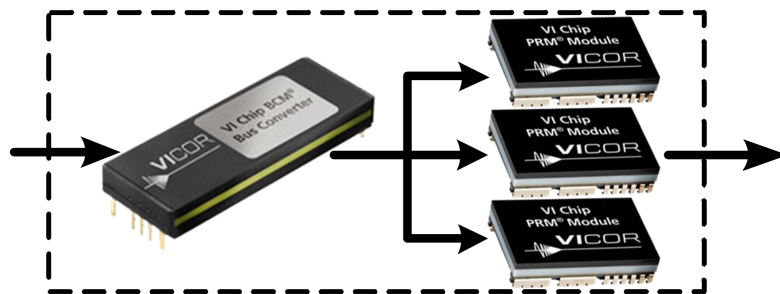
Solution 1: Efficiency Sacrifice of Two stage Scheme

□ Two-stage for on-board power module



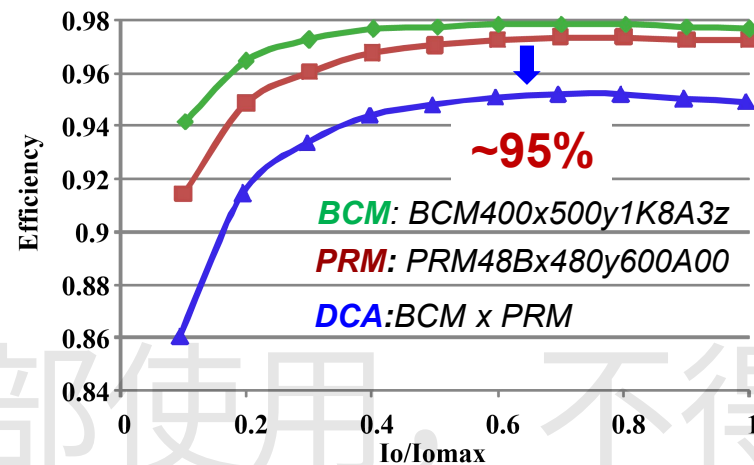
DCX
unregulated

Non-Isolated DC-DC
regulated



98%, 2735W/in³
~1MHz

97.6%, 2072W/in³
~1MHz

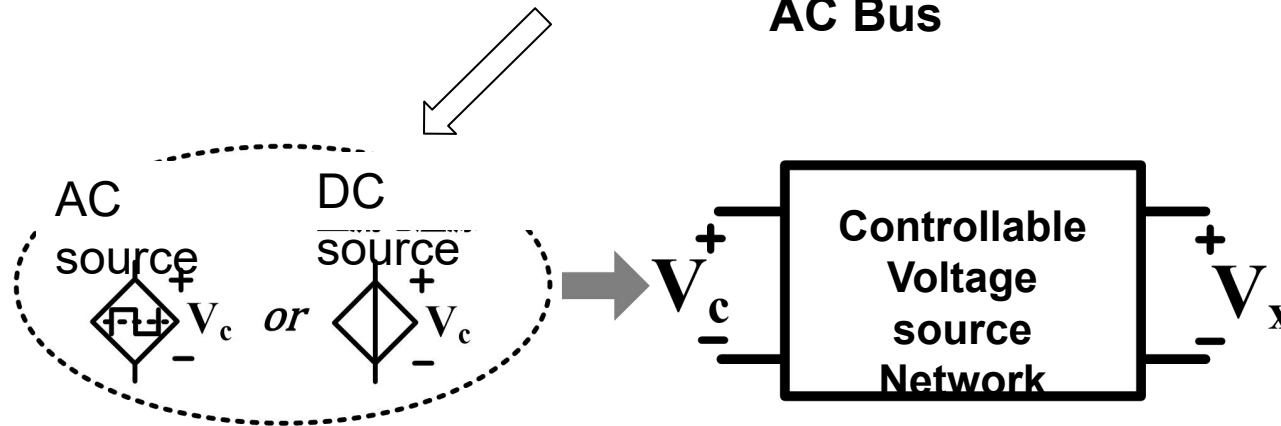
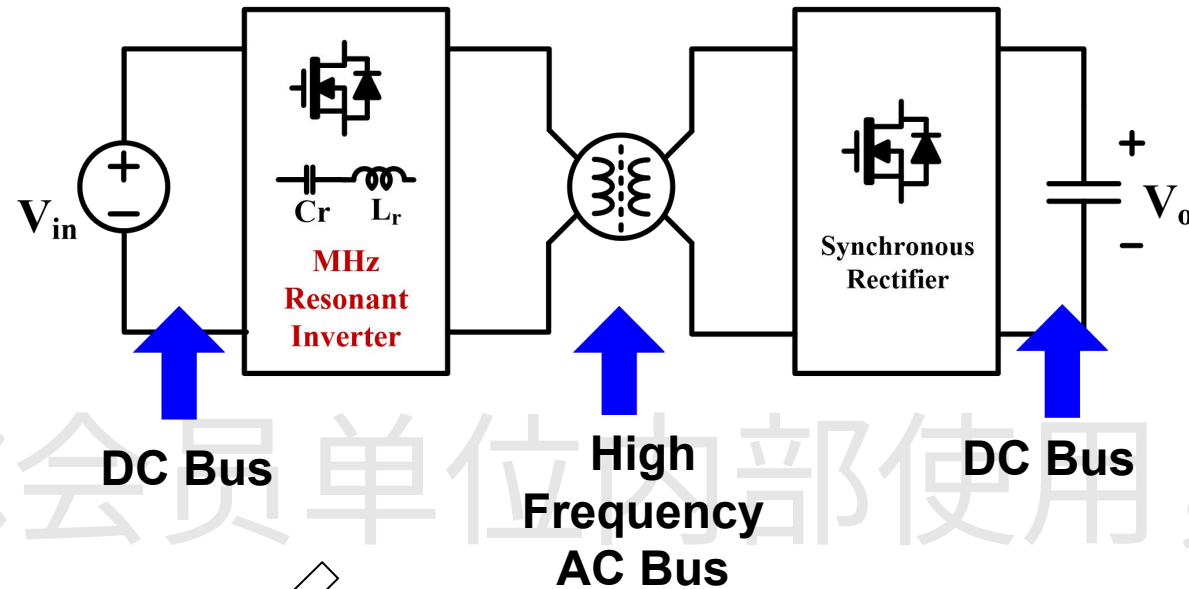


Efficiency decrease

One stage ?

Source: BCM400x500y1K8A3z
PRM48Bx480y600A00

Proposed Solution: Series Voltage Regulation Scheme



Two ports network :

V_c : in series

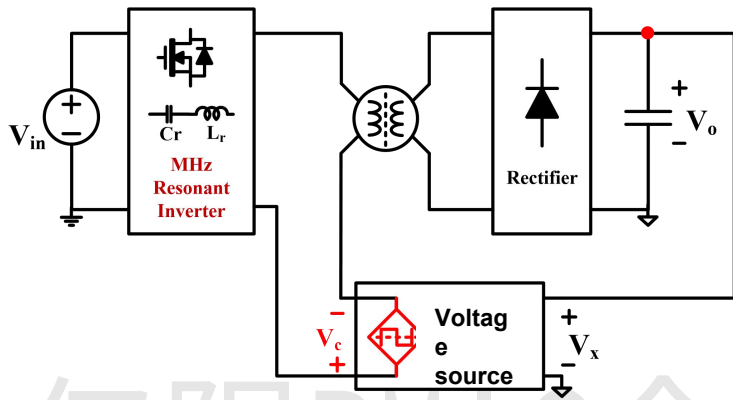
V_x : paralleling

Inserting a Controllable
Voltage Source

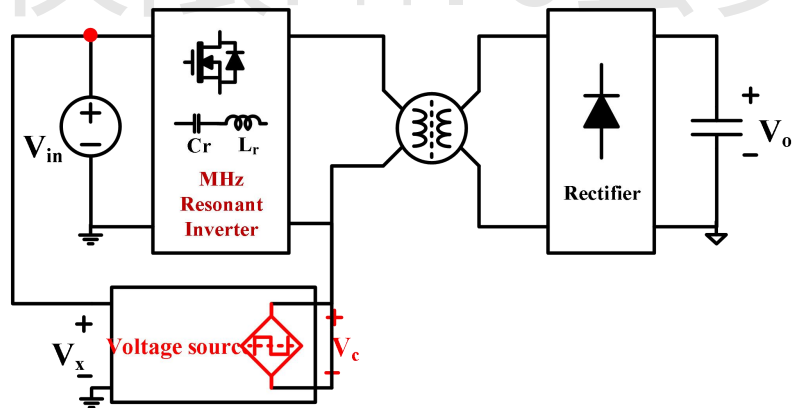
Three Types of Tight Regulated DCXs (RDCX)

□ concept of six RDCXs based on isolated DC/DC converters

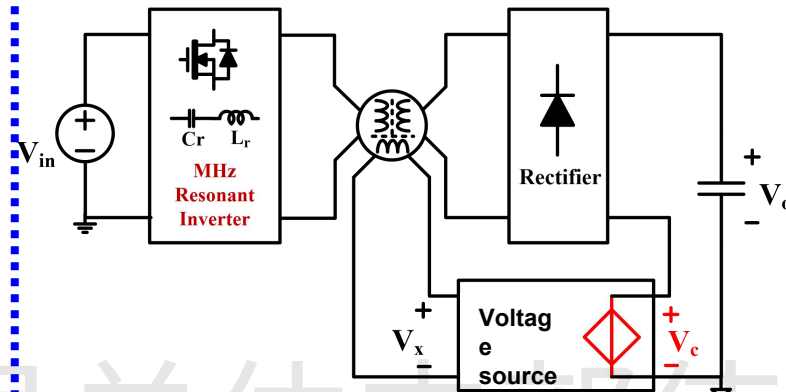
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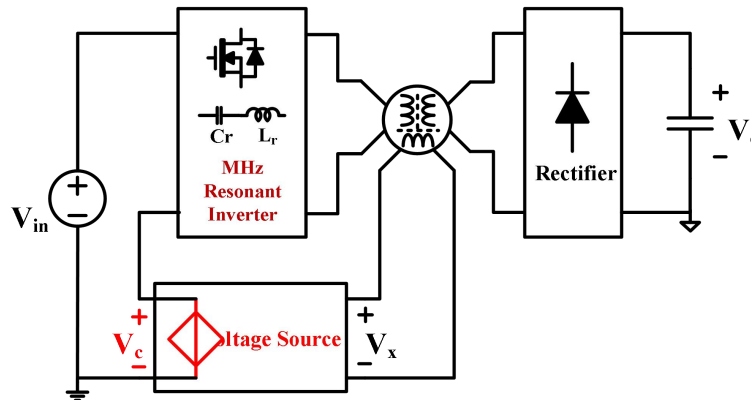
Two-port network



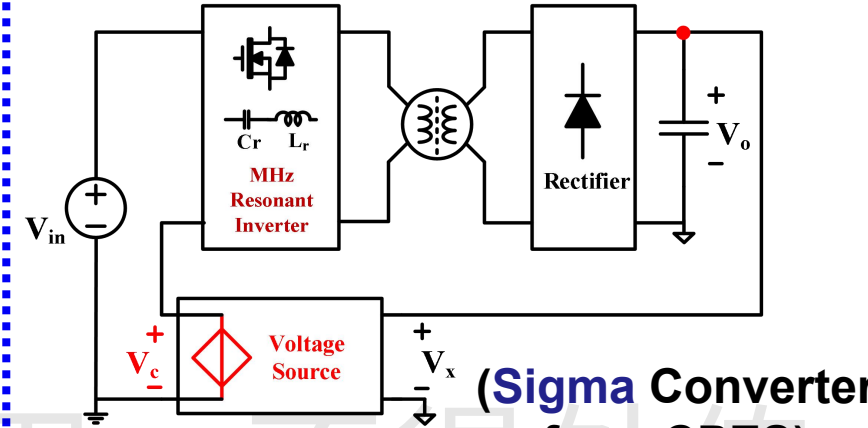
1. AC in series / DC parallel



Two-port network

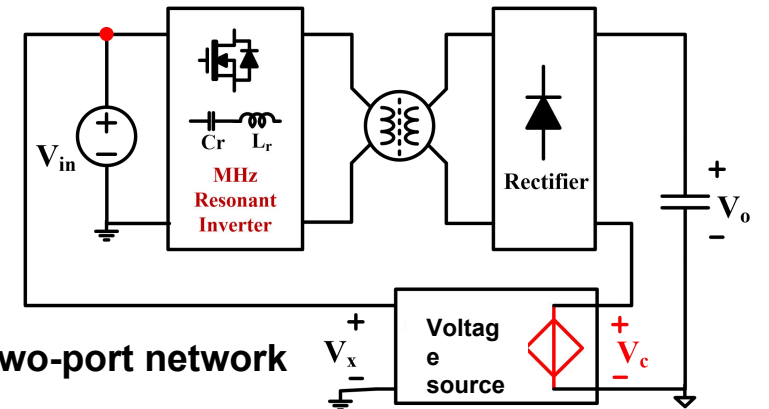


2. AC Parallel / DC in series

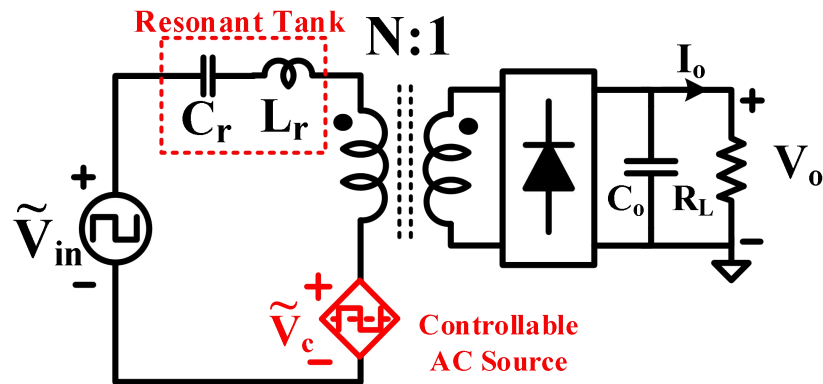


Two-port network

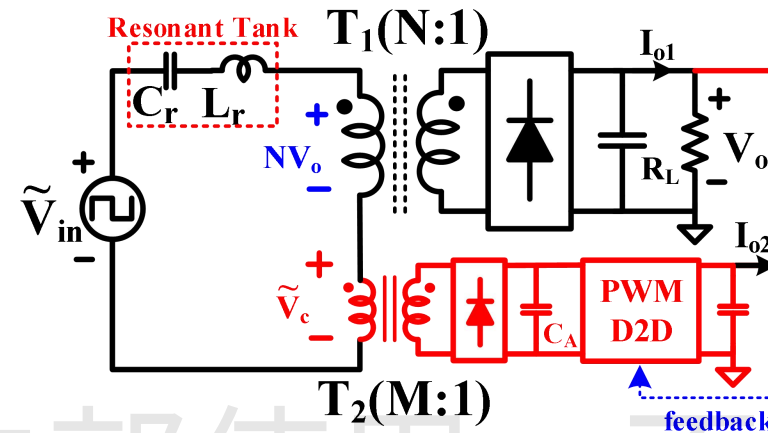
3. DC parallel / DC in series



RDCX- AC in series/DC in parallel – Example



Concept block



Implementation block

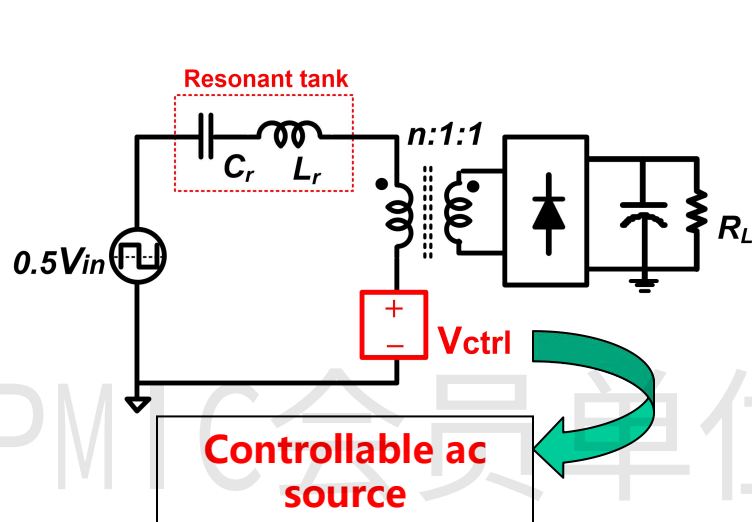


- Regulated V_o
- Partial power regulation
- Simple control
- Most power transferred to load by DCX

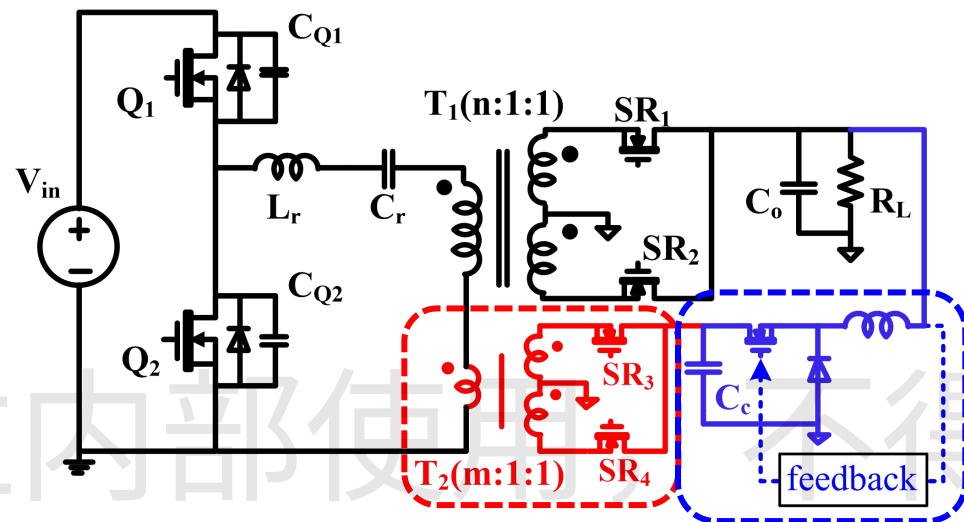
[1] X. Wu, H. Chen and Z. Qian, 1-MHz LLC Resonant DC Transformer (DCX) With Regulating Capability. IEEE Transactions on Industrial Electronics, 2016. 63(5): p. 2904-2912.



□ AC series/ DC parallel



☺ Tight regulated
(Quasi-single stage)



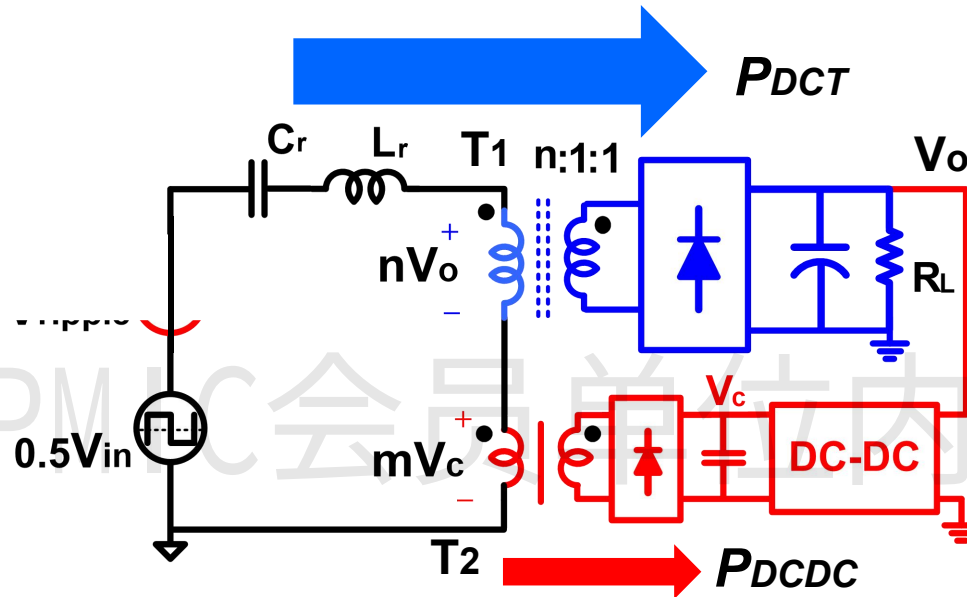
DCX

Buck

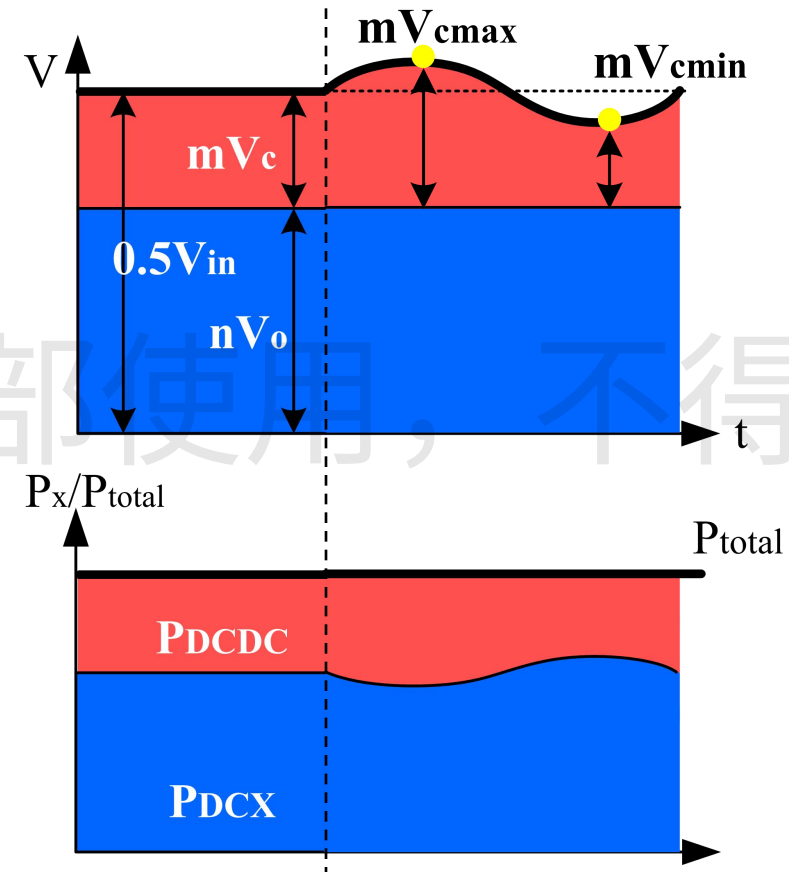
DCX & D2D non-synchronous

- ☺ Fixed switching frequency for resonant converter
- ☺ Simple PWM controller to regulated output
- ☺ High frequency, high efficiency
- ☺ The frequency of PWM is independent to DCX

RDCX- AC in series/DC parallel - Operating Principle



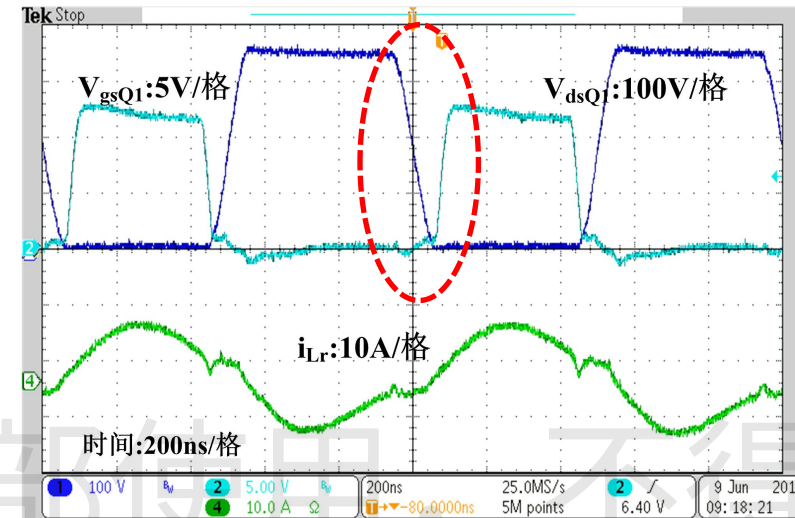
$$k = \frac{P_{dc/dc}}{P_{total}} = \frac{mV_c}{mV_c + nV_o}$$



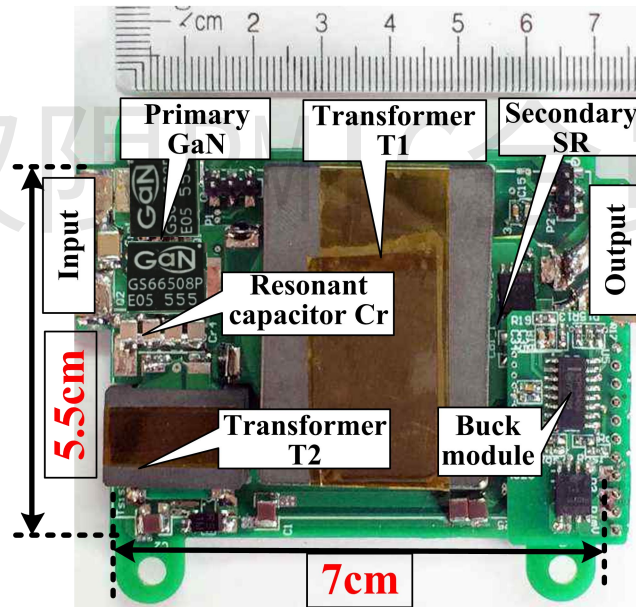
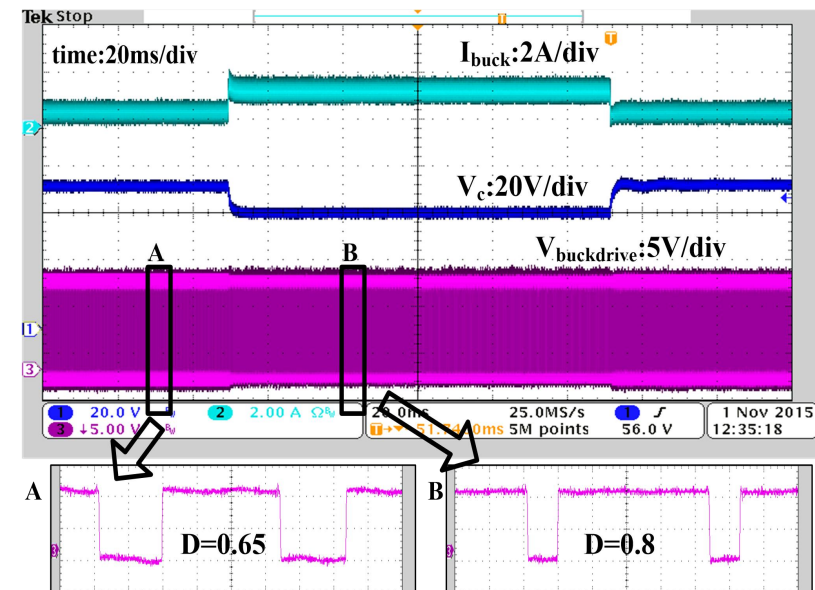
RDCX- AC in series/DC parallel – Example 1 380V-40V

V_{in} : 350-380VDC
 f_s : 1MHz
 V_o : 40V/25A (1kW)
 Density: $\sim 700W/in^3$

Primary voltage
with ZVS



Full load, $I_o=25A$

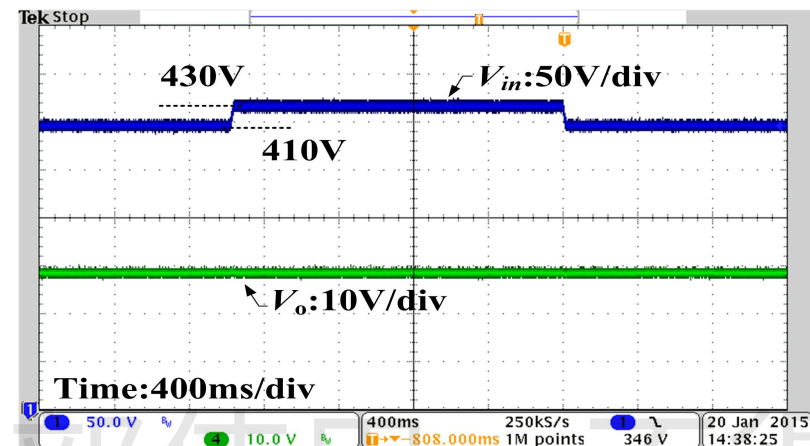
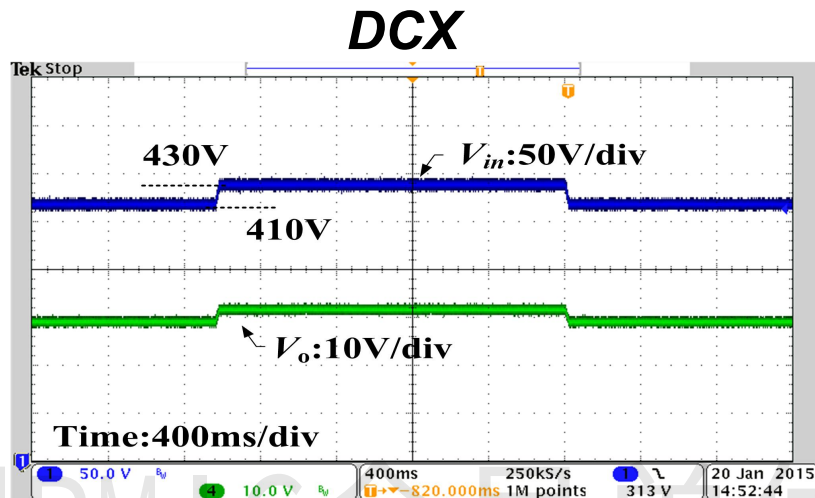


(year: 2015)

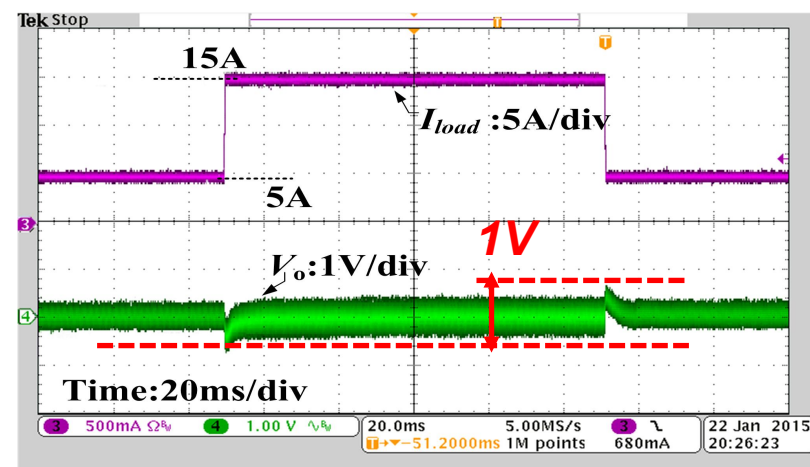
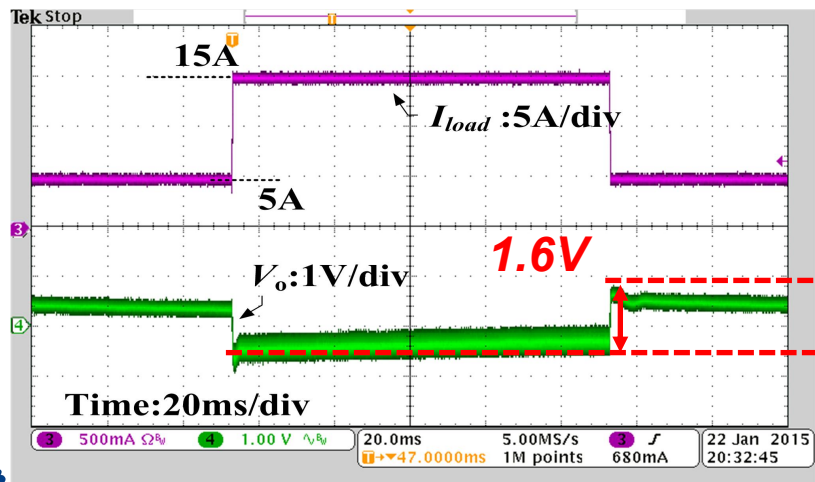
Prototype of RDCX



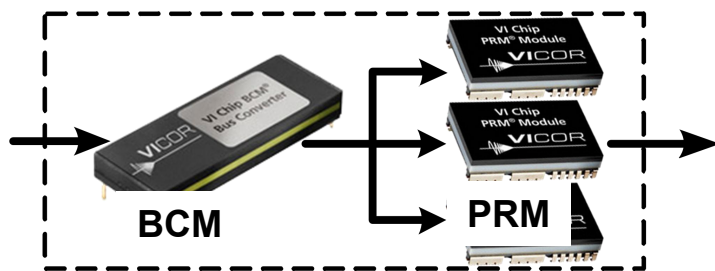
RDCX- AC in series/DC parallel - regulating capability



➤ V_o tight regulation with load jump

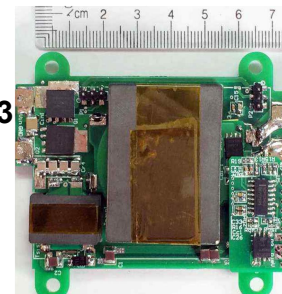


Comparison between RDCX and two stage

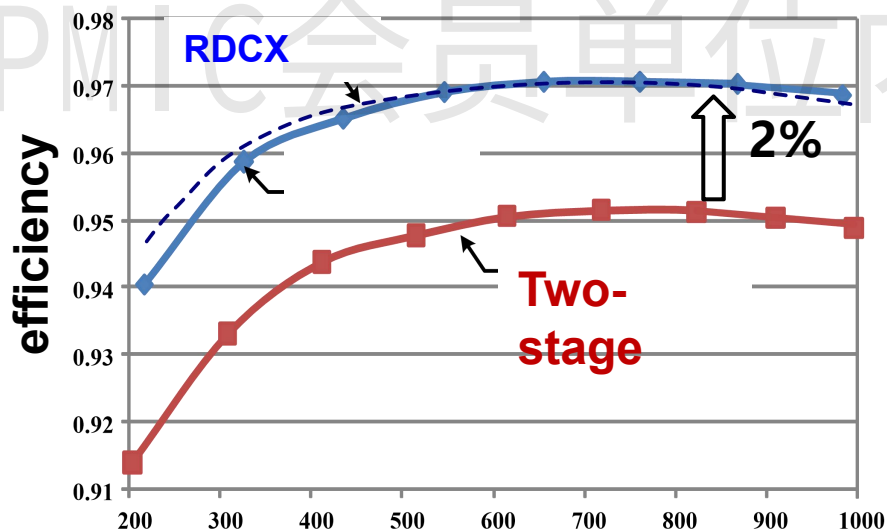


**Two-stage
scheme**

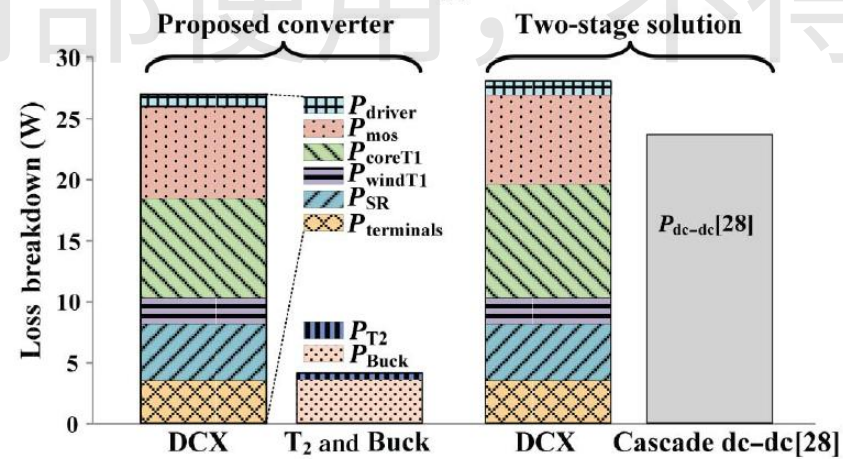
Density: $>700\text{W}/\text{in}^3$
~1MHz



**Proposed 380V-40V
RDCX**

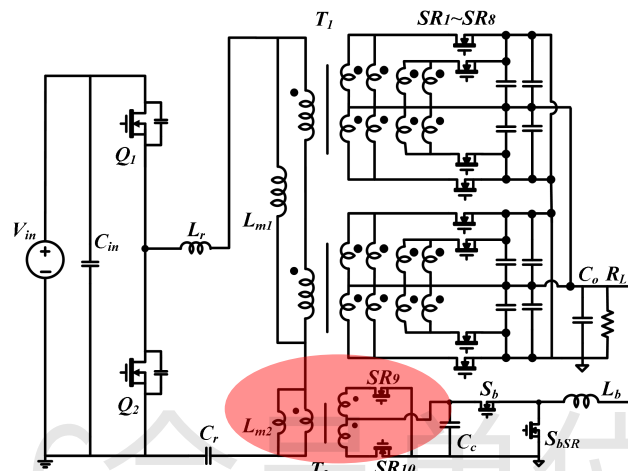


**(a) Measured efficiencies vs.
commercial two-stage products**



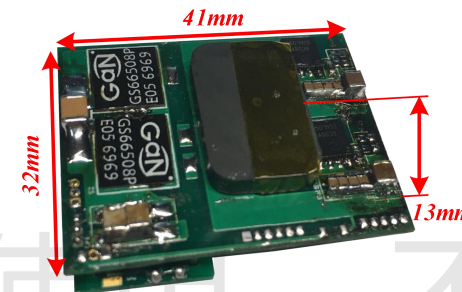
(b) Loss Breakdown

RDCX- AC in series/DC parallel Example 2: 380V-12V

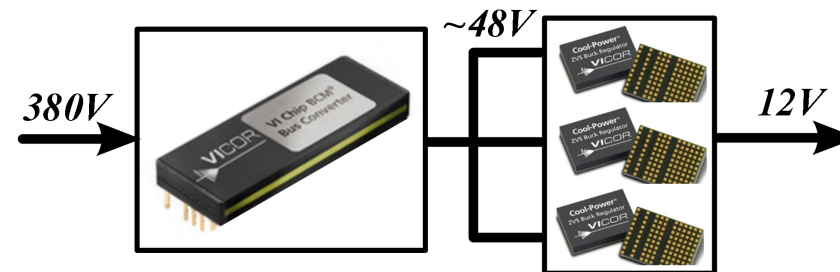
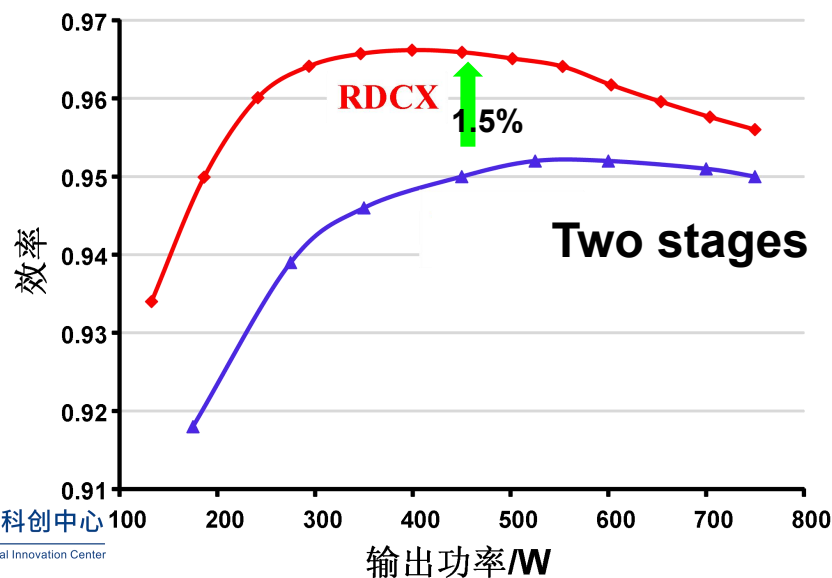


Auxiliary Transformer

V_{in} :340V-380VDC;
 V_o :12V/65A
 f_s :1MHz



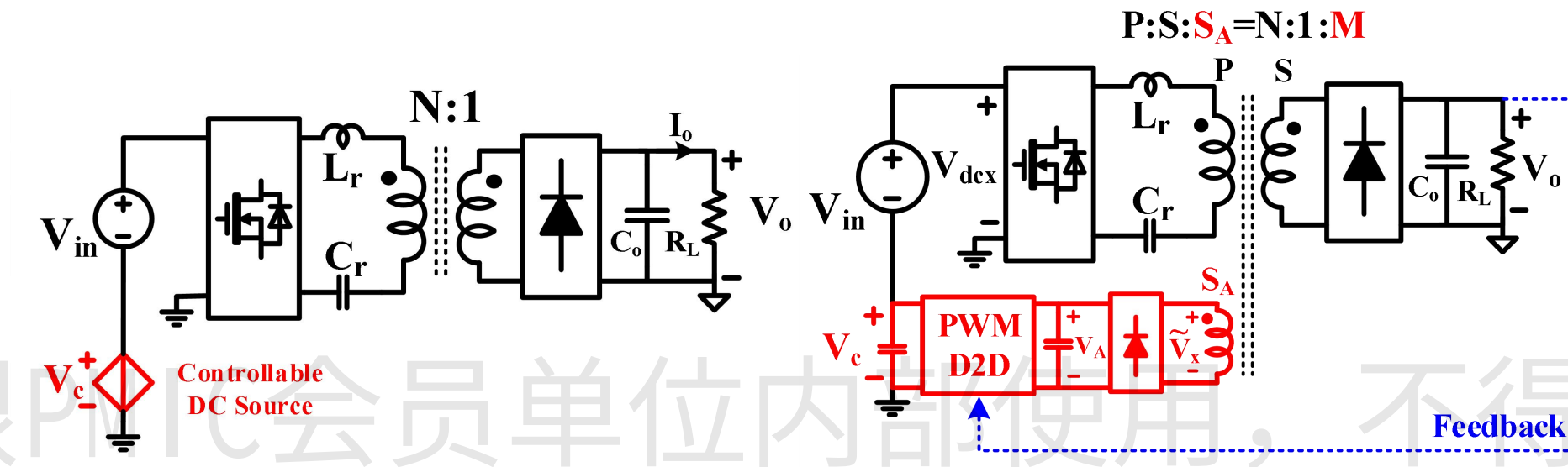
RDCX Density: 720W/in³



Two stages density: 560W/in³

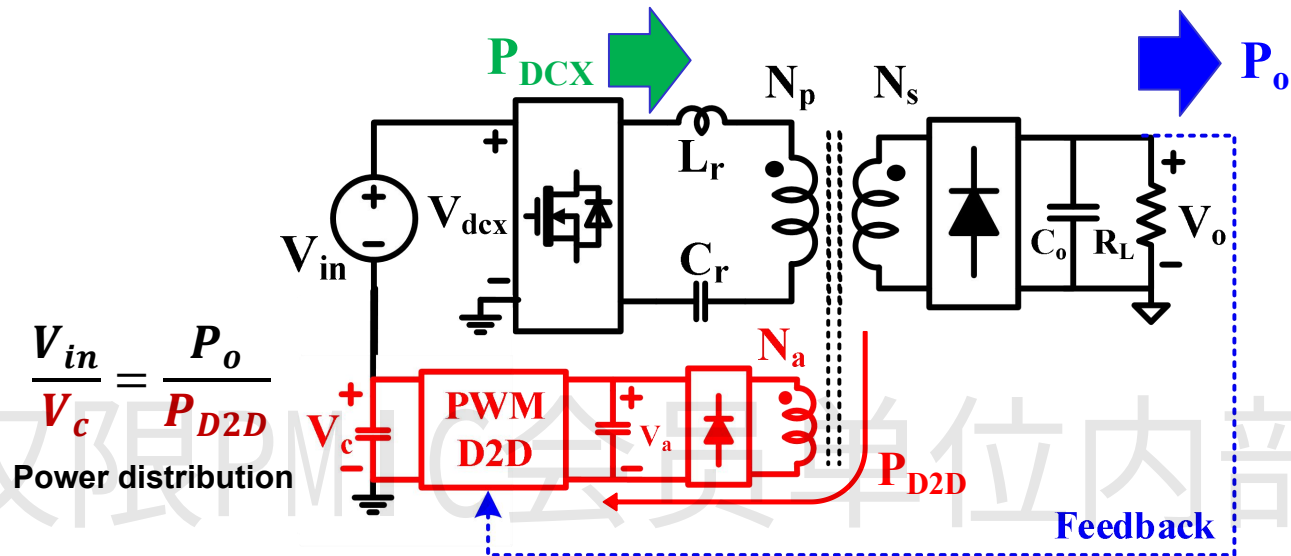
Ref:BCM6123xD1E5117yzzPI3526-00-LGIZ

RDCX - DC In Series / AC In Parallel - Example



- Regulated V_o
- Part power regulation
- Without additional transformer
- Suitable for high normal input voltage

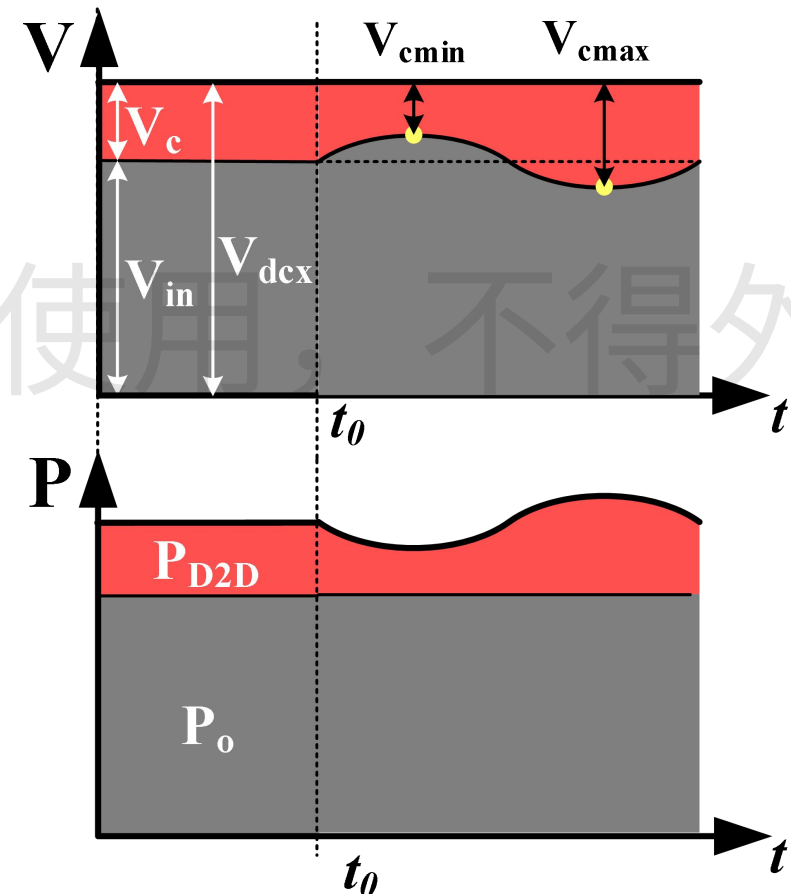
RDCX - DC In Series / AC In Parallel - Principle



Regulated DCX (RDCX)

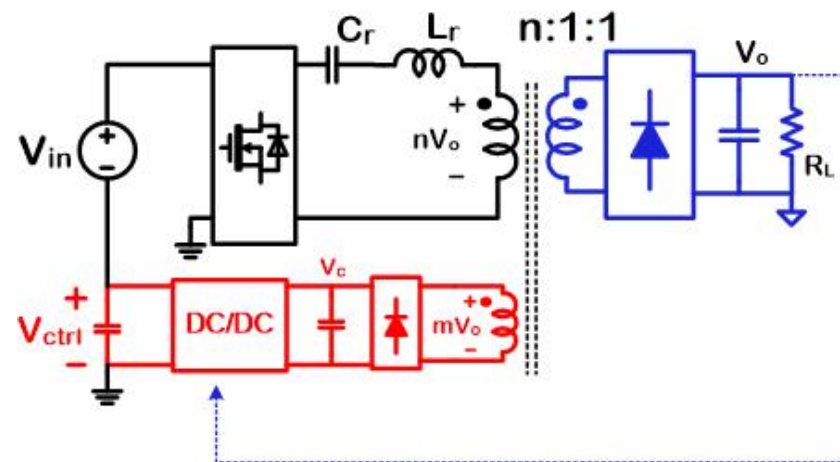
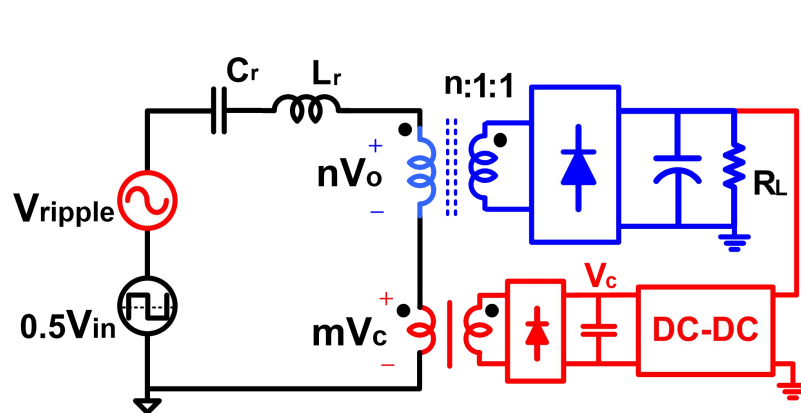


1. Tight regulated;
2. Optimized DCX;
3. Partial power regulation;
4. Simple control strategy.

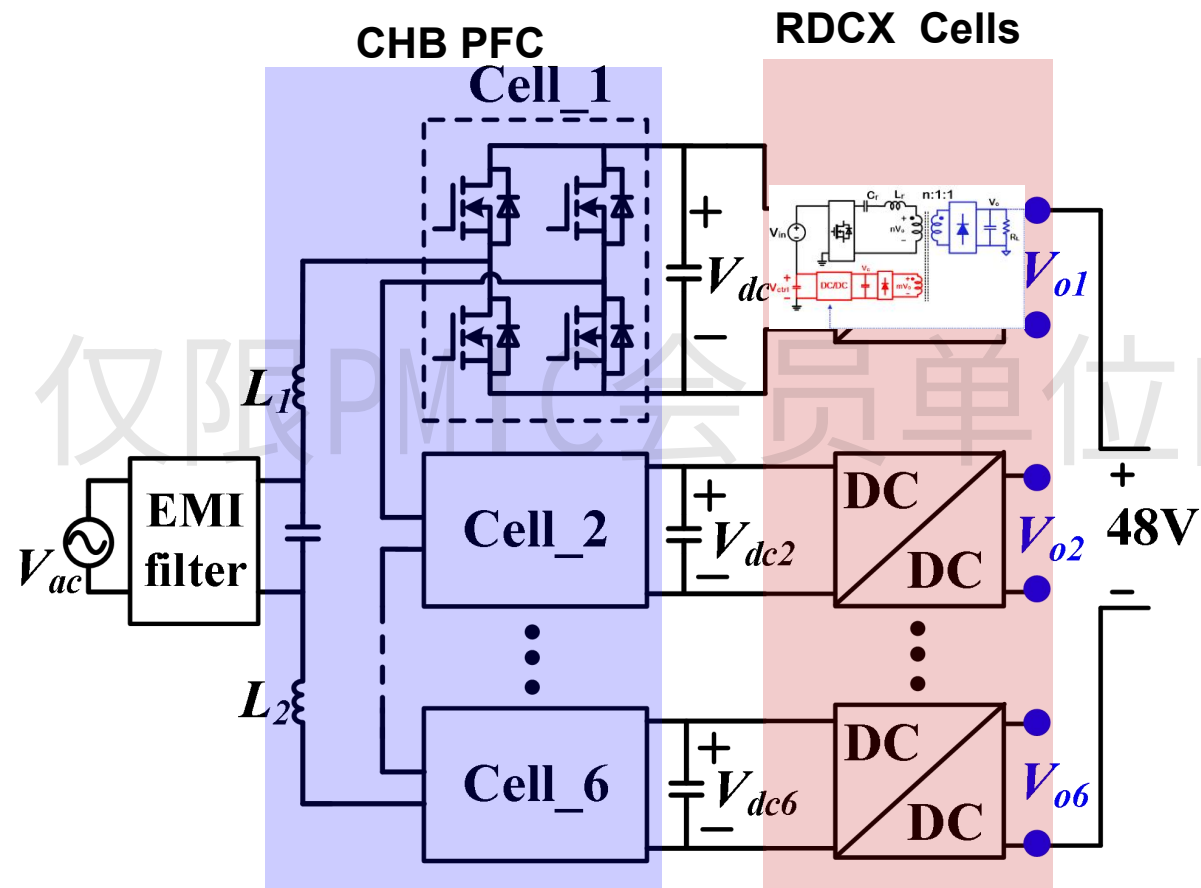


□ Main power stage stresses

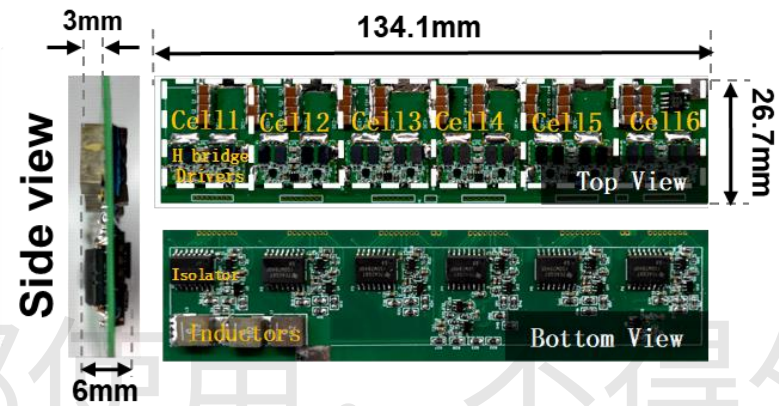
	LLC	AC series	DC series
Voltage stress	V_{in_max}	V_{in_max}	$N \cdot V_o \approx V_{in_max}$
Current stress	$\frac{\pi \cdot P_{o_max}}{2V_{in_min}} \cdot \frac{f_r}{f_{s_min}}$	$\frac{\pi \cdot P_{o_max}}{2V_{in_min}}$	$\frac{\pi \cdot P_{o_max}}{2V_{in_min}}$



Example: 48V output RDCX cell circuit with Multi-input in AC/DC Converter



CHB PFC:



Power density: 1500W/in³

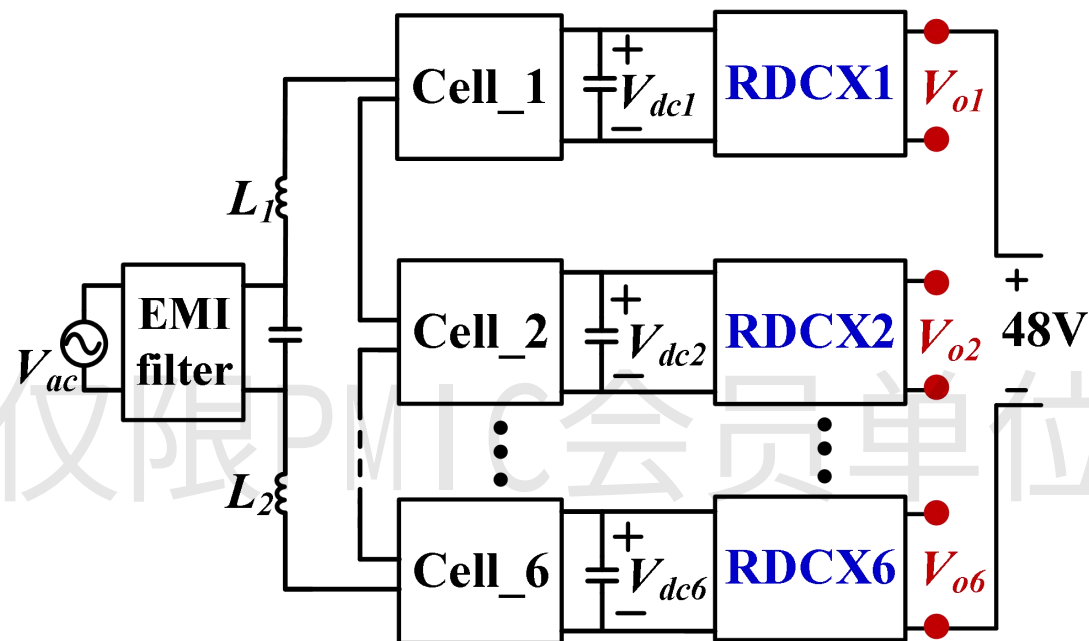
Peak efficiency: 99.1%(@220Vac)

DC/DC:

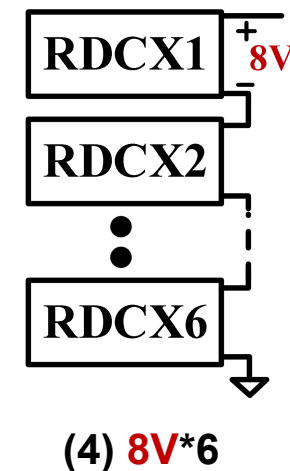
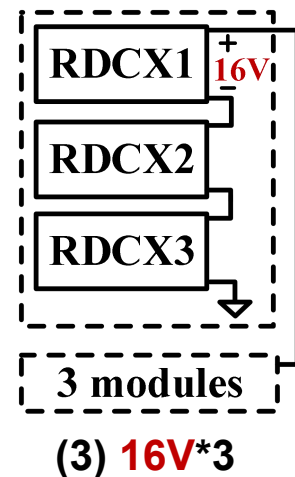
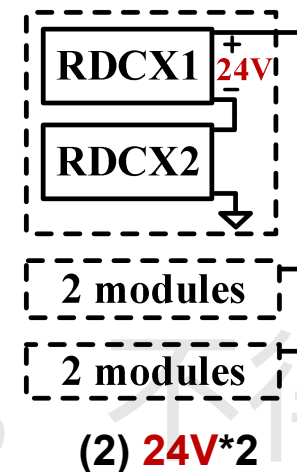
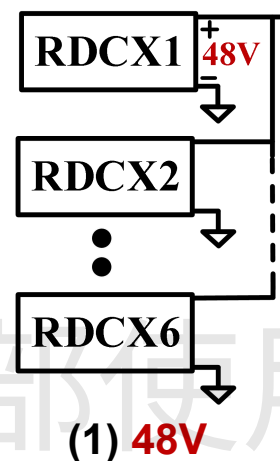
- 48V-level input
- Total 48V output
- Tight regulated and isolated

J. Wu, and X. Wu. "FoM Based Optimal Frequency and Voltage Level Design for High efficiency High density Multilevel PFC with GaN Device." APEC 2020

RDCX Output Connections in the Front-End Rectifier



Only 4 choices: $48V = 48V * 1 = 24V * 2 = 16V * 3 = 8V * 6$



Different V_o :

- Loss of Sec. (voltage stress of devices)
- Parameter design of other parts

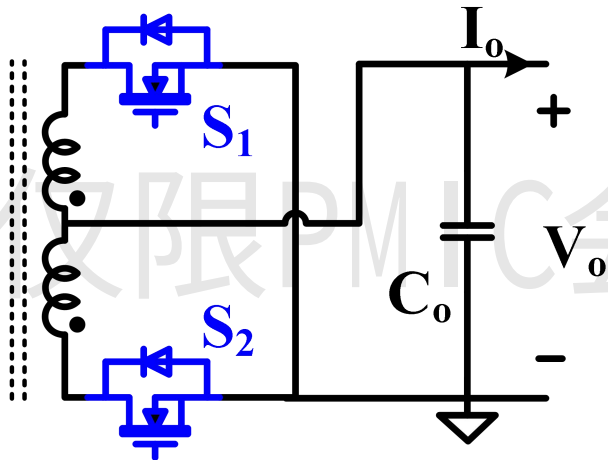
Loss model of Sec. switches at different V_o



Loss of Sec. switches:

$$P_s = P_{s_con} + P_{s_dri} = \frac{T_s I_o^2 \pi^2}{8 T_r} \cdot k_{temp} k_{dyn} R_{ds_on} + 2 V_g f_s \cdot \frac{FoM}{R_{ds_on}}$$

$$(FoM = Q_g * R_{ds_on})$$



Center-tapped rectifier (CTR)

Minimum loss:

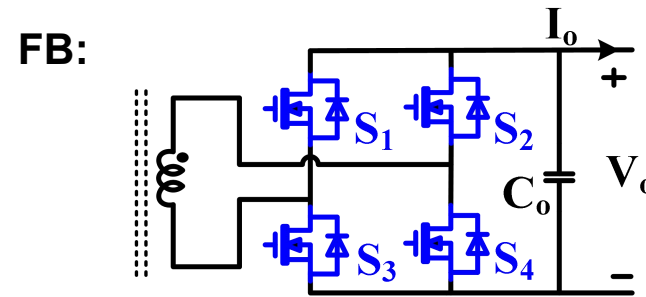
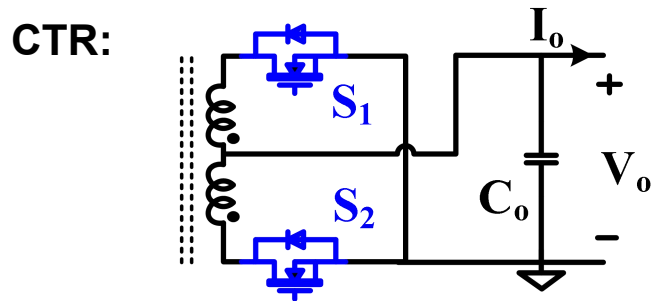
$$P_{s\min} = \pi I_o \sqrt{\frac{T_s}{T_r} \cdot V_g f_s k_{temp} k_{dyn} \cdot FoM} @ R_{ds_on} = \frac{4}{\pi I_o} \sqrt{\frac{T_r}{T_s} \cdot \frac{V_g f_s \cdot FoM}{k_{temp} k_{dyn}}}$$

Normalization:

$$P_{s\min_N} = \frac{P_{s\min}}{P_o} = \pi \sqrt{\frac{T_s}{T_r} \cdot V_g f_s k_{temp} k_{dyn}} \cdot \frac{\sqrt{FoM}}{V_o}$$

Determine the output voltage

Min. Loss of Secondary-Side Rectifier

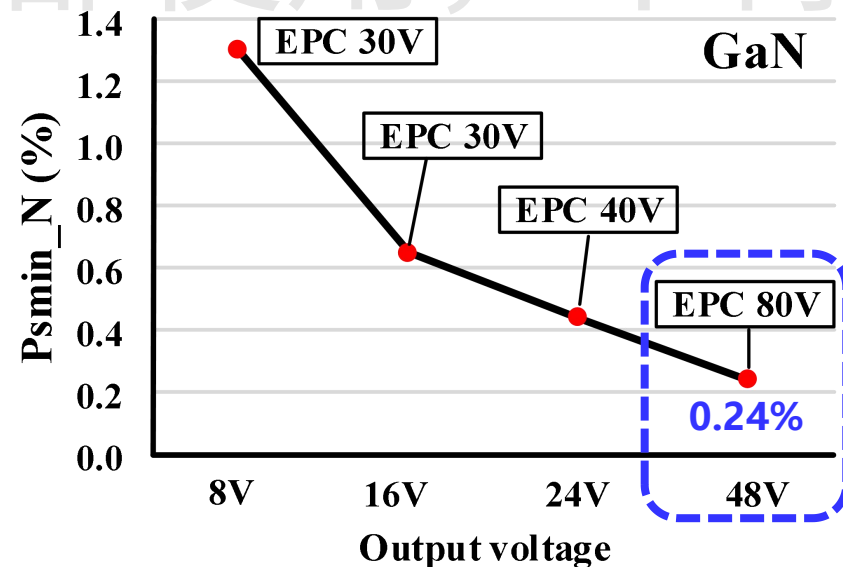
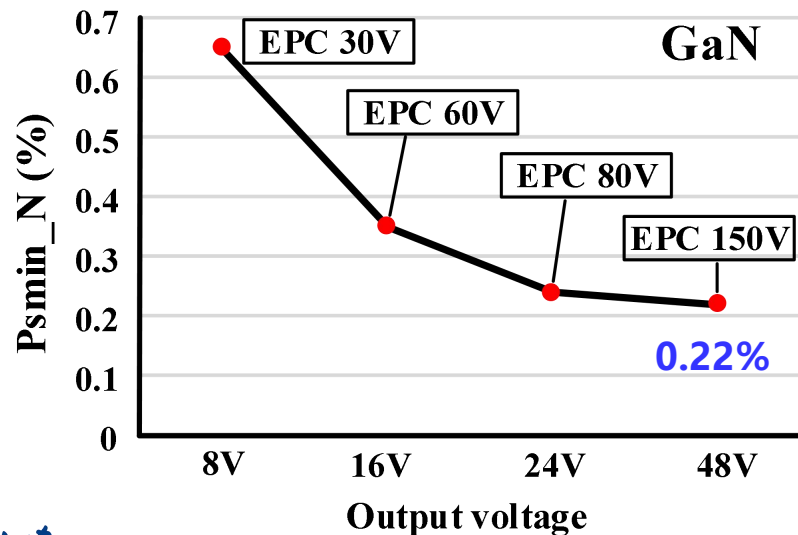


Min. loss:

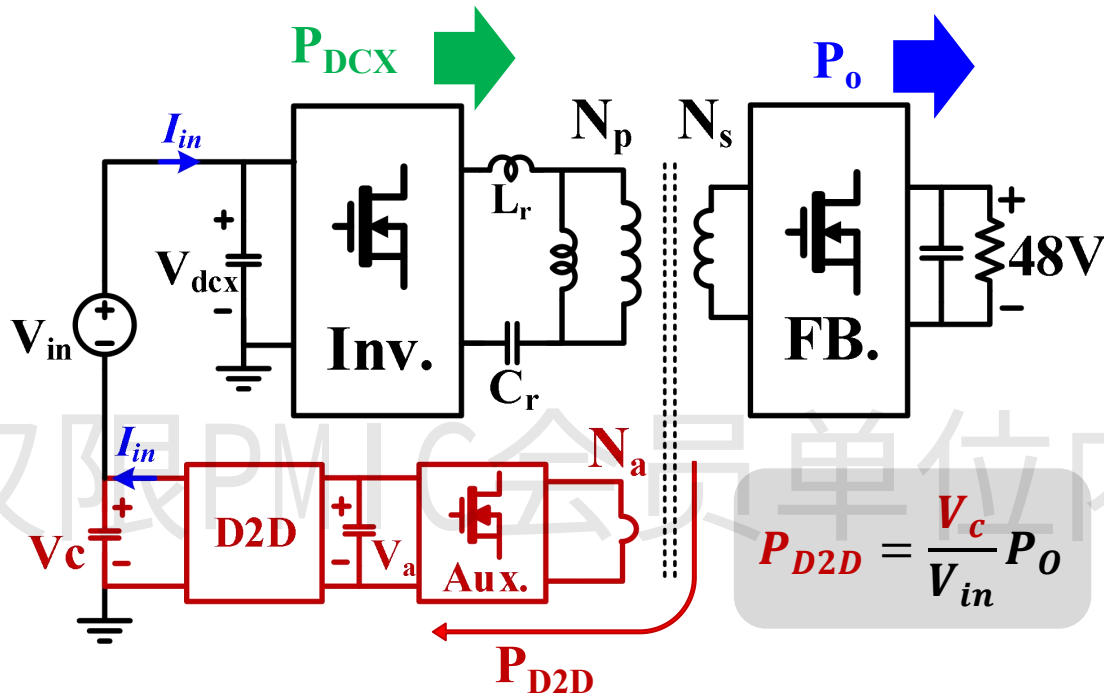
$$P_{smin_N} = \pi \sqrt{\frac{T_s}{T_r} \cdot V_g f_s k_{temp} k_{dyn}} \cdot \frac{\sqrt{FoM}}{V_o}$$

Min. loss:

$$P_{smin_N} = 2\pi \sqrt{\frac{T_s}{T_r} \cdot V_g f_s k_{temp} k_{dyn}} \cdot \frac{\sqrt{FoM}}{V_o}$$



Transformer Design - Turns Ratio Selection



V_o	48V
P_o	500W
V_{in}	61~71V
f_s	1MHz

Minimize V_c to improve efficiency:

$$V_{dcx} = V_{in} + V_c \geq V_{inmax} = 71V$$

$$N_p : N_s = V_{dcx} : V_o = 2.96 : 2 \approx 3 : 2$$

$$V_{dcx} = 72V$$

Inv.: Full bridge

Aux. circuit:

$$V_c = V_{dcx} - V_{in} = 1 \sim 11V$$

$$N_a = 1$$

Aux.: Center-tapped Rec.

D2D: Buck

$$N_p : N_s : N_a = 3 : 2 : 1$$

Relationship between the shape and loss of transformer

[1] T. Liu, et al., 1 MHz 48V-12V Regulated DCX with Single Transformer, JESTPE,

Area limitation to design a:

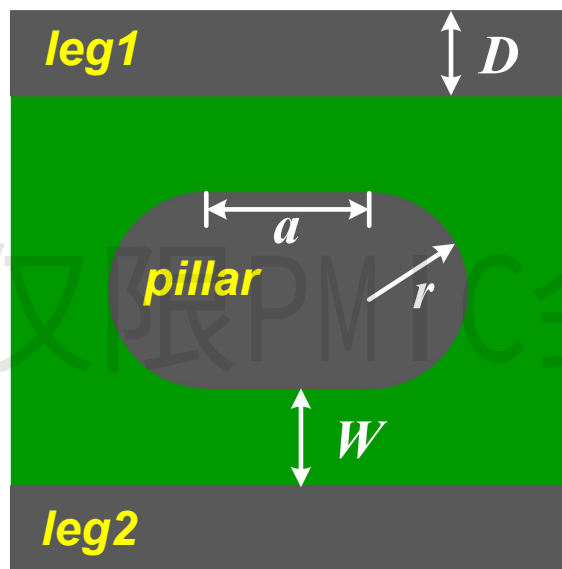
Area of leg:

$$S_{leg} = D \cdot (2r + 2W + a) = 0.5 A_e$$

Area of pillar:

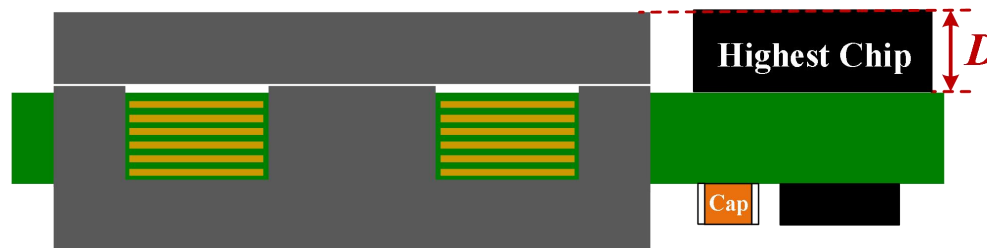
$$S_{pillar} = \pi r^2 + 2ar = A_e$$

$$a = \frac{4D(r + W) - \pi r^2}{2(r - D)}$$



a, r, W, D need design

Height limitation to design D:



Highest chip: Isolator



Height=1.8mm

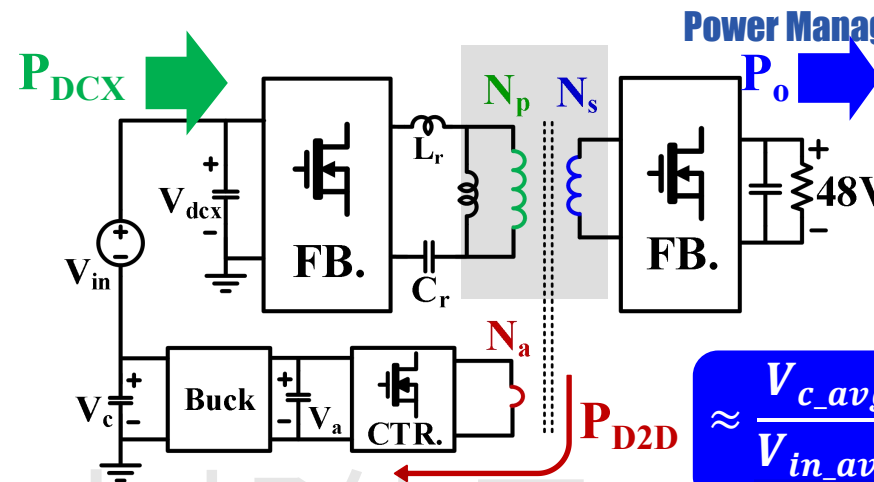
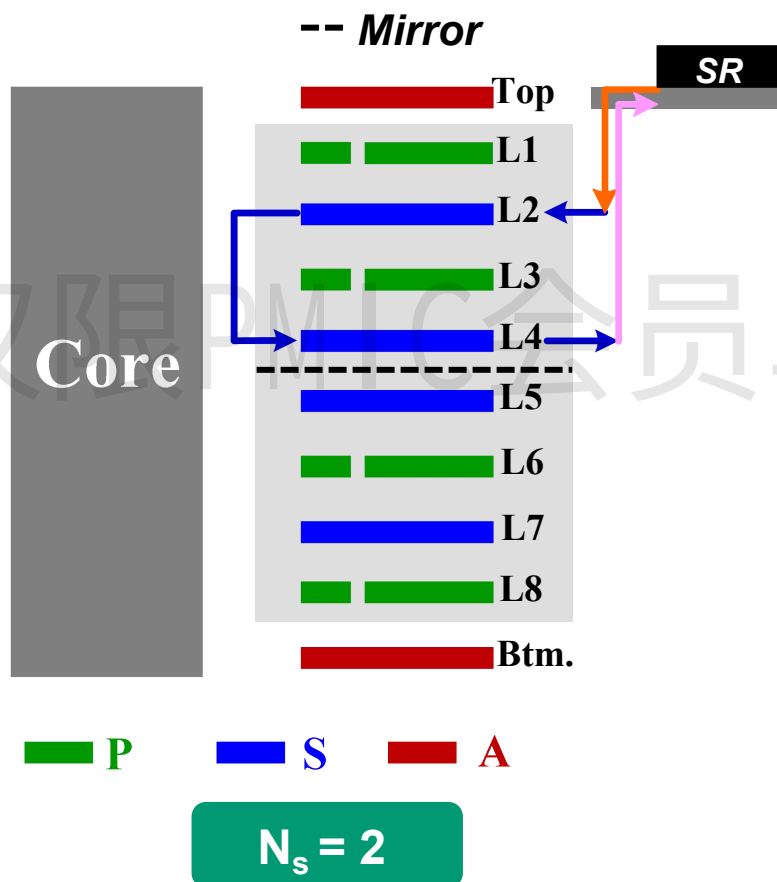
Define: D=1.9mm

$$\text{Core loss: } P_{fe} = P_v(Ae) \cdot V_e(r, W) = P_v(r, W) \cdot V_e(r, W)$$

Copper loss in function of shape

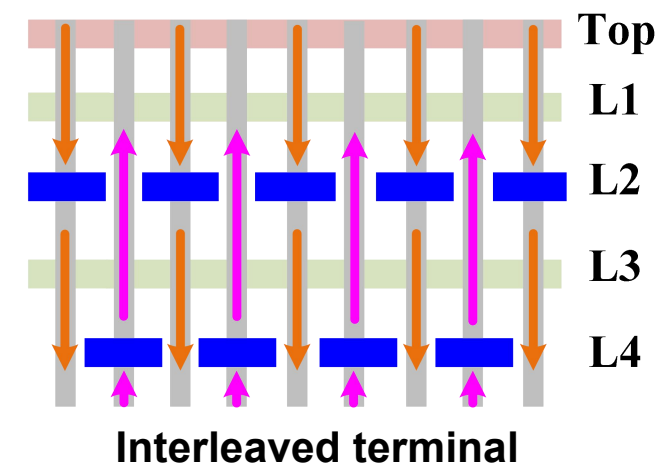
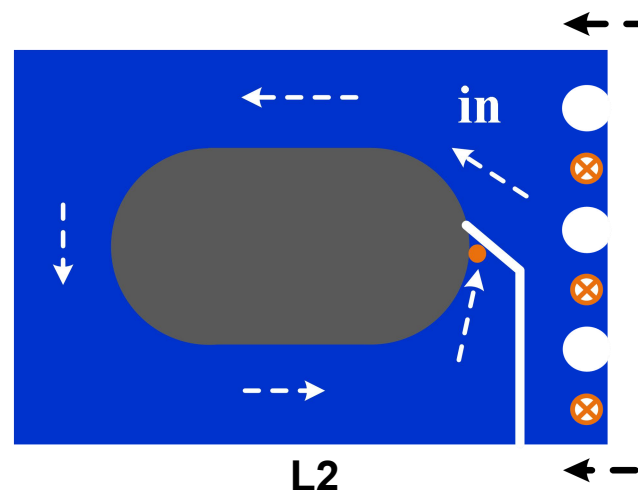
Secondary-side Winding with Interleaved Terminal

10-layer board:



$$\approx \frac{V_{c_avg}}{V_{in_avg}} P_o = 9\% P_o$$

Second-side winding terminal:

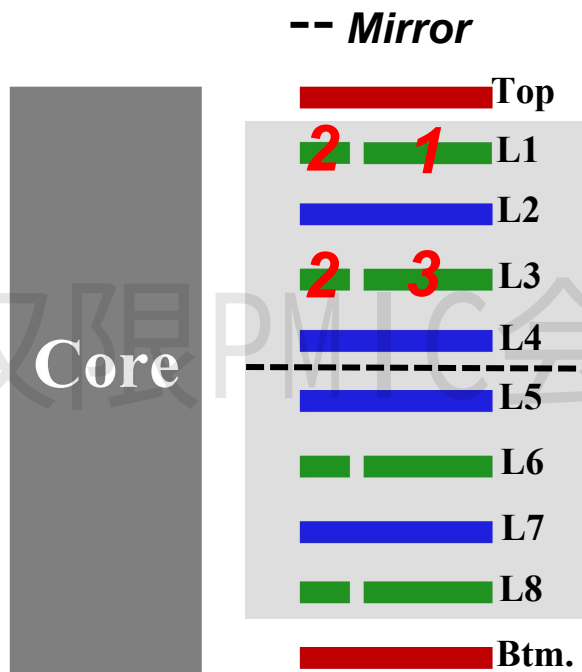


Primary-side winding design



3-turn Primary Winding in 2 Layers

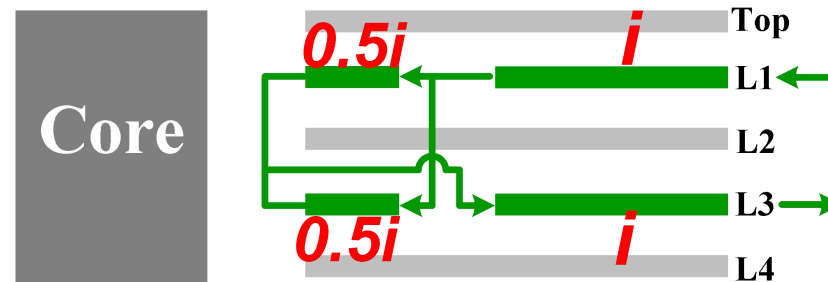
10-layer board:



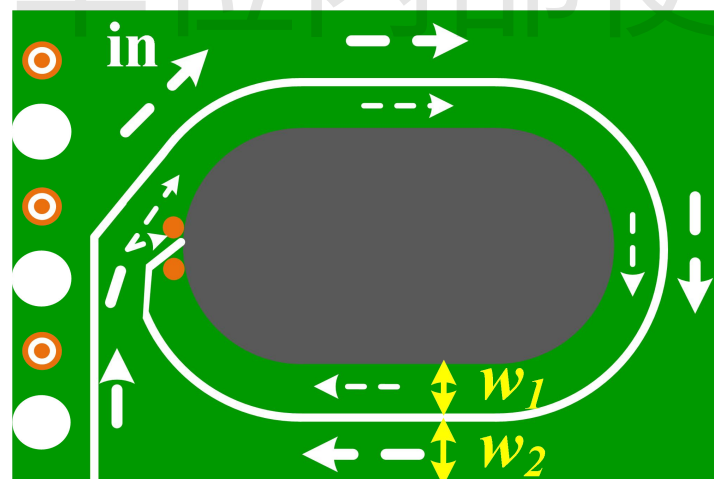
P S A

$N_p = 3$

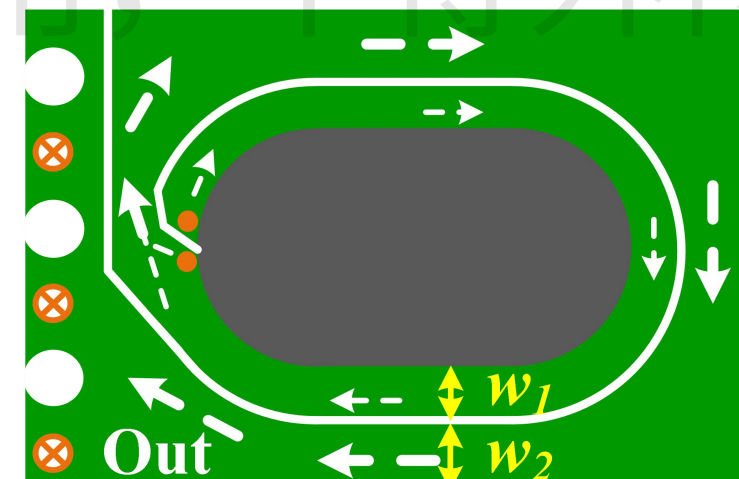
Current in L1 and L3:



Primary-side winding structure:

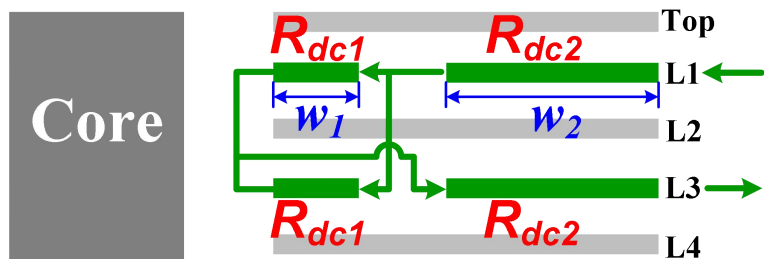


L1 & L8



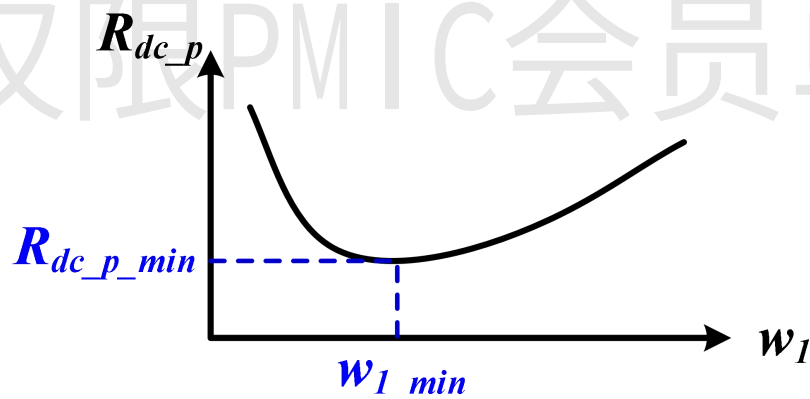
L3 & L6

Design w_1 and w_2 to get minimum loss



DC resistance of primary-side winding:

$$R_{dc_p}(r, W, w_1) = \frac{1}{2} [2R_{dc_2}(r, W, w_1) + \frac{1}{2}R_{dc_1}(r, W, w_1)]$$



Achieve minimum Pri. copper loss:

$$R_{dc_1}(r, W, w_{1_min}) = 2 \cdot R_{dc_2}(r, W, w_{1_min})$$

$$\Rightarrow R_{dc_p}[r, W, w_{1_min}(r, W)] = R_{dc_p}(r, W)$$

Copper loss: $P_{cu} = k_{ac} k_{temp} [R_{dc_p}(r, W) \cdot i_{prms}^2 + R_{dc_s}(r, W) \cdot i_{sms}^2 + R_{dc_a}(r, W) \cdot i_{arms}^2]$

Min. Transformer Loss under Each Footprint

Core loss:

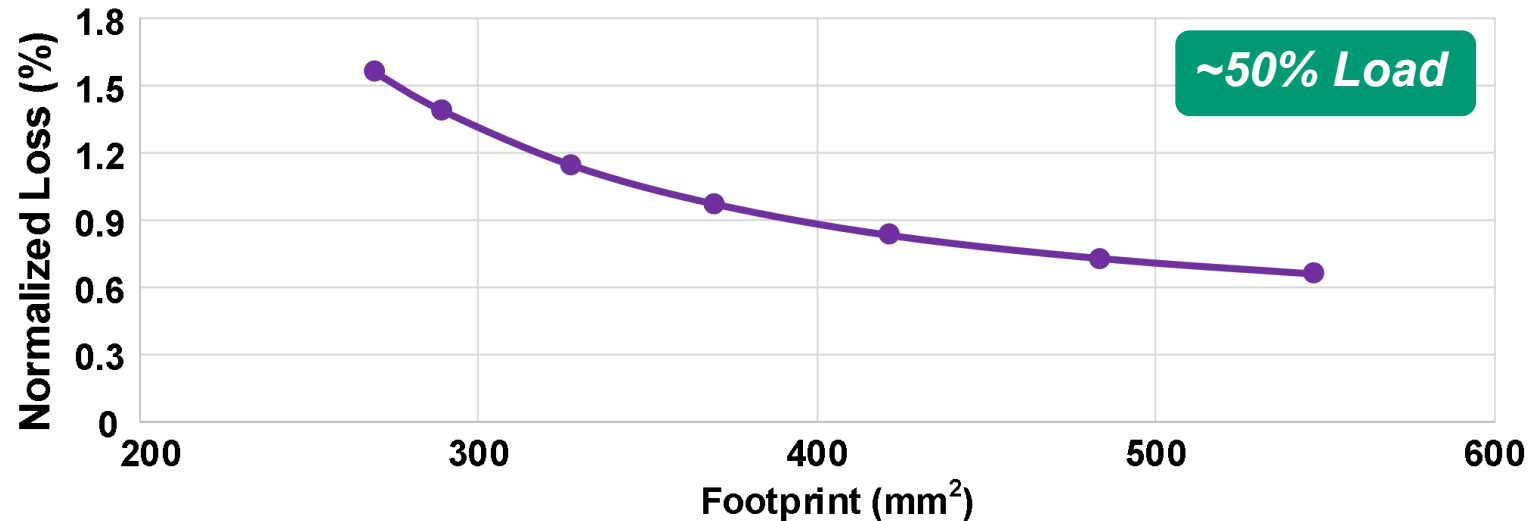
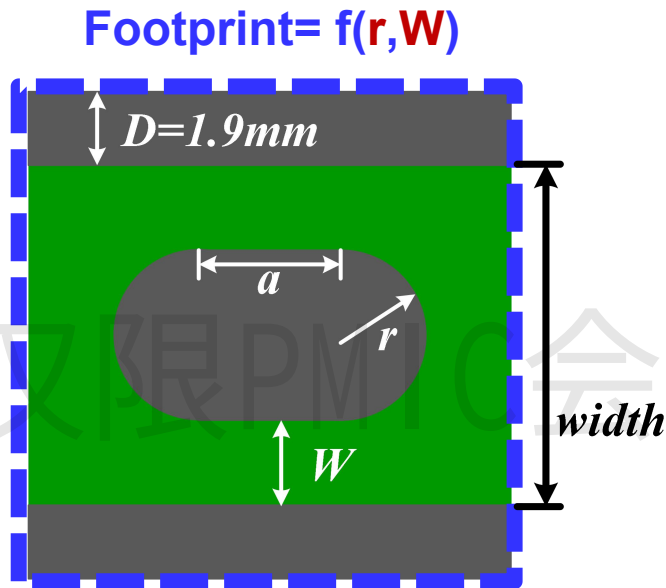
$$P_{fe}(r, W) = P_v(Ae) \cdot V_e(r, W) = P_v(r, W) \cdot V_e(r, W)$$

Copper loss:

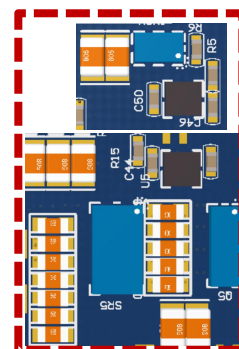
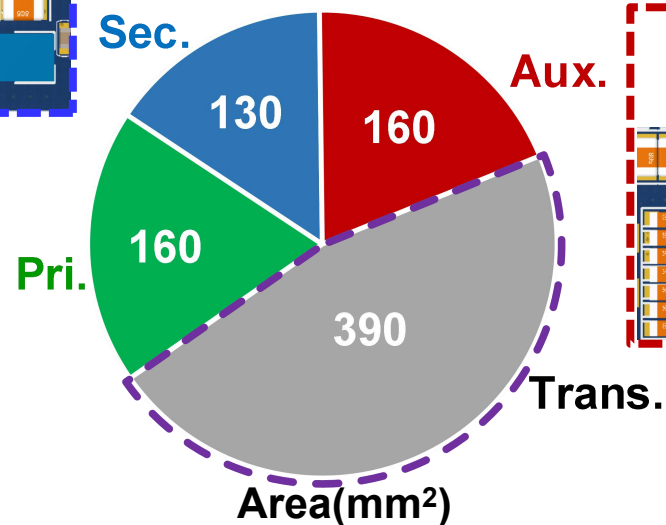
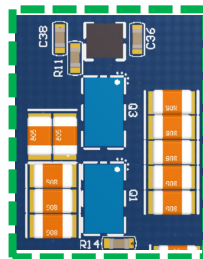
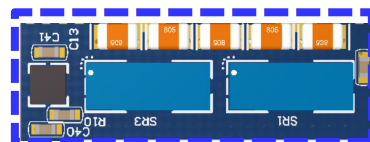
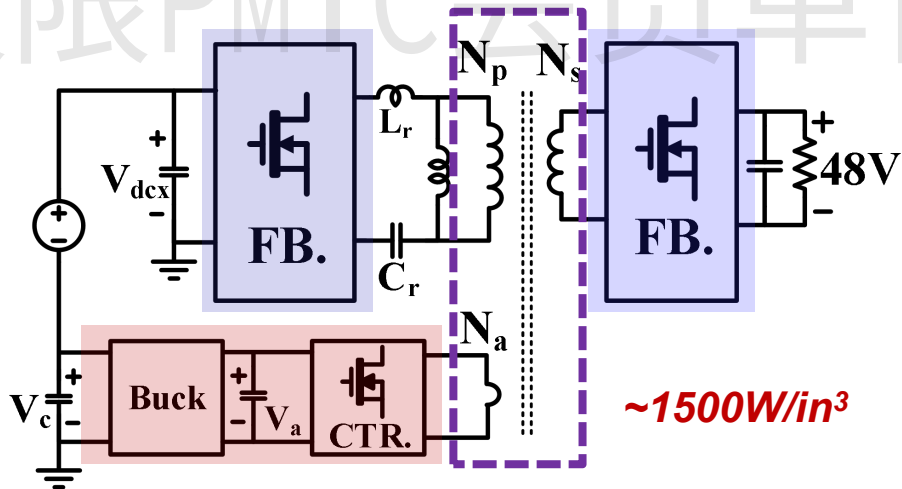
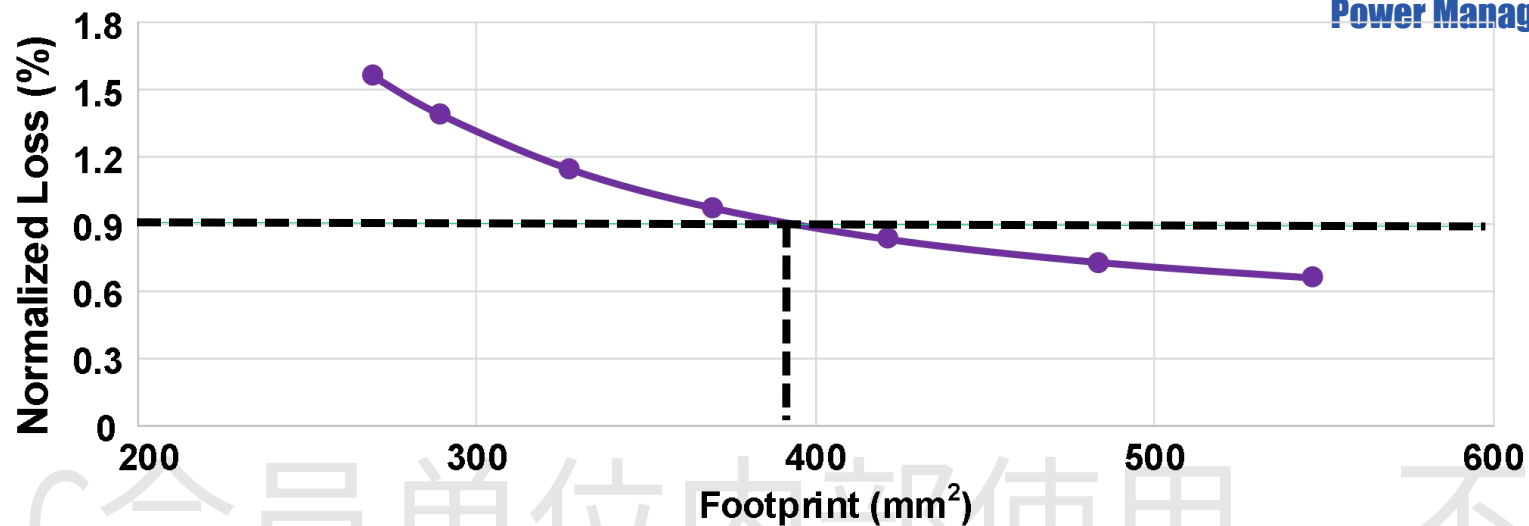
$$P_{cu}(r, W) = k_{ac} k_{temp} \left[R_{dc_p}(r, W) \cdot i_{prms}^2 + R_{dc_s}(r, W) \cdot i_{srms}^2 + R_{dc_a}(r, W) \cdot i_{arms}^2 \right]$$

Considering the width of transformer window:

$$width = 2(r + W) = 14mm$$



Design Point of Transformer

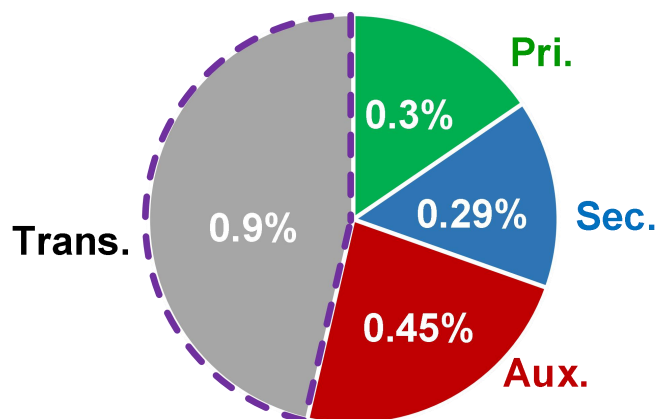
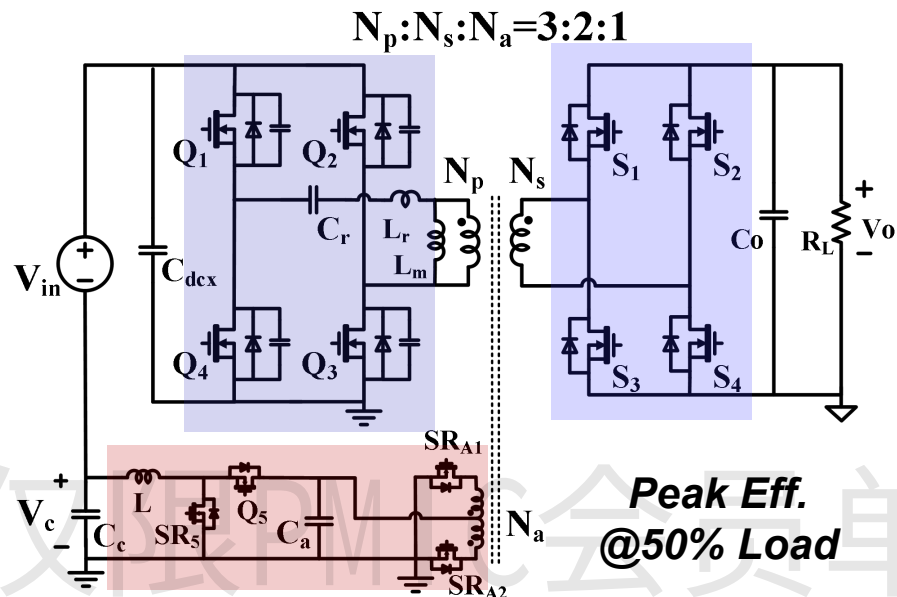


Height=6.5mm

Area $\approx$ 840mm²



Switching Device Selection



Peak efficiency: ~98%

Secondary-side full bridge:

$$R_{smin} = \frac{4}{\pi I_o} \sqrt{\frac{T_r}{T_s} \cdot \frac{V_g f_s \cdot FoM}{k_{temp} k_{dyn}}} = 1.5m\Omega \rightarrow \boxed{Rs=2.2m\Omega}$$

Loss: 0.29%

Aux. Buck (600kHz):

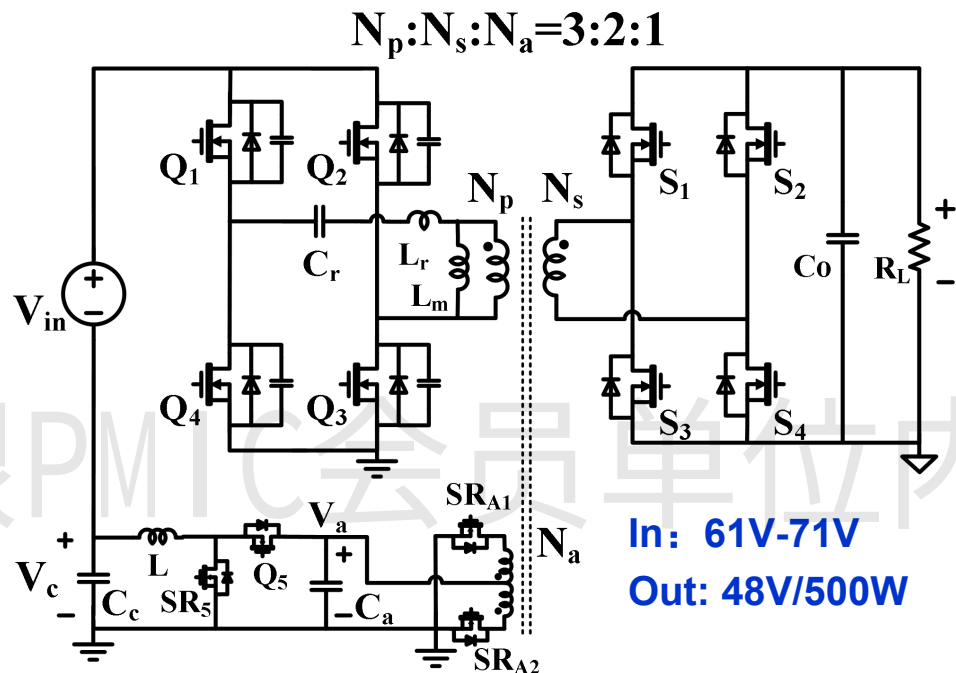
Peak efficiency: ~95% (by experience) $\xrightarrow{P_{D2D} \approx 9\%P_o}$ $P_{bmin_N} \approx 0.45\%$

Primary-side full bridge:

$$R_{pmin} = \frac{2V_{in}}{\pi V_o I_o T_s} \sqrt{\frac{16N_p^2 V_o^2 N FoM^2 T_r^2}{N_s^2 t_d^2} + \frac{4V_g T_r FoM}{k_{dyn} k_{temp}}} = 2.5m\Omega$$

$\rightarrow \boxed{Rp=3.8m\Omega}$ Loss: 0.3%

Prototype and Parameters of RDCX Cell



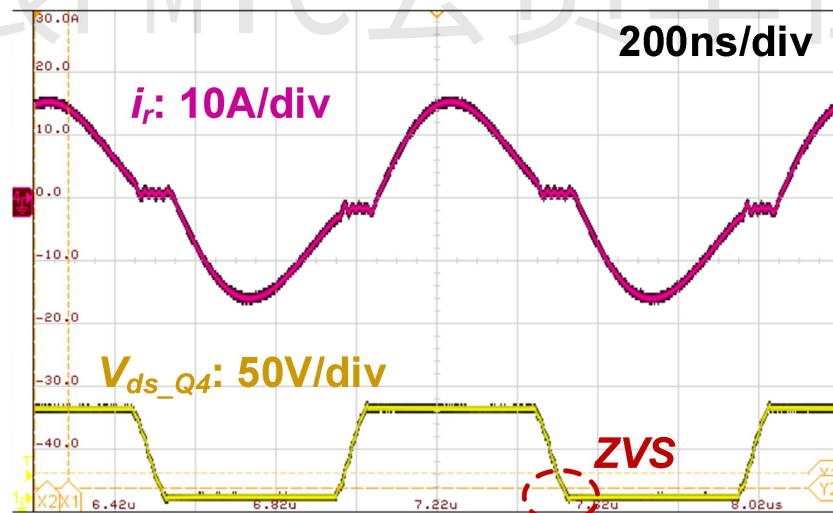
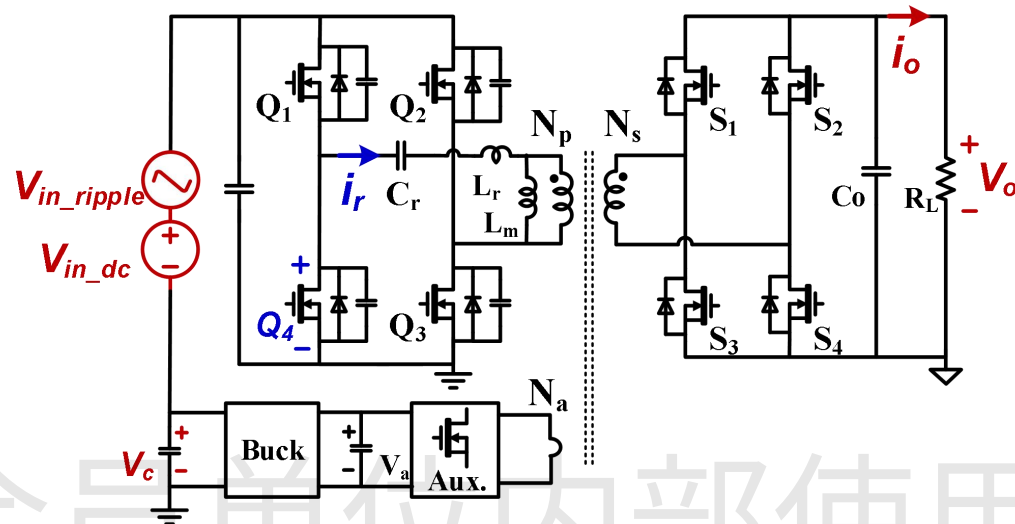
DCX	
Q1-Q4	EPC2053
S1-S4	EPC2206
SRA1-SRA2	EPC2045
Cr	1000nF
Core Material	DMR51W
fs	1MHz
Buck	
Q5	EPC2015C
SR5	EPC2030
L	2.7uH
fb	600kHz



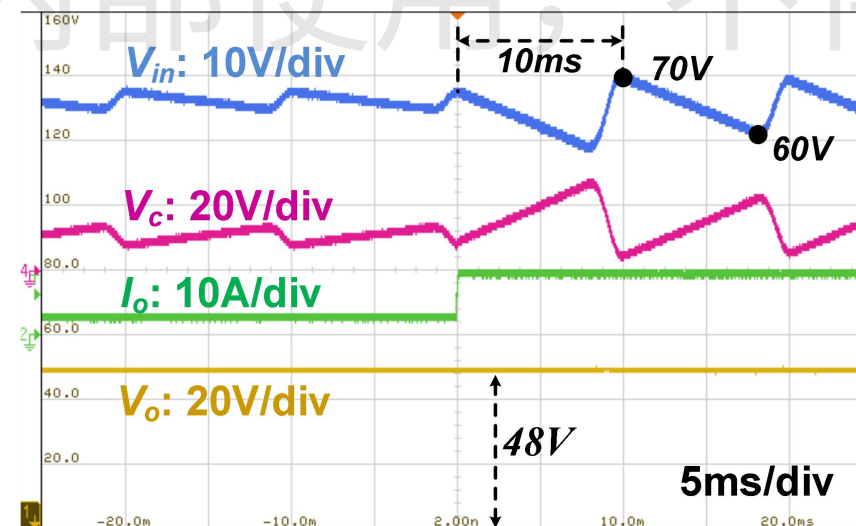
Size: 43.5*19.5*6.5mm³

Density: ~1500W/in³

Key Waveforms of RDCX Cell



Full load waveform @ $V_{in}=66V$



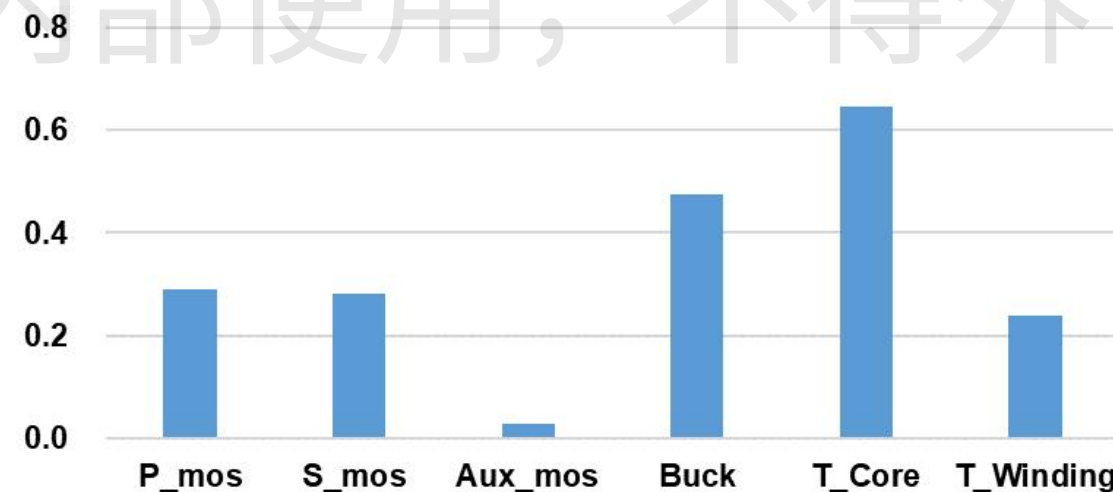
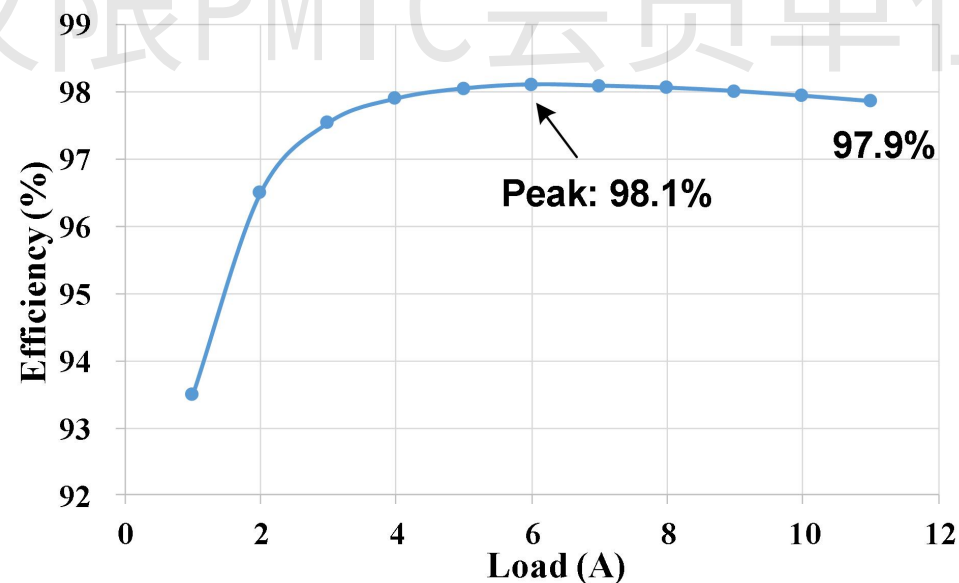
Load step from 3A to 10A

Efficiency of RDCX Cell



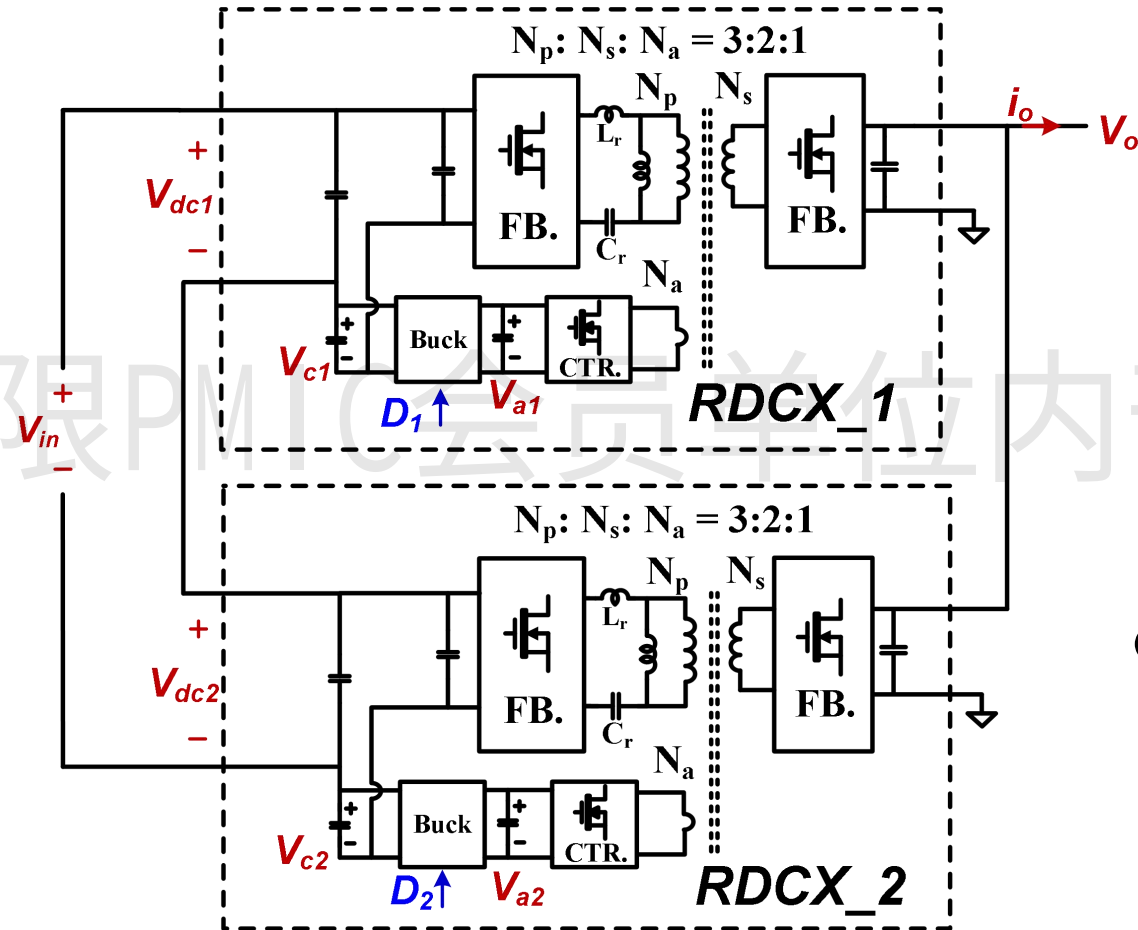
Parameters:

- In: 61-71V;
- Out: 48V-500W
- Density: **~1500W/in³**
- Peak Eff.: **98.1%**



Loss breakdown @50% Load

2-Cell ISOP Input Voltage Sharing Control Strategy



Voltage Gain:

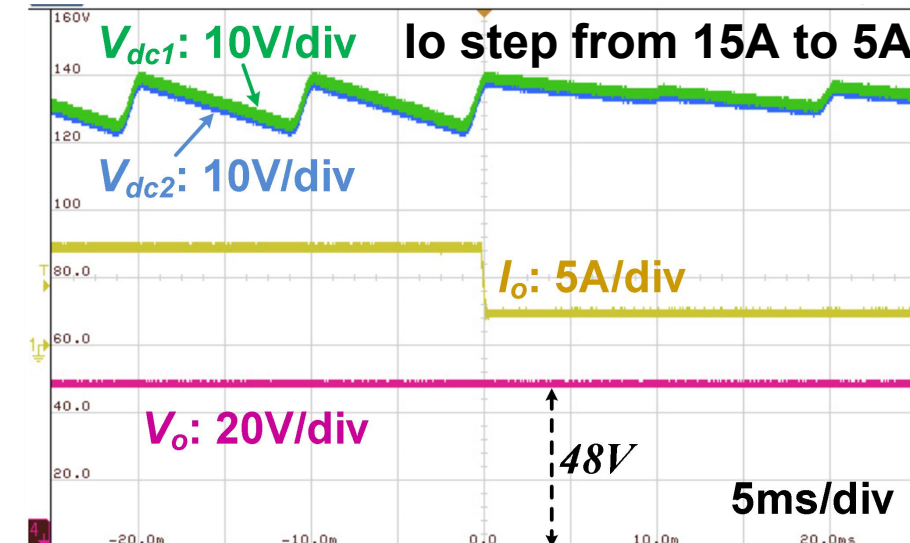
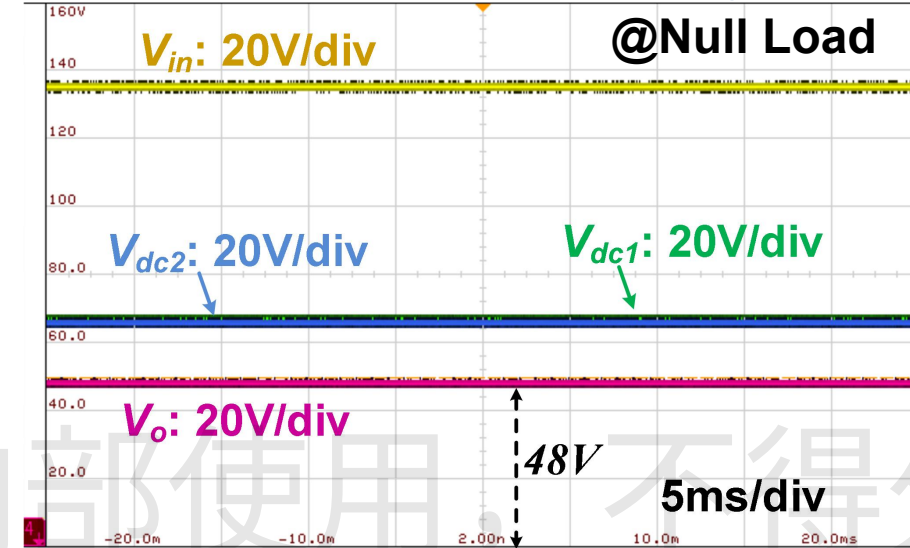
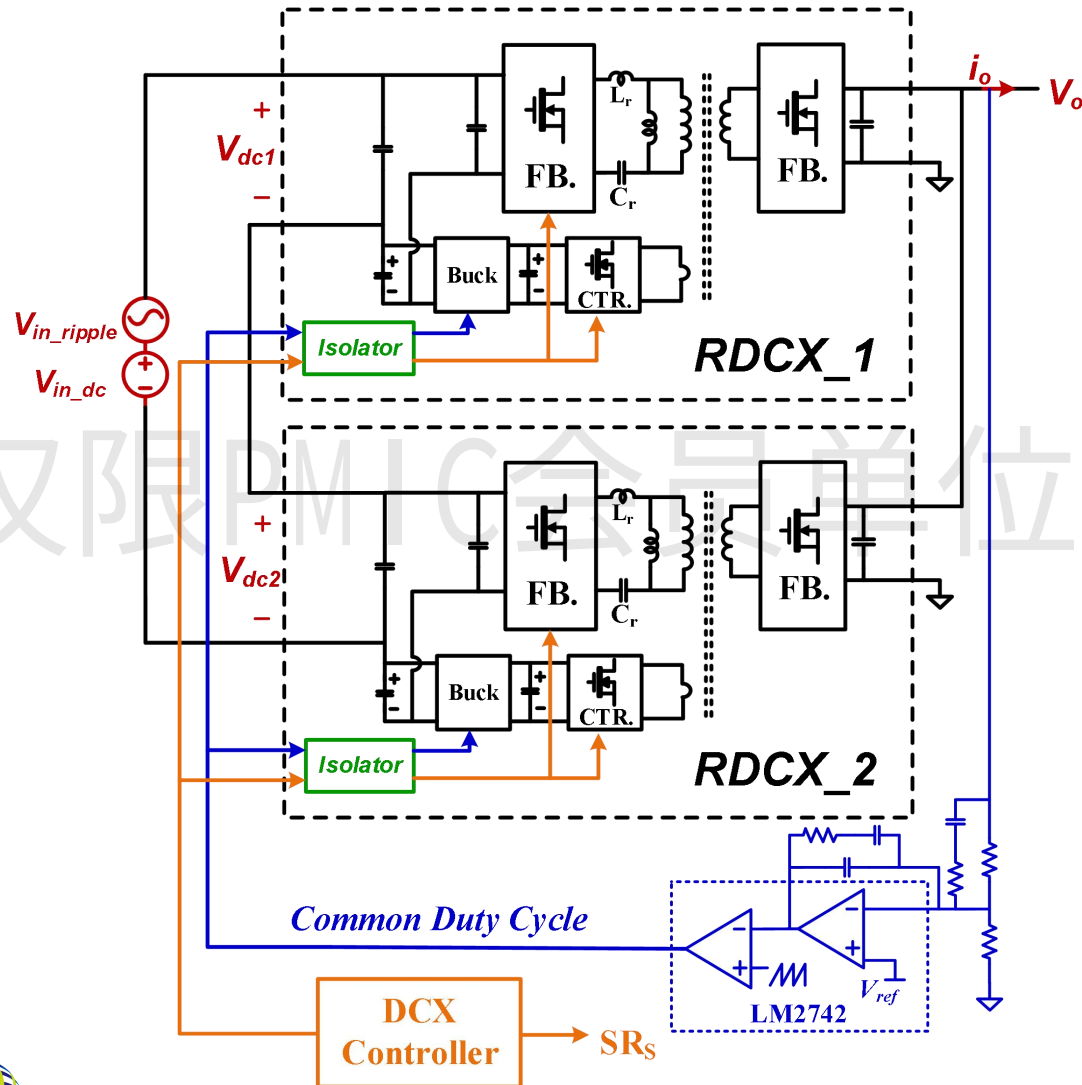
$$\frac{V_o}{V_{dc1}} = \frac{N_s}{N_p - D_1 \cdot N_a}$$

$$\frac{V_o}{V_{dc2}} = \frac{N_s}{N_p - D_2 \cdot N_a}$$

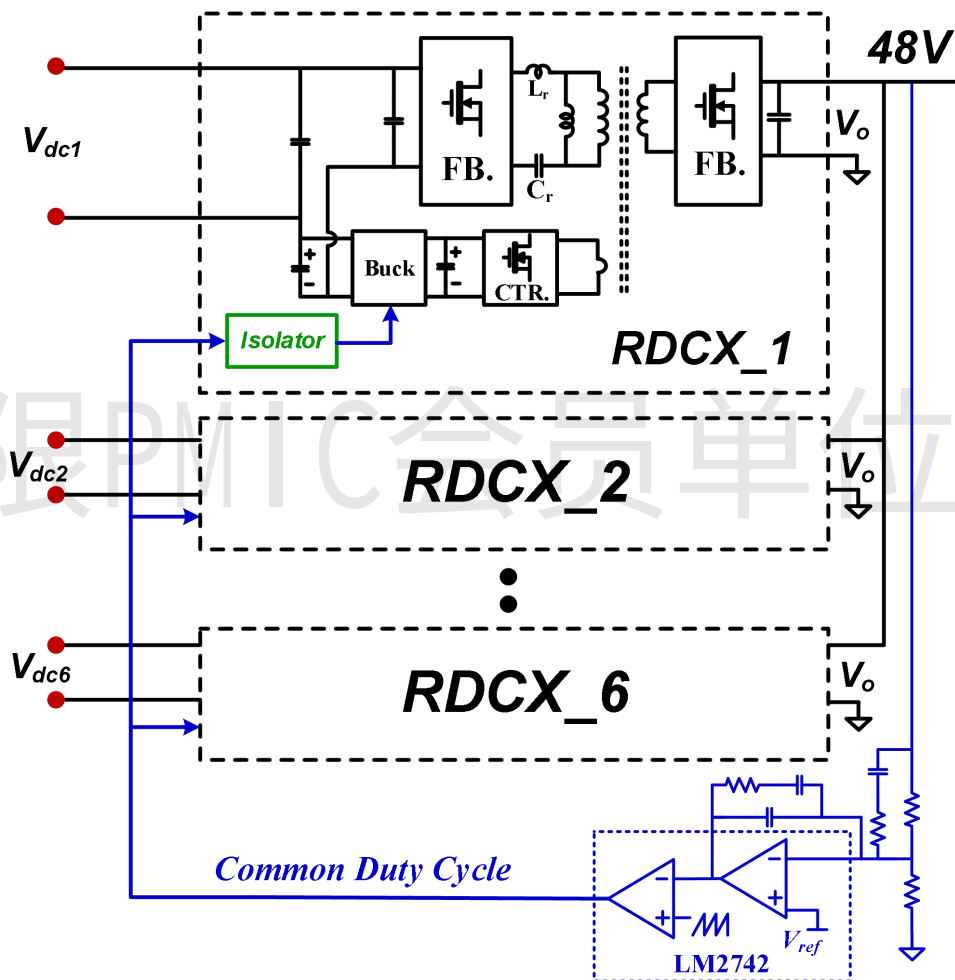
Common-duty-cycle control: $D_1 = D_2$

$$V_{dc1} = V_{dc2}$$

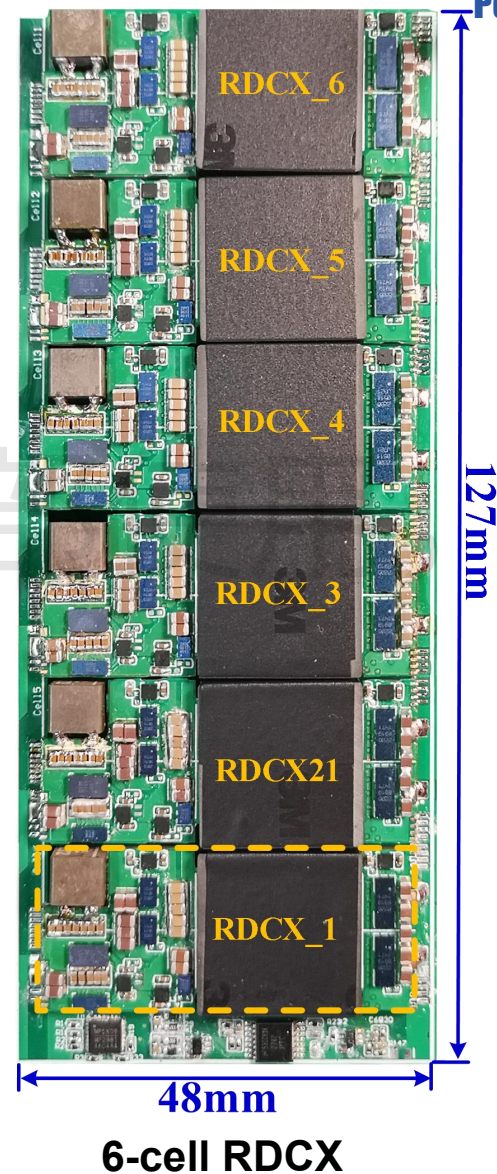
2-Cell ISOP RDCX Operation



Prototype of 6-Cell RDCX



Common-duty-cycle control



Parameters:

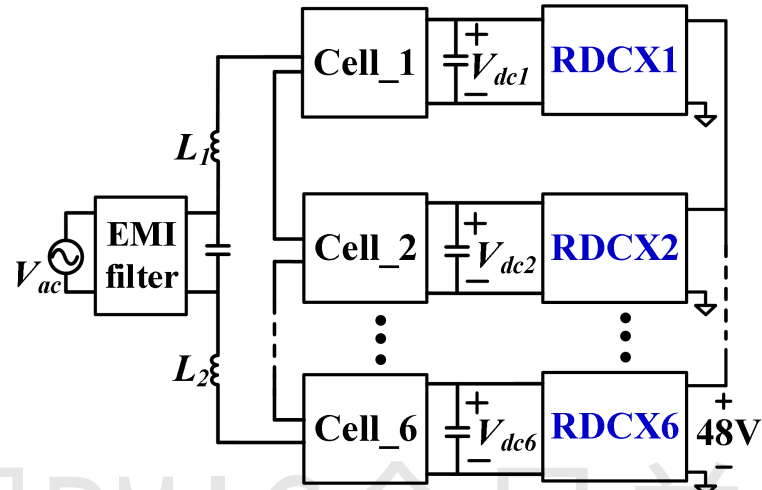
Power: 3kW

Height: 6.5mm

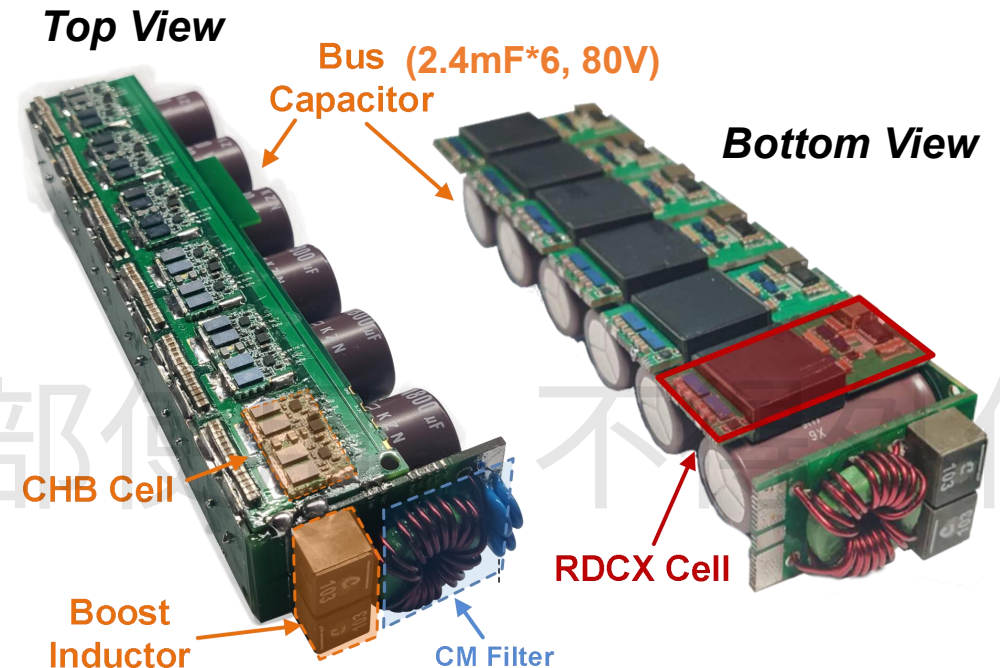
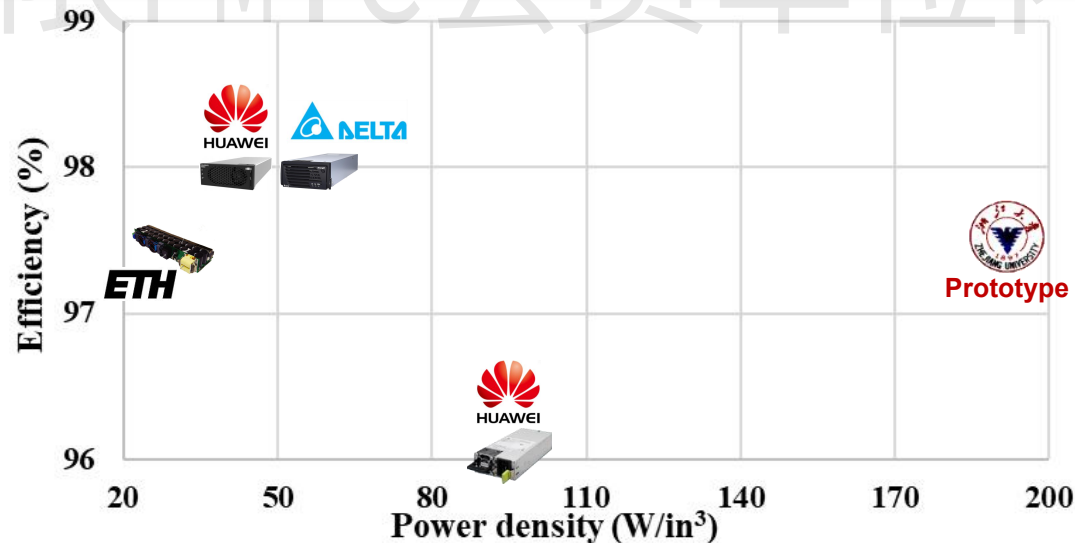
Density: $\sim 1300\text{W/in}^3$
(with Controller)

Front-End AC/DC Rectifier Prototype with Six RDCX Cells

Power Management Innovation Consortium



Proposed front-end rectifier with 6-cell RDCX



Front-end rectifier prototype

- Density: **190W/in³** (3kW)
- Peak Eff.: **97.2%** (half Load)



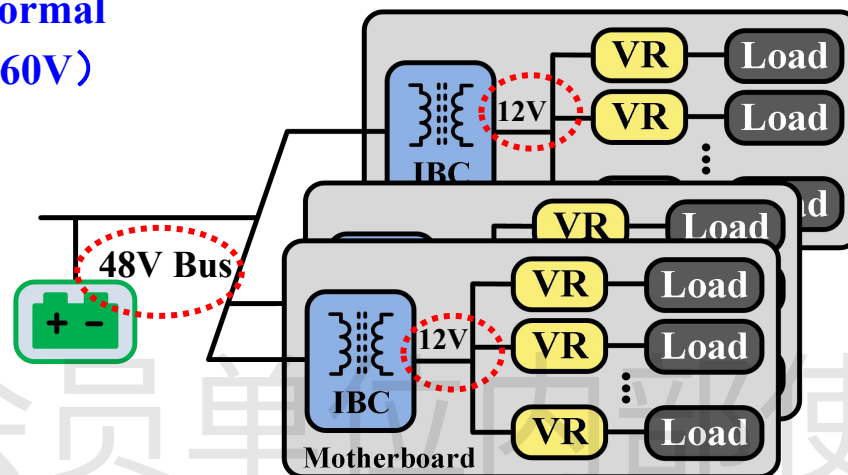
- ❑ Cellular 380V DCX namely using Low NFoM device in stead of high voltage switch
 - ❑ Achieving MHz High frequency and high efficiency
 - ❑ Low common mode EMI
 - ❑ Reduced conduction loss and flexible output
- ❑ Regulated DCX (RDCX) instead of two-stage scheme
 - ❑ MHz high efficiency dc-dc with regulating capability
 - ❑ Fixed switching frequency for DCX and PWM converter
 - ❑ Most power is transferred to load by DCX, small portion power is transferred to load by two stage.
- ❑ Cellular RDCX for a multi-input DC-DC stage in AC/DC converter
 - ❑ MHz frequency with low voltage switches
 - ❑ High efficiency and high density are both achieved



1. Introduction of power supply architecture of internet datacenter and popular high density high efficiency applications.
2. Topology for MHz high efficiency 380V-48V/12V power conversion
 - 2.1 Unregulated DC-DC techniques
 - 2.2 EMI design considerations of planar PCB transformer
 - 2.3 Tight regulated 380V-12V conversion
3. **MHz high efficiency 48/12V/XV power converters**
 - 3.1 **Low power DCX converter for intermedia bus application.**
 - 3.2 Tight regulated DC-DC converter for 48V-12V in server
 - 3.3 High Density Transformer Design for 48V MHz DC-DC converter
4. Conclusions



~54V Normal
(42V~60V)



Intermediate Bus Architecture

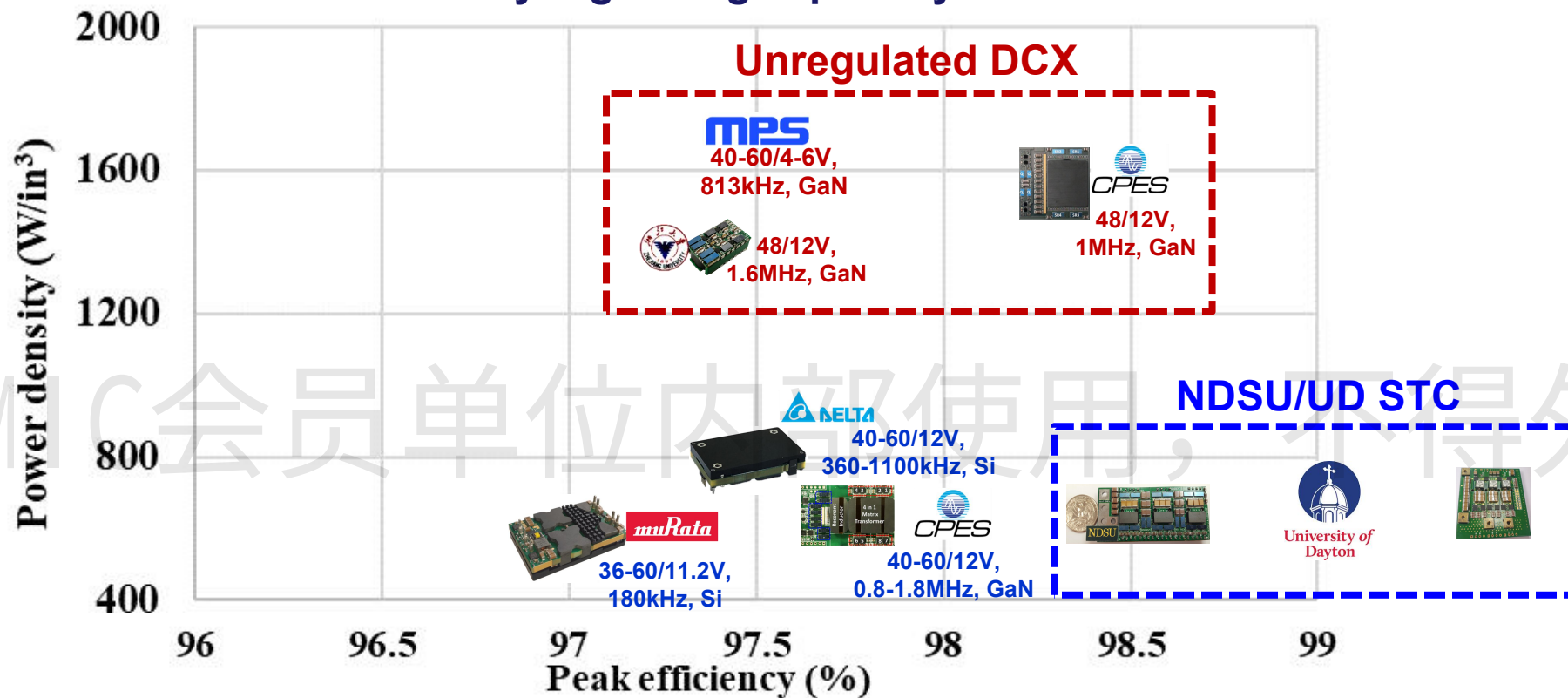
Requirements:

- ❑ High Efficiency
- ❑ High power density
- ❑ Voltage regulation capability (option)
- ❑ Wide input voltage range

Bus converter with 48V Input

By regulating capability

Power Management Innovation Consortium



[1] DRQ-11.4/88-L48NB-C, murata

[2] Q54SJ108A2, Delta

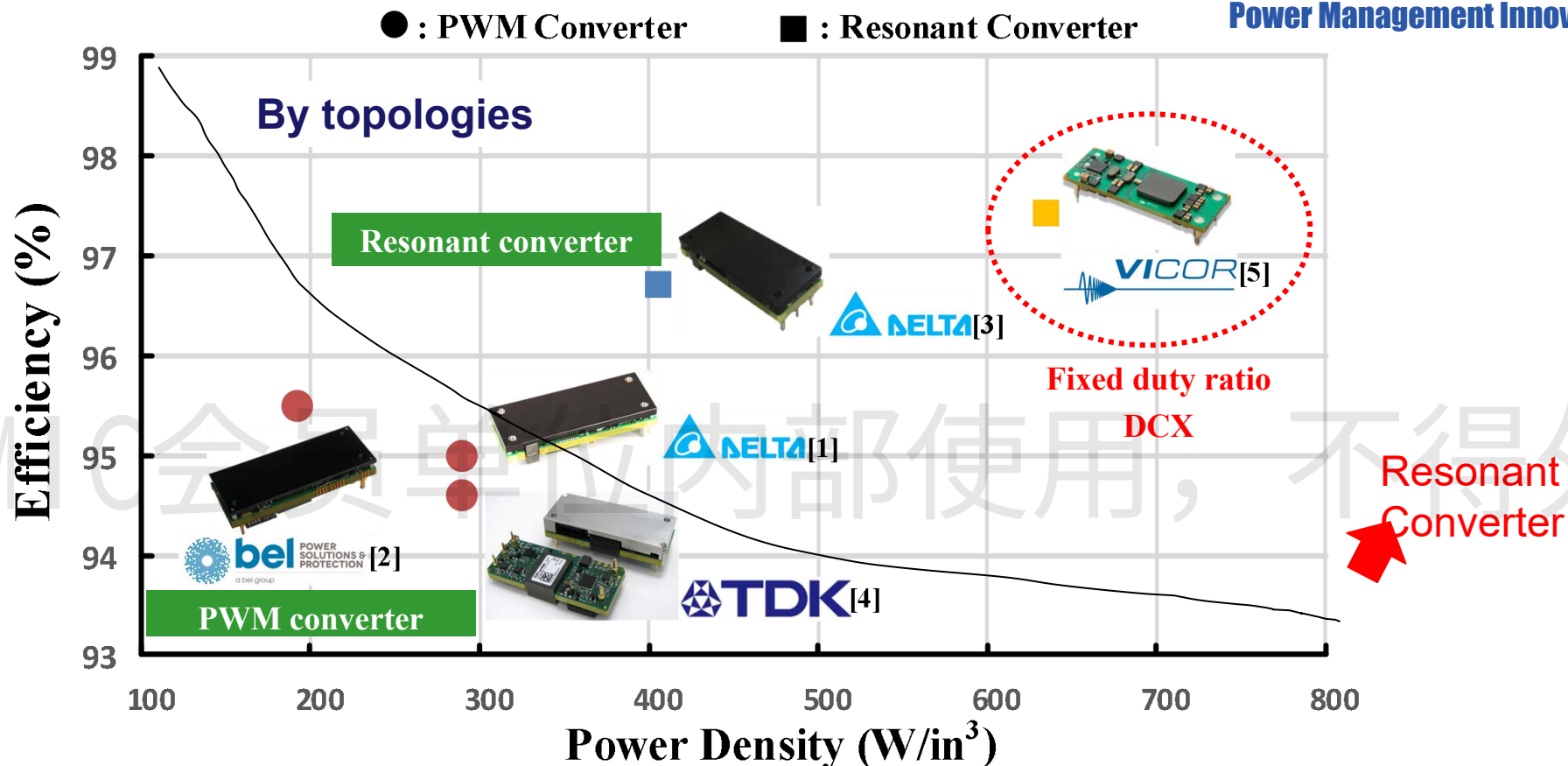
[3] M. H. Ahmed, et al., High-efficiency, High-density Isolated/Regulated 48V Bus Converter with a Novel Planar Magnetic Structure. APEC 2019.

[4] G. Li, et al. High Power Density 48–12 V DCX With 3-D PCB Winding Transformer. IEEE TPE, 2020. 35(2): p. 1189-1193.

[5] M. H. Ahmed, et al., Two-Stage 48V VRM With Intermediate Bus Voltage Optimization For Data Centers. IEEE JESTPE, 2020, Early Access



Open Frame 48V dc-dc Commercial Products



[1] E48SC12025, 2017, Delta

[2] ORCY-D4T12x, 2017, Belfuse

[3] E54SJ12040, 2017, Delta

[4] IEH48025A120V, 2013, Lambda-TDK

[5] IB0E120T400xx-xx, 2016, VICOR

Single-stage Converter with regulation capability:



- Limited power density
- Limited efficiency (<97%)

Conventional Resonant DCX Topology for 48V Applications

Power Management Innovation Consortium

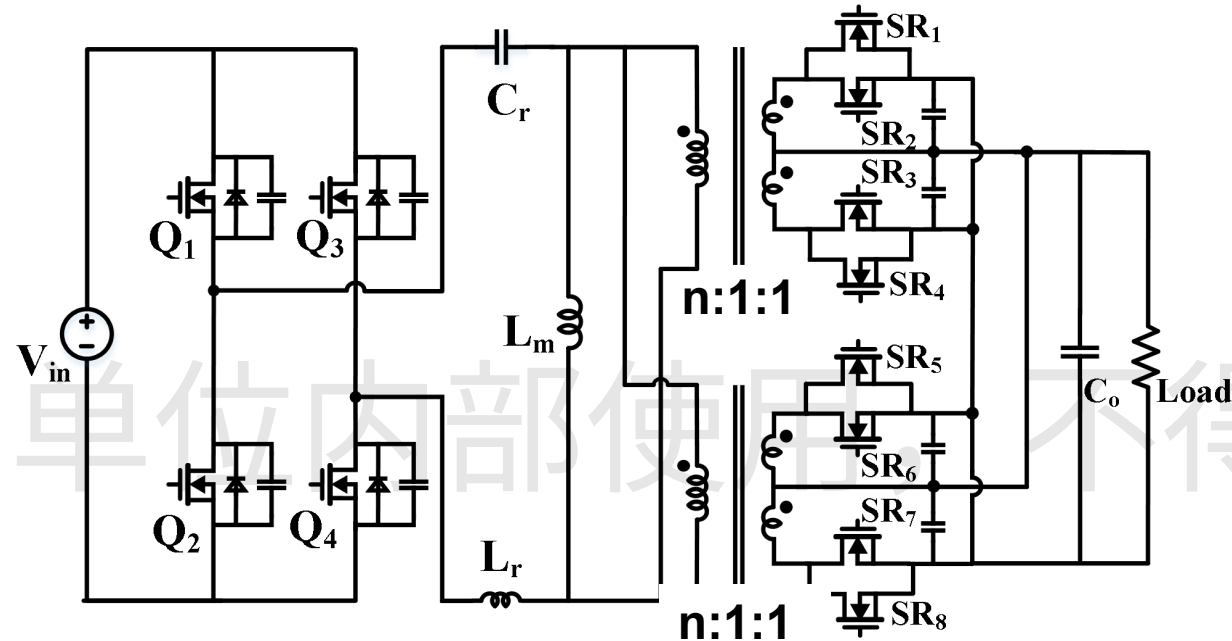
Resonant topology working at resonant frequency



DCX, GaN
48V/12V, 1.6MHz



DCX, GaN
48V/12V, 1MHz



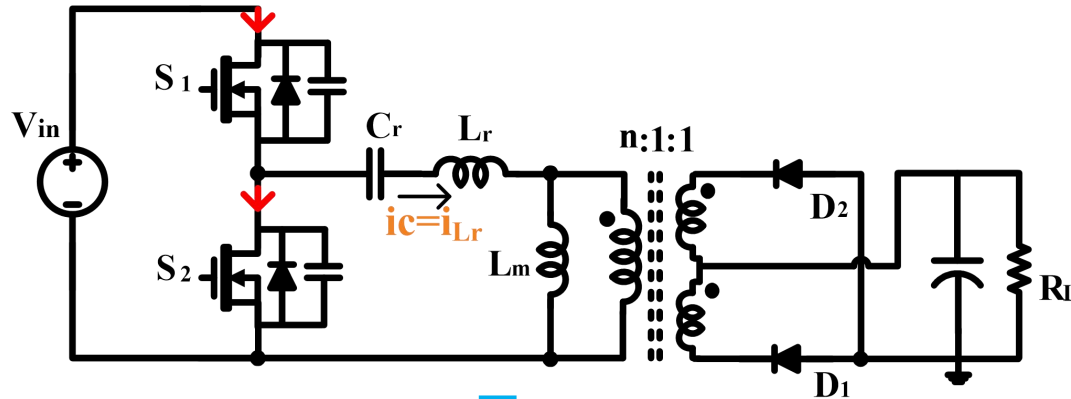
Features:

1. ZVS-on;
2. ZCS-off;
3. Only one magnetic device;
4. Optimized at fixed frequency.

- High efficiency
- High density
- Large amount of devices

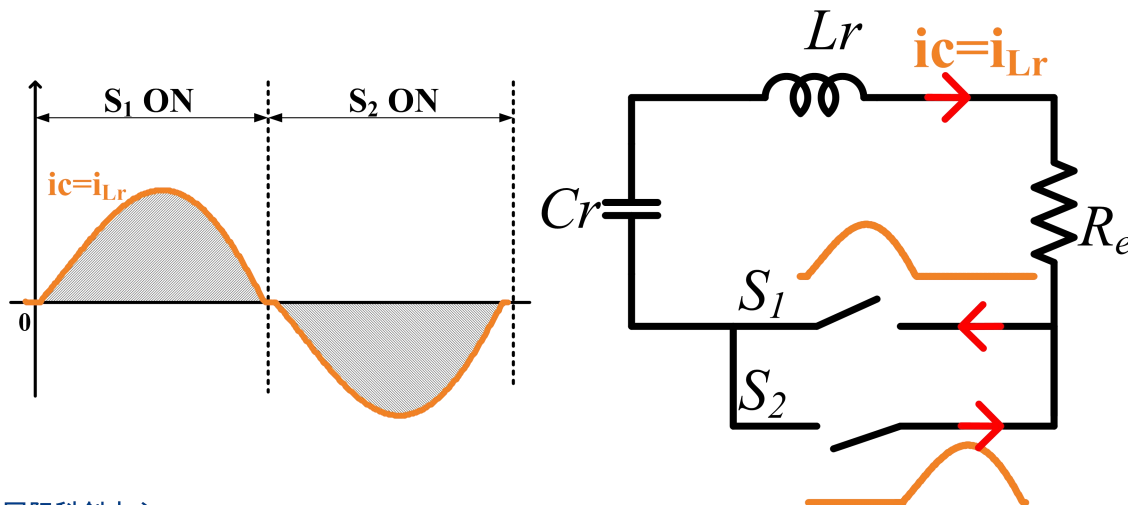


Bidirectional LLC Resonant Tank



Center tap rectifier
for LLC half bridge

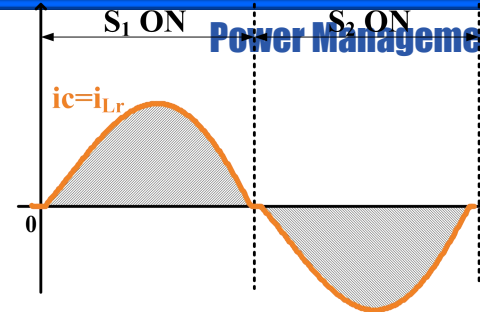
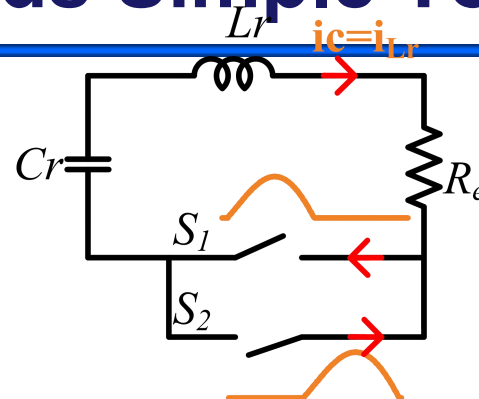
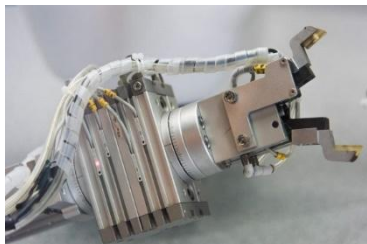
仅限PMIC会员单位内部使用，不得外传



Equivalent
Bidirectional resonant tank
derived from LLC converter

Low Power Applications Needs Simple Topology

Industry robotics



Bidirectional resonant tank

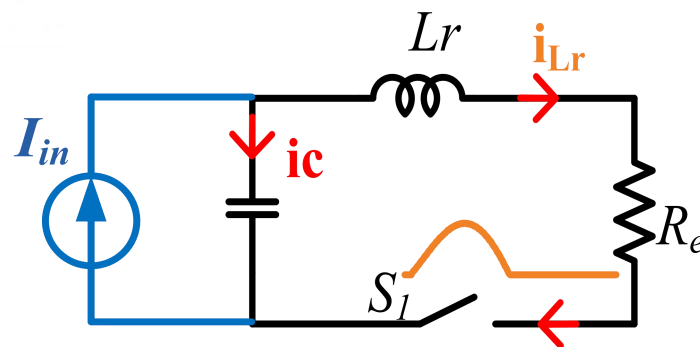
Telecom exchanger



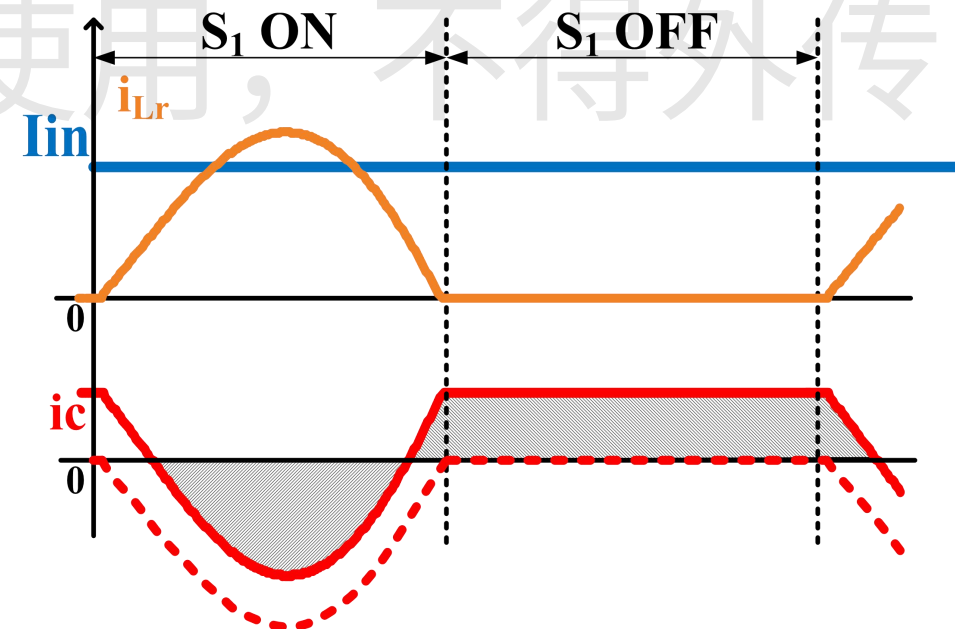
Bias & driver



Portable instruments

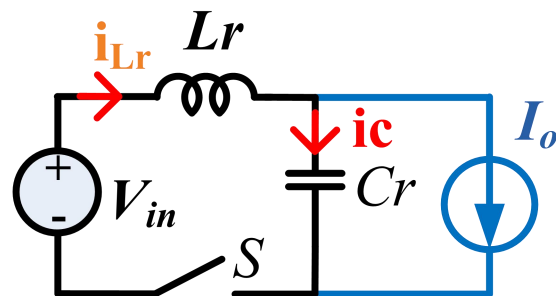
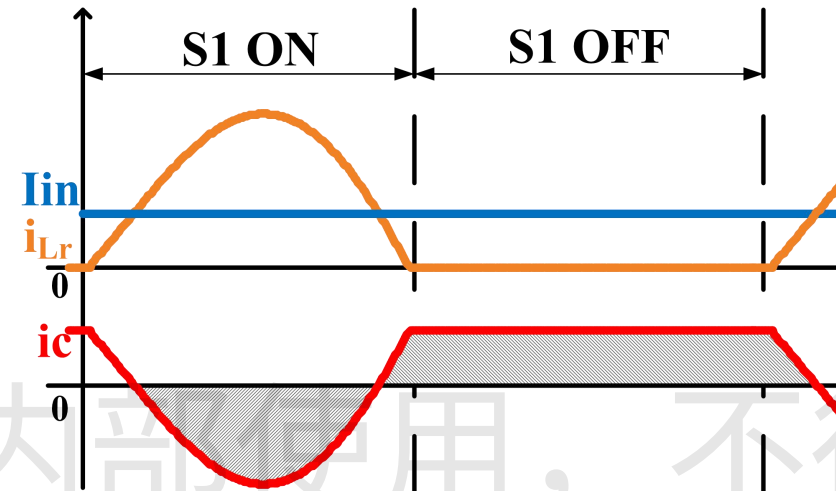
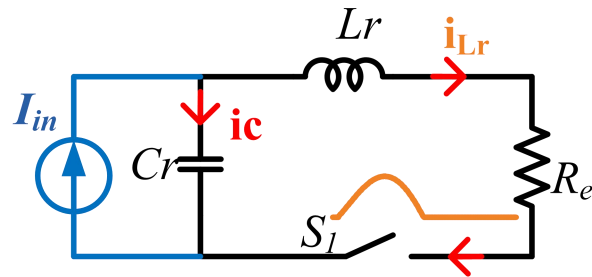


Proposed Unidirectional Resonant tank With DC current source

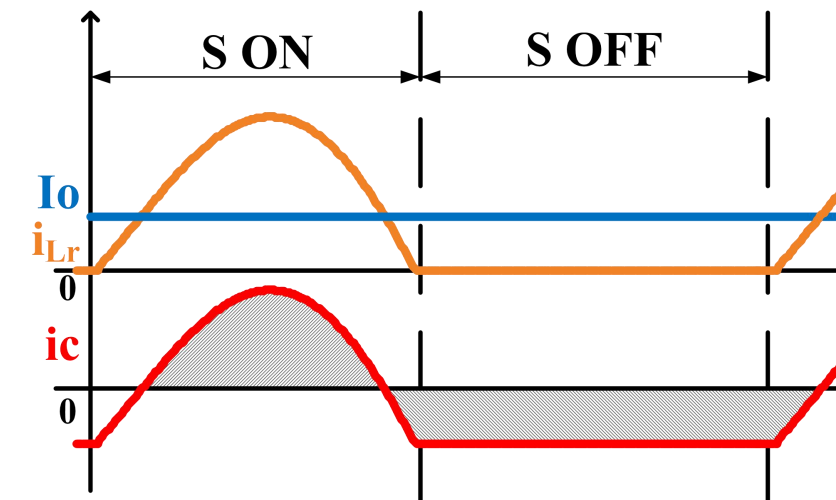


Two Types of Unidirectional Resonant Tank

Type I
Input current source

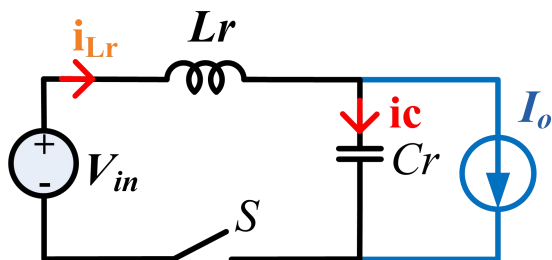
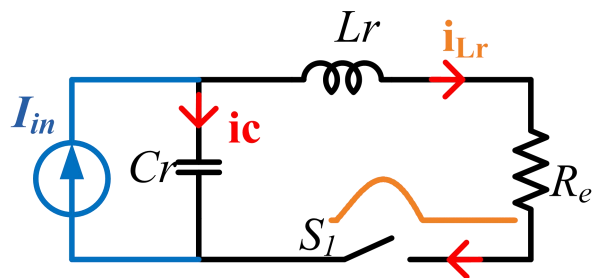


Type II
Output current source

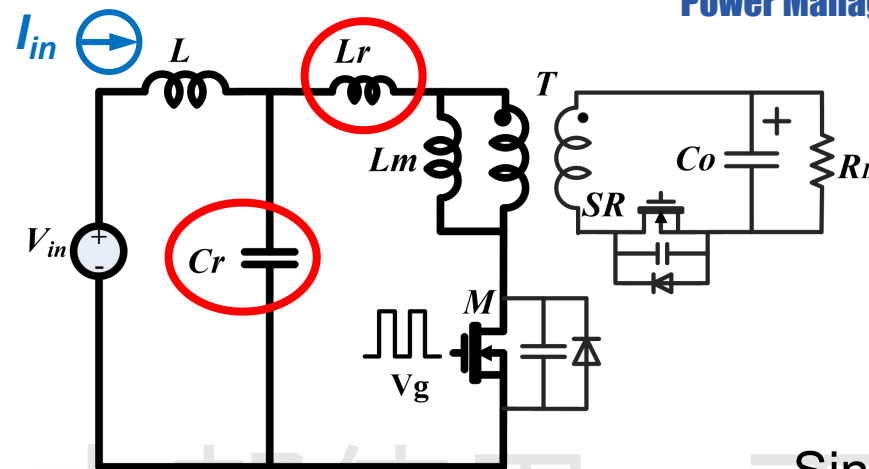


Derivation of single switch DCX topology with Unidirectional Resonant Tank

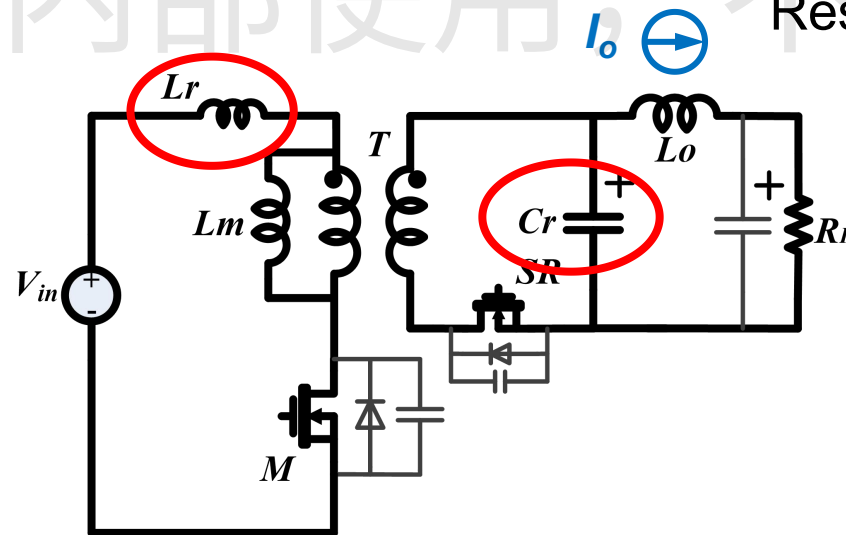
Type I
Input current source



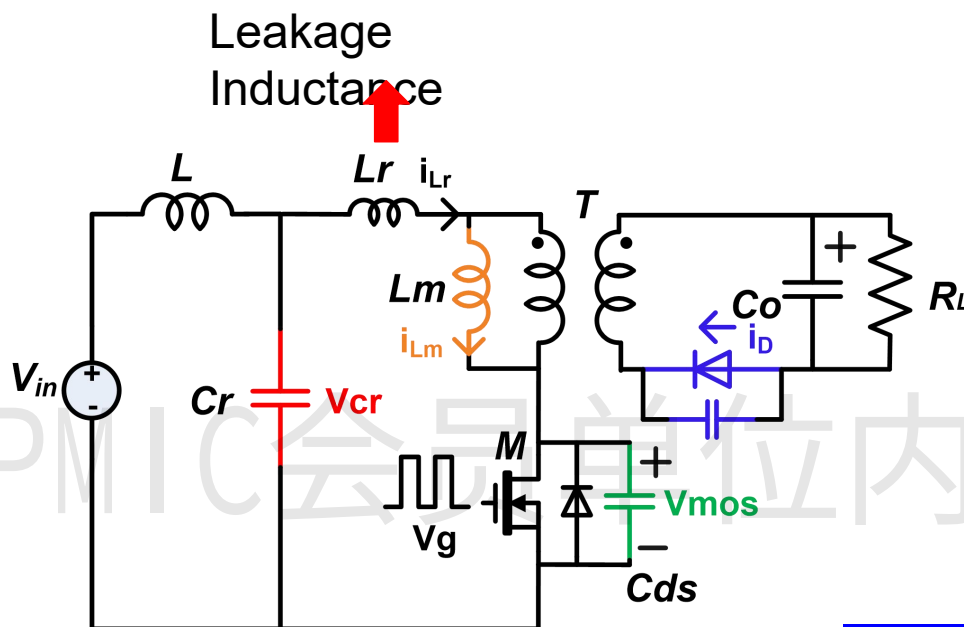
Type II
Output current source



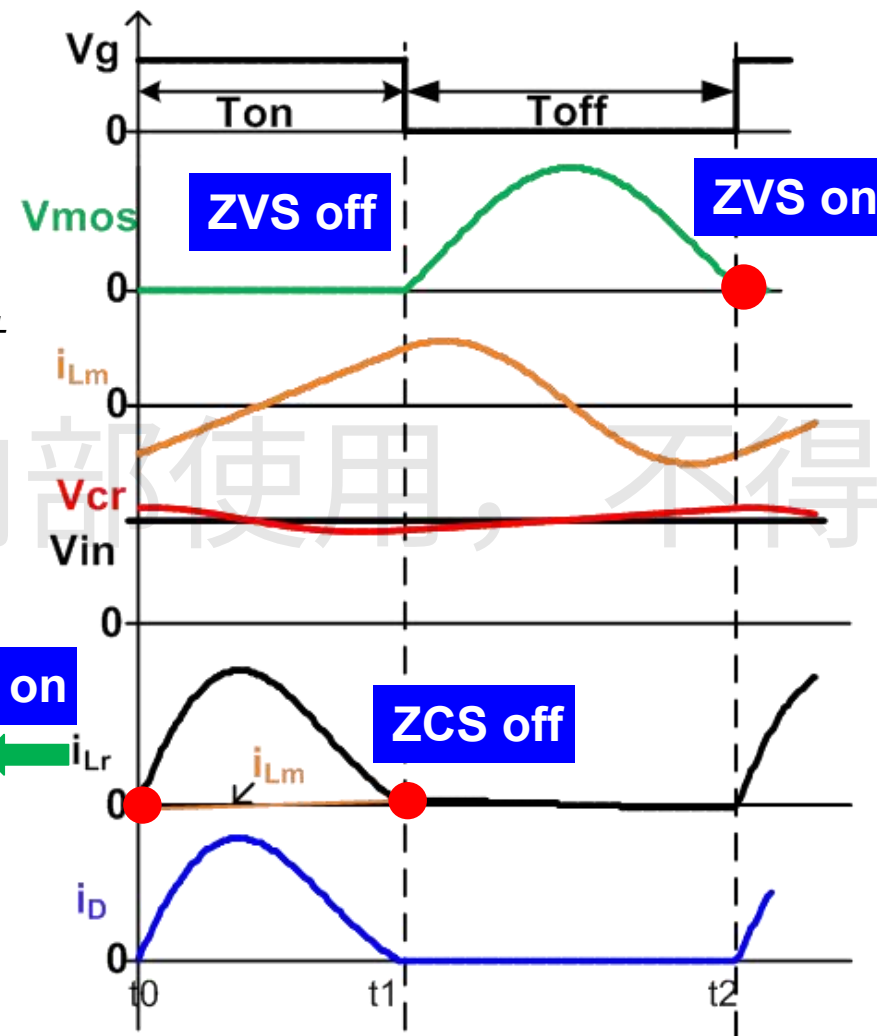
Single Switch Forward
Resonant DCX



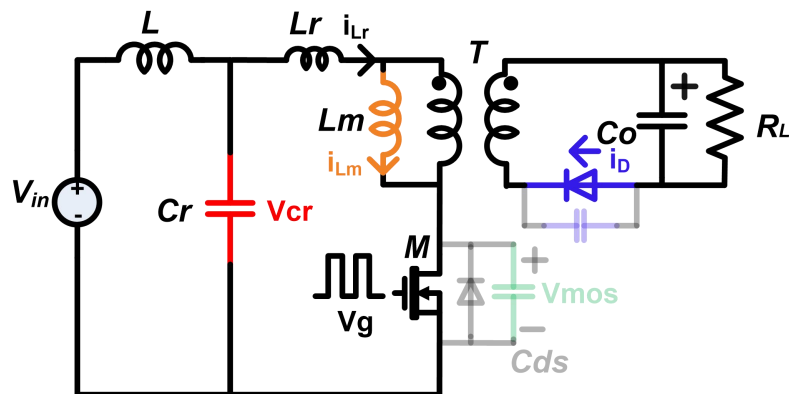
Operation of ZVZCS Forward DCX



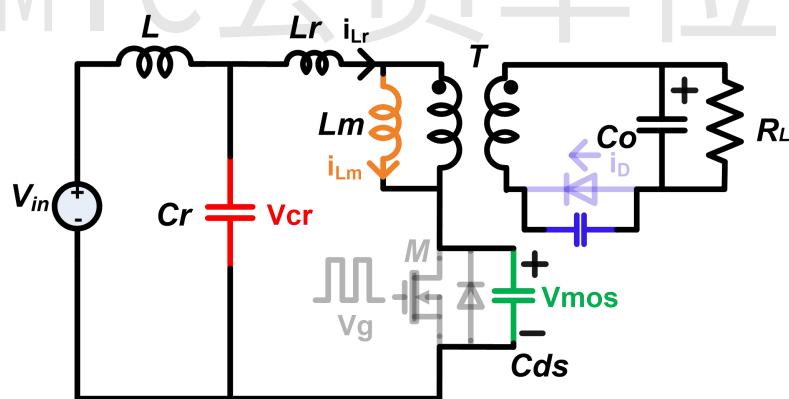
- ☺ Very simple.
- ☺ Very good ZVZCS.
- ☺ High frequency operation



Two Operation Mode for the Forward DCX

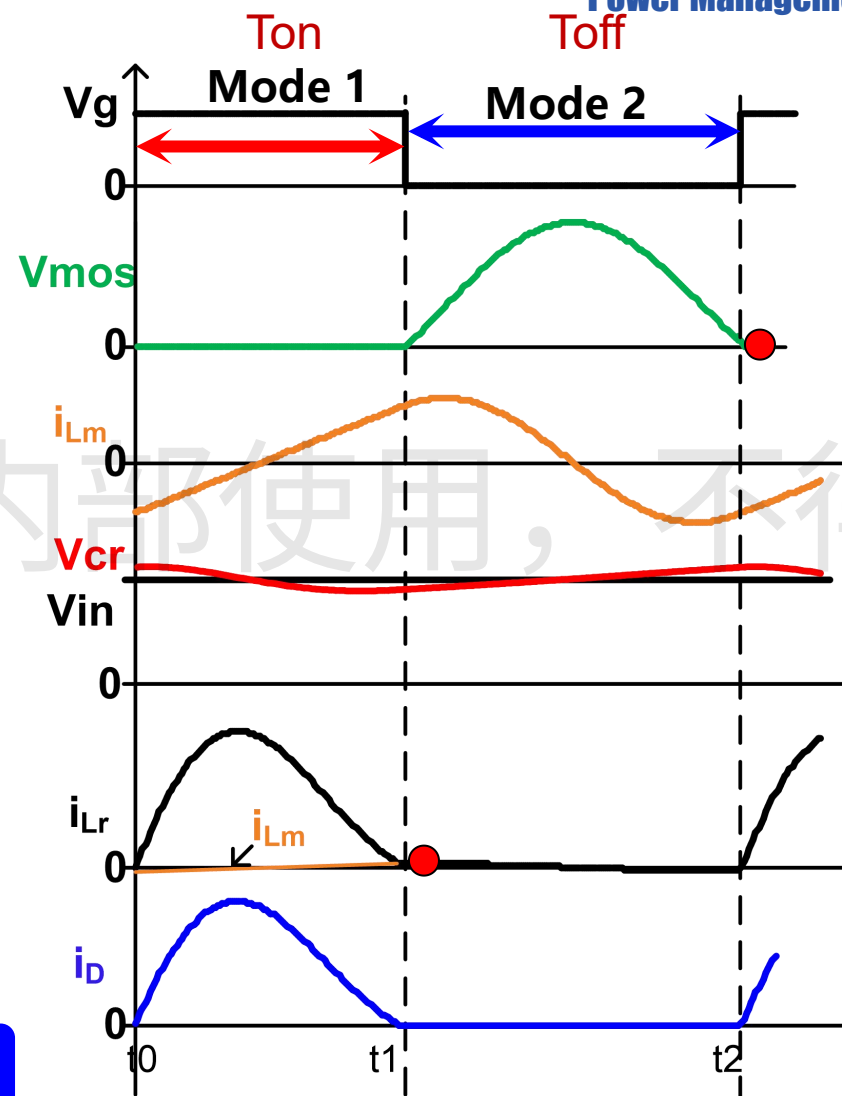


Mode 1



Mode 2

☺ ZVZCS operation



How to determine the Ton and Toff?

Relationship between Ton and Toff

(1) ZCS
Condition of switch

$$i(T_{on}) = 0$$

Neglecting the
magnetizing current

The equation between Ton and Toff

$$T_{off} = -\frac{\sin \omega T_{on}}{\omega} - \frac{(\cos \omega T_{on} - 1)^2}{\omega \sin \omega T_{on}}$$

$$v_{mos}(T_{off}) = 0$$

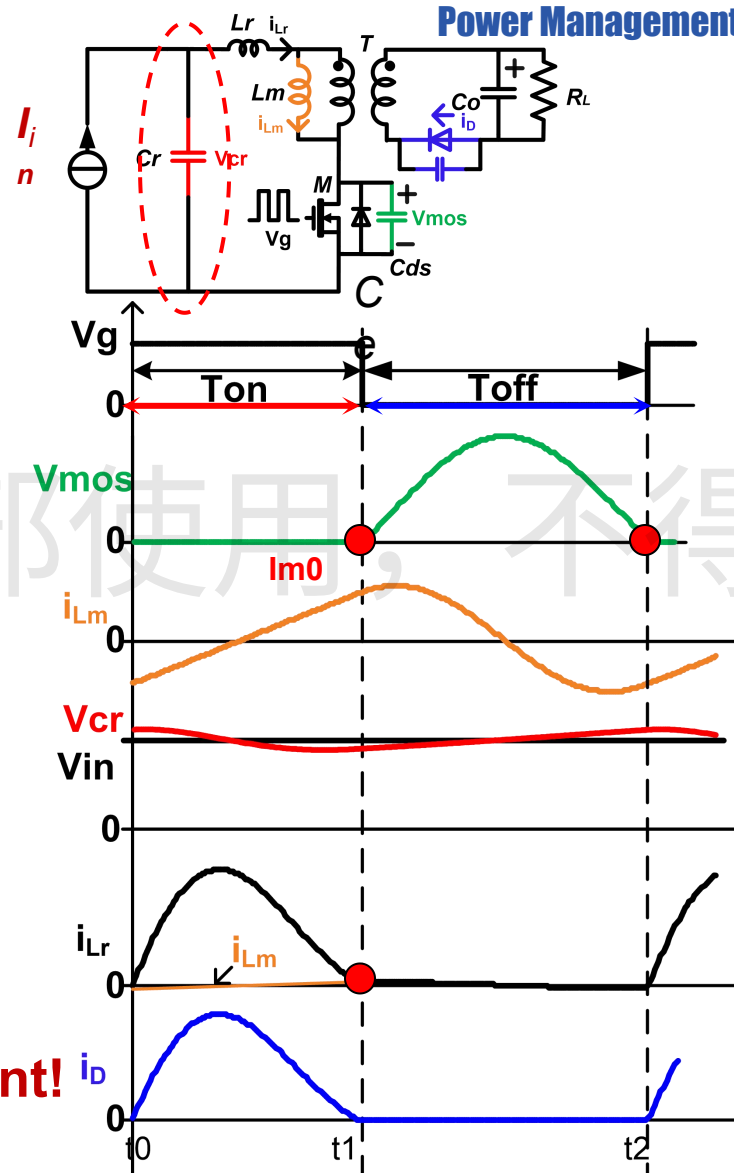
$$I_{m0} = V_{in} \cdot T_{on} / 2$$

$$\omega = 1/\sqrt{L_r C_r}$$

Soft switching is Load independent!

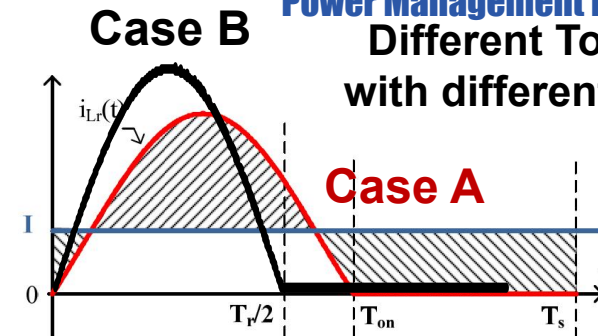
(2) Charge balance
during switching cycle

$$I_{in} \cdot (T_{on} + T_{off}) = \int_0^{T_{on}} i_{Lr} dt$$



Low Duty Cycle will cause High Current Stress

Different Ton
with different Cr



For given Cr, Lr, Lm, Ce and Vin

Calculate Ton according to $v_{mos}(T_{off}) = 0$

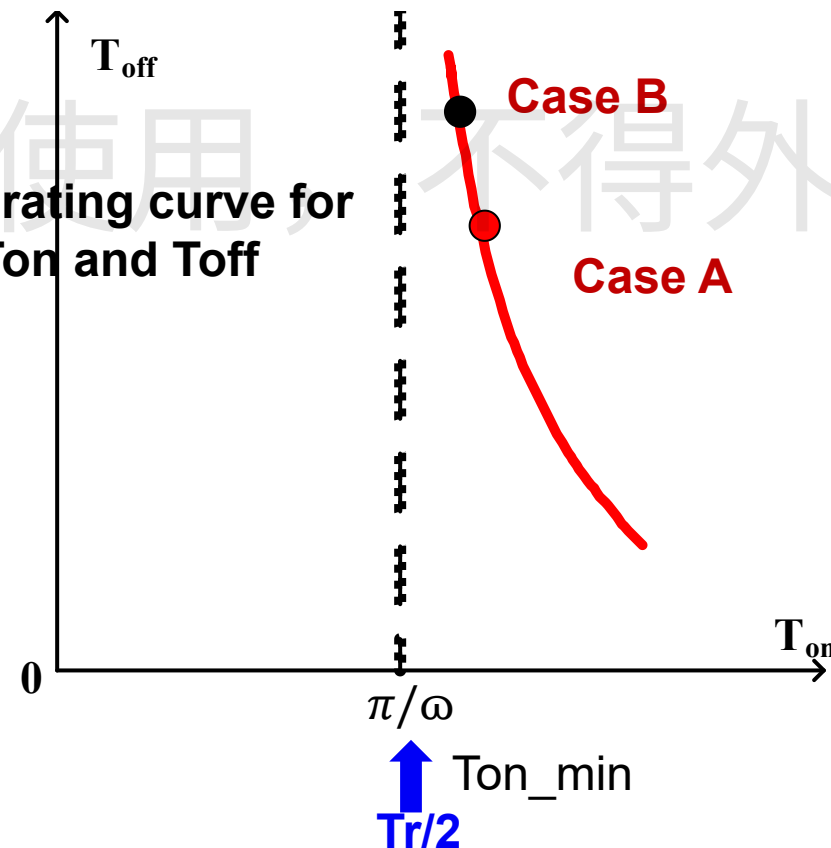
$$T_{on} = \frac{2(\cos \omega_1 T_{off} - 1)}{\omega_1 \sin \omega_1 T_{off}} \quad \omega_1 = 1 / \sqrt{(L_r + L_m)C_e}$$

D and f definition:

$$D = T_{on} / (T_{on} + T_{off})$$

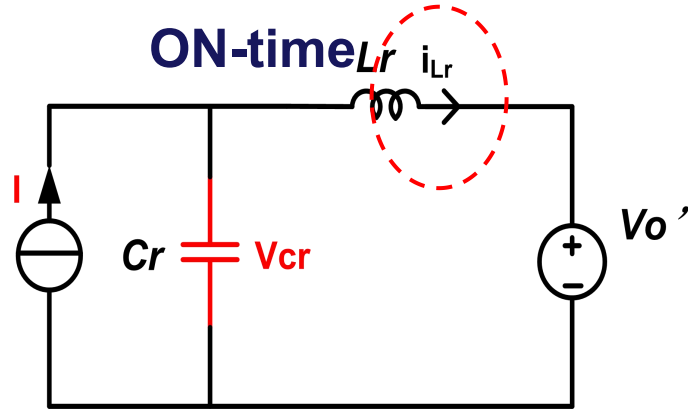
$$f_s = 1 / (T_{on} + T_{off})$$

Operating curve for
Ton and Toff



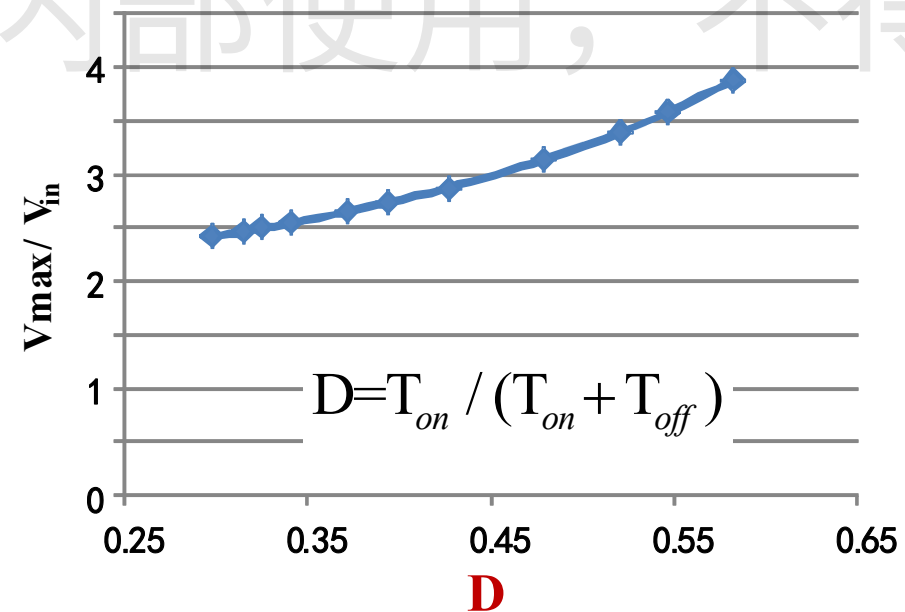
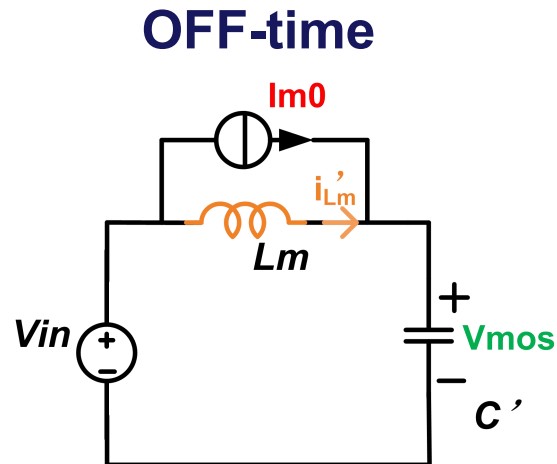
High Duty Cycle will Lead to High Device Voltage Stress

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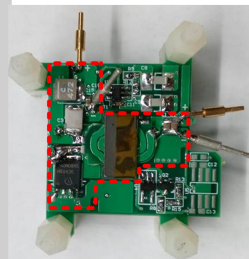
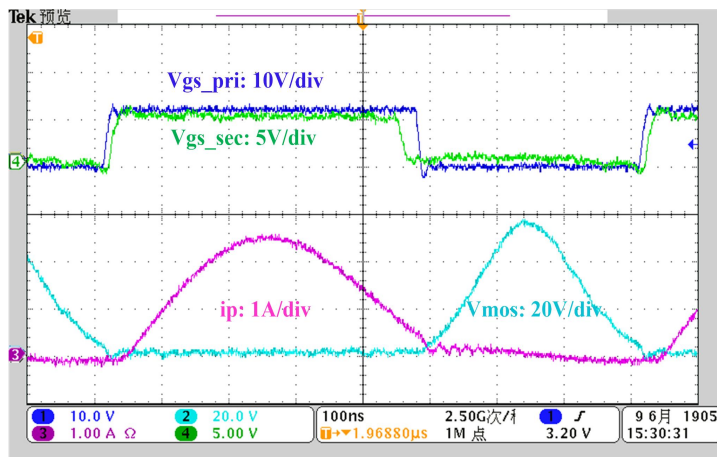
$$V_{mos_peak} \approx V_{in} + V_{in} \sqrt{\frac{k^2 \pi^2}{4} \left(\frac{T_{on}}{T_{off}} \right)^2 + 1}$$

$$= V_{in} + V_{in} \sqrt{\frac{k^2 \pi^2}{4} \left(\frac{D}{1-D} \right)^2 + 1}$$

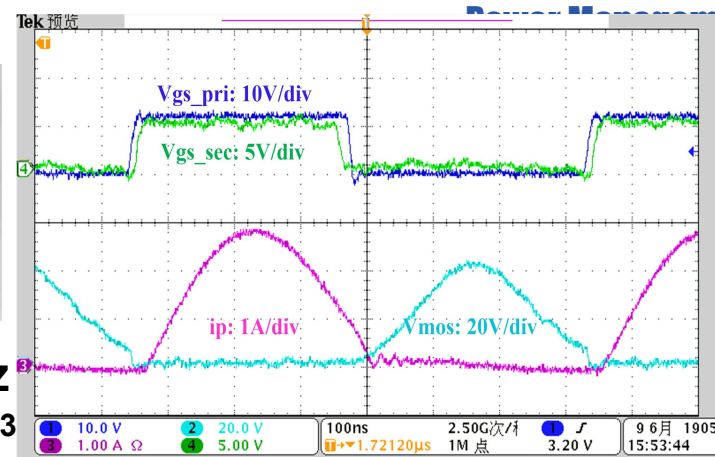


Calculated Voltage Stress

Measured Waveforms at Different D

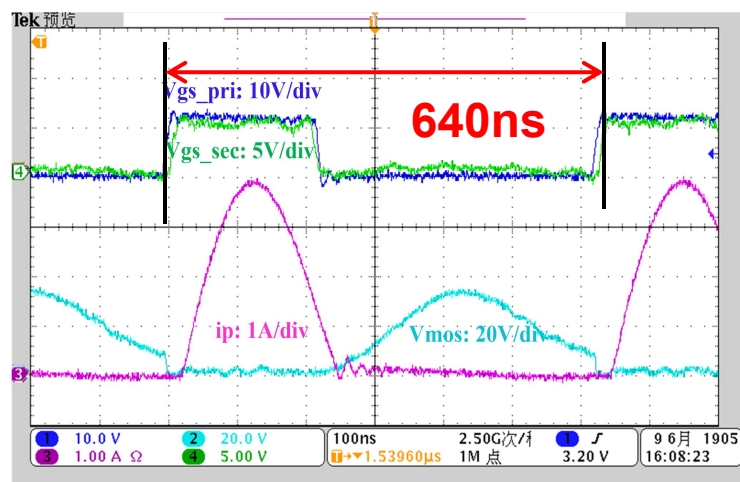


@ 1.6MHz
~150 W/in³
Up to 96%



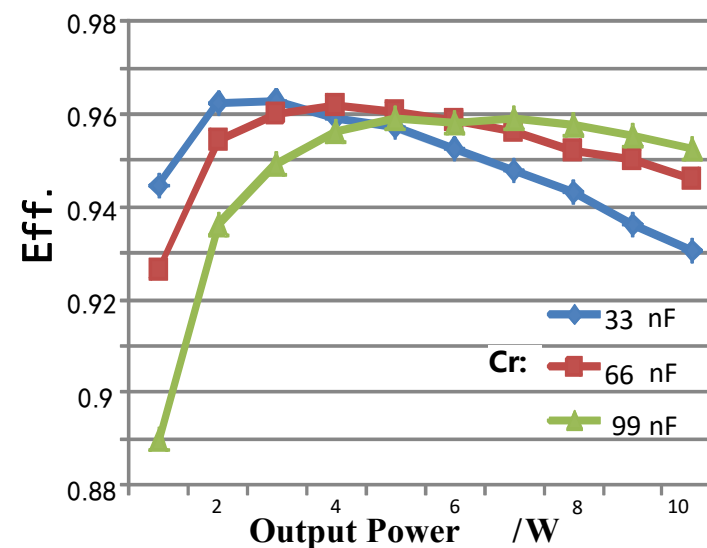
Cr=66nF, fs=1.45MHz

- High D, high Vmos, low Irms



Cr=33nF, fs=1.6MHz

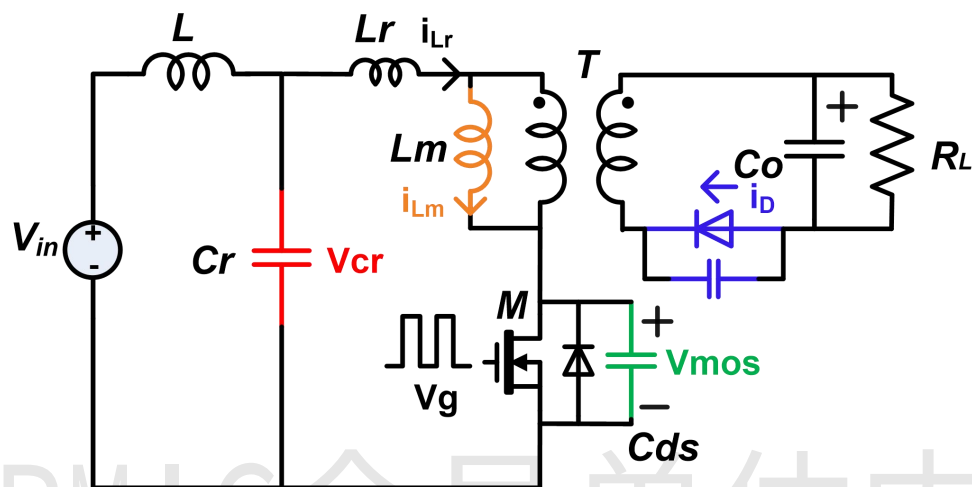
- Low D, low Vmos, high Irms



Input 12V
Output 5V/2A



Limitation of Single Switch Forward DCX



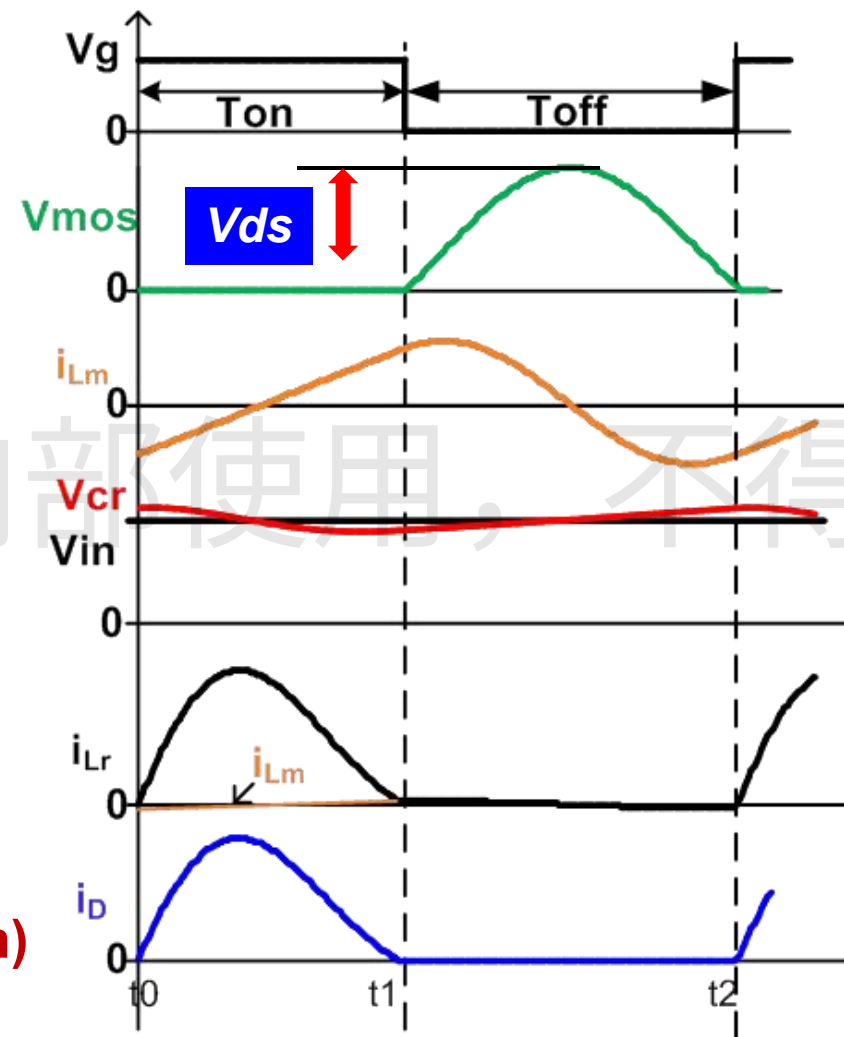
Advantages:

- ZVZCS operation.



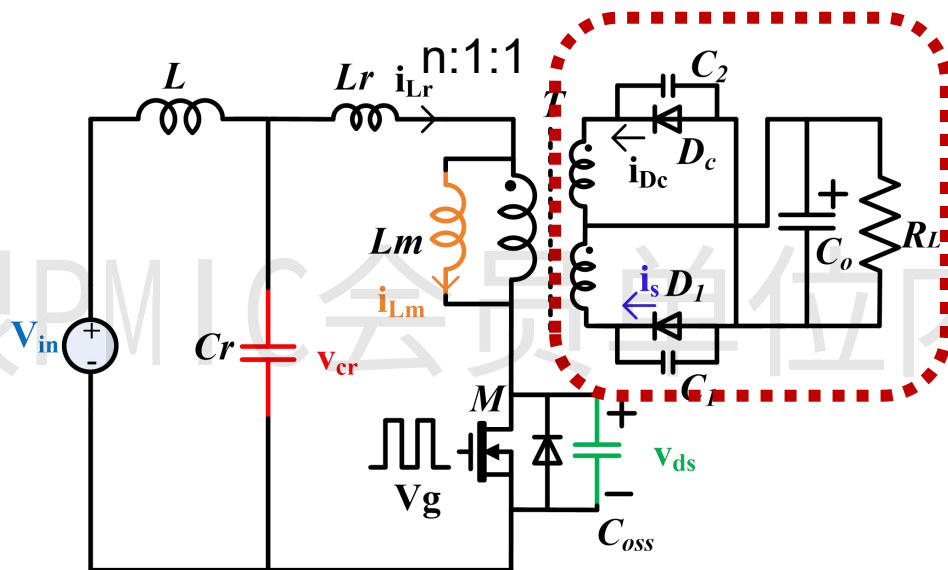
Disadvantages:

- High voltage stress (at least $3 \cdot V_{in}$)



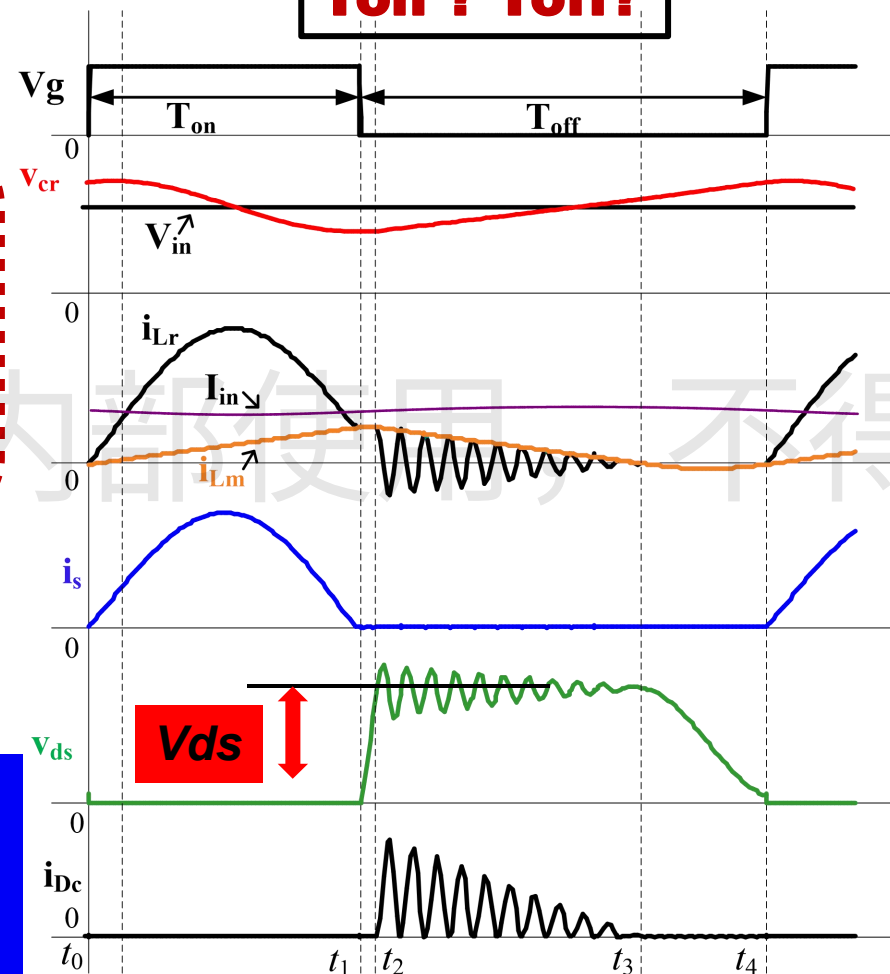
Secondary Clamping of Single Switch DCX

□ Reduce the voltage stress



- ✓ Less Turns
- ✓ Magnetizing energy transfer to load
- ✓ Keep ZVZCS

Ton ? Toff?



Frequency (f_s) & Duty Cycle (D)

□ Given : L_r , C_r , L_m , C_e

ZCS off $T_{off}-T_{on}$ conditions

$$T_{off} = -\frac{\sin \omega T_{on}}{\omega} - \frac{(\cos \omega T_{on} - 1)^2}{\omega \sin \omega T_{on}}$$

ZVS on

$$T_{off} = T_{on} + \Delta t_2 + \Delta t_4$$

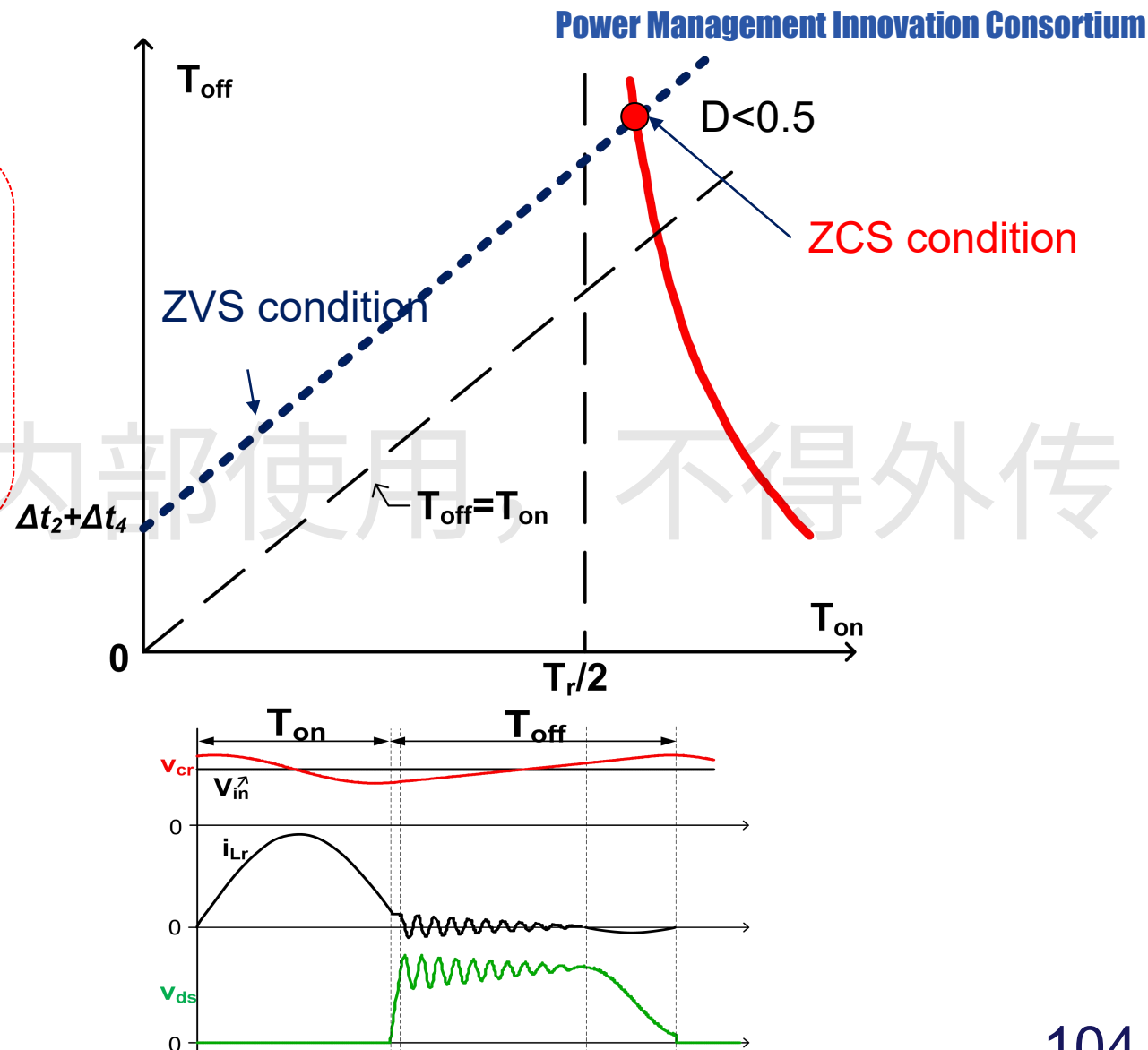
➤ Duty cycle and f_s :

$$D = T_{on} / (T_{on} + T_{off})$$

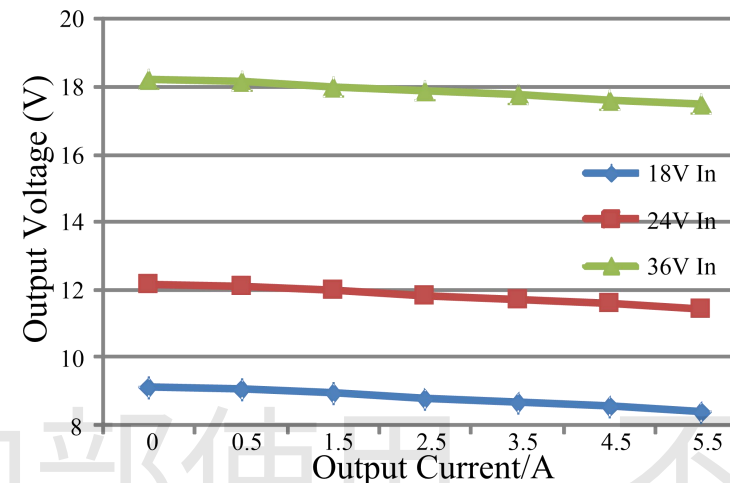
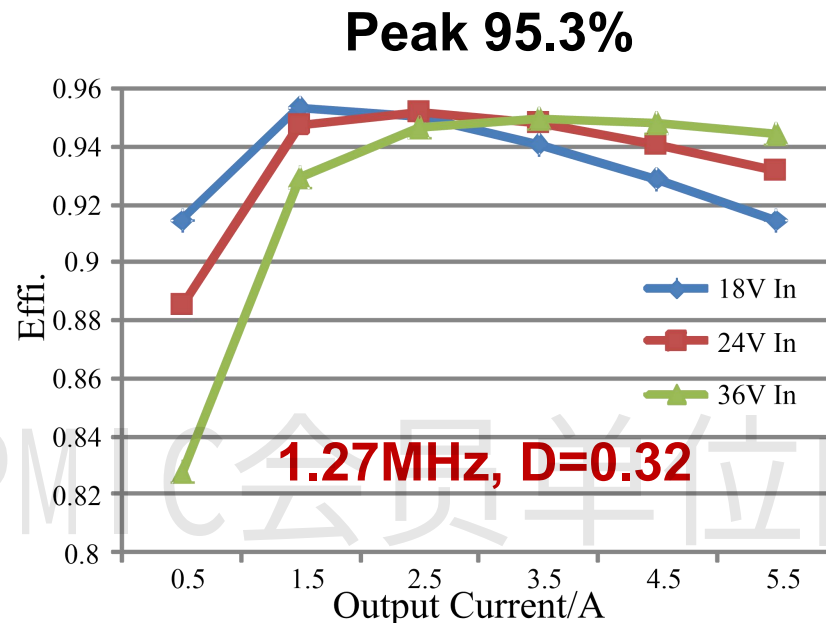
$$f_s = 1 / (T_{on} + T_{off})$$

✓ Simple control and drive

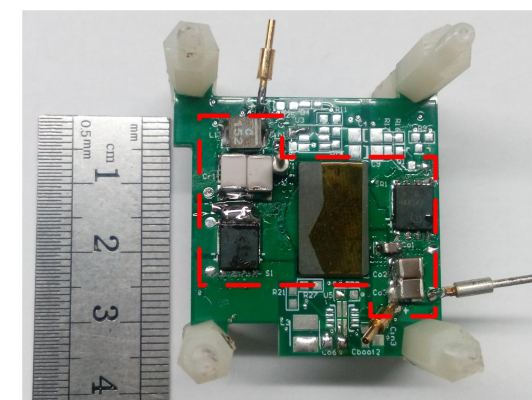
✓ ZVZCS



Measured Efficiencies at different input voltages



Po: 66Watt @24V Vin
fs: ~1.2MHz
Efficiency : 95.3%

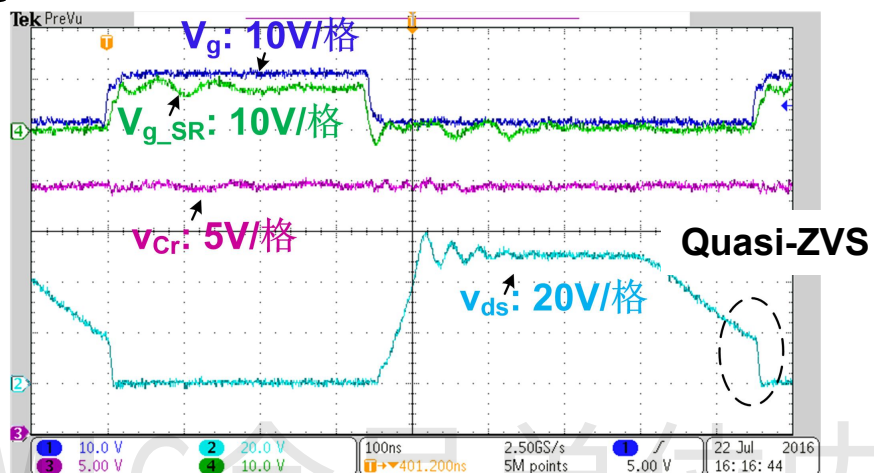


Power density: ~270W/in³

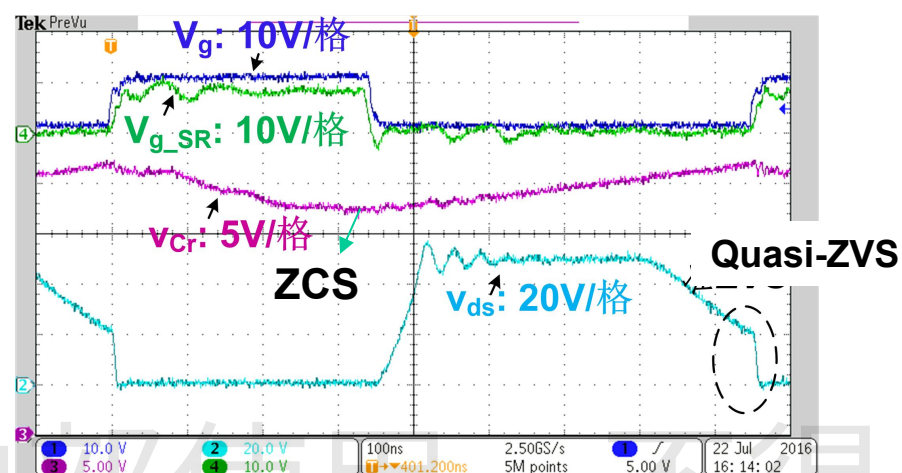
Vin	18~36V
Transformer	2:1:1
Cr	300nF

Experimental verifications

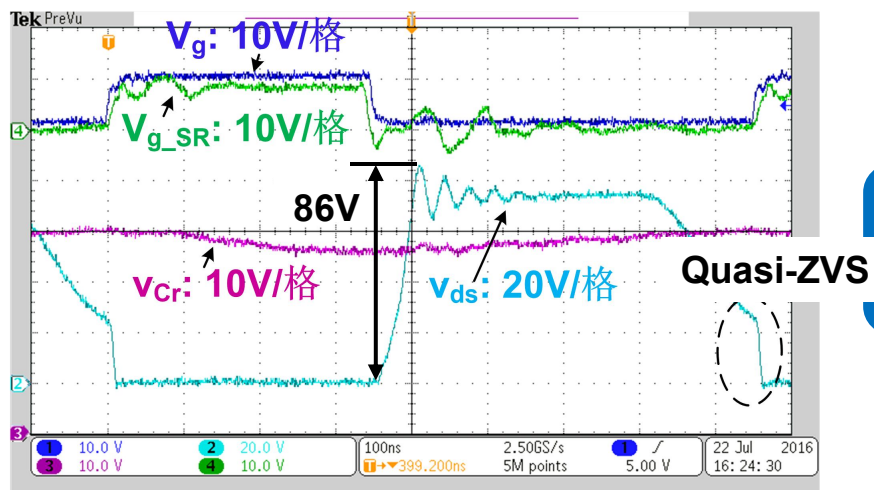
➤ @1.18MHz D=0.4



24V Vin, Null load



24V Vin, full load, $I_o=5.5A$



36V Vin, $I_o=5.5A$

ZVZCS in full voltage and load ranges

□ Stress: $2.4 \cdot V_{in}$

ZVS on for all switches

- 107

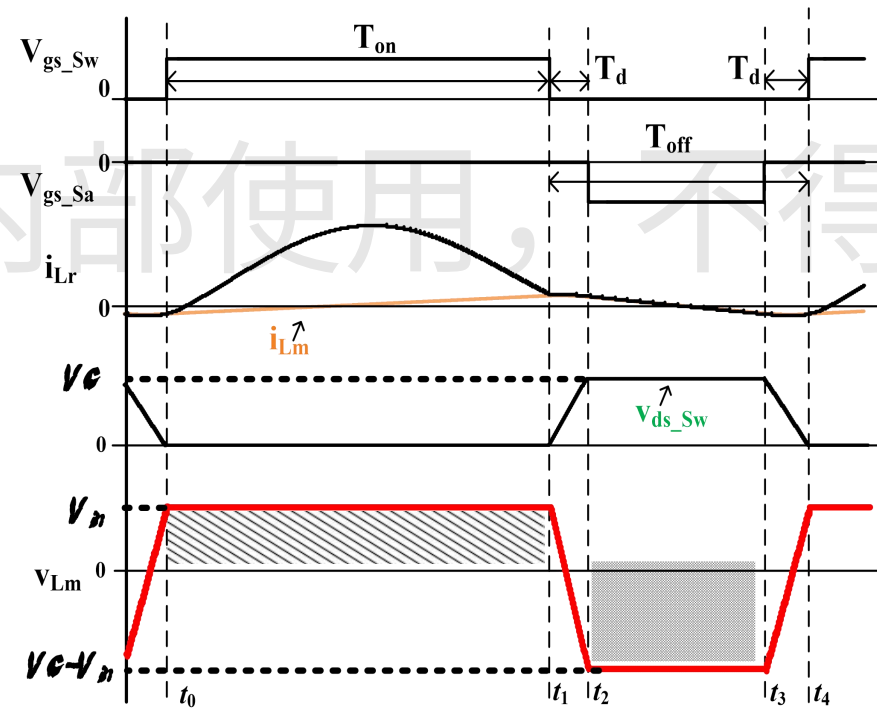
ON-OFF Relationship (ZVS on)

Lm volt-second balance @Vin_max & estimated large D

$$\frac{V_c}{V_{in}} = \frac{T_{on}}{T_{off} - 2T_d} + 1 \approx 1 / (1 - D)$$

Given:
 T_d, V_{c_max}

$$T_{off} = \frac{V_{in_max} \cdot T_{on}}{V_{c_max} - V_{in_max}} + 2T_d$$



*Neglect voltage ripple of Vc

Determine Maximum Duty Cycle using Device Voltage Stress

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ZCS condition

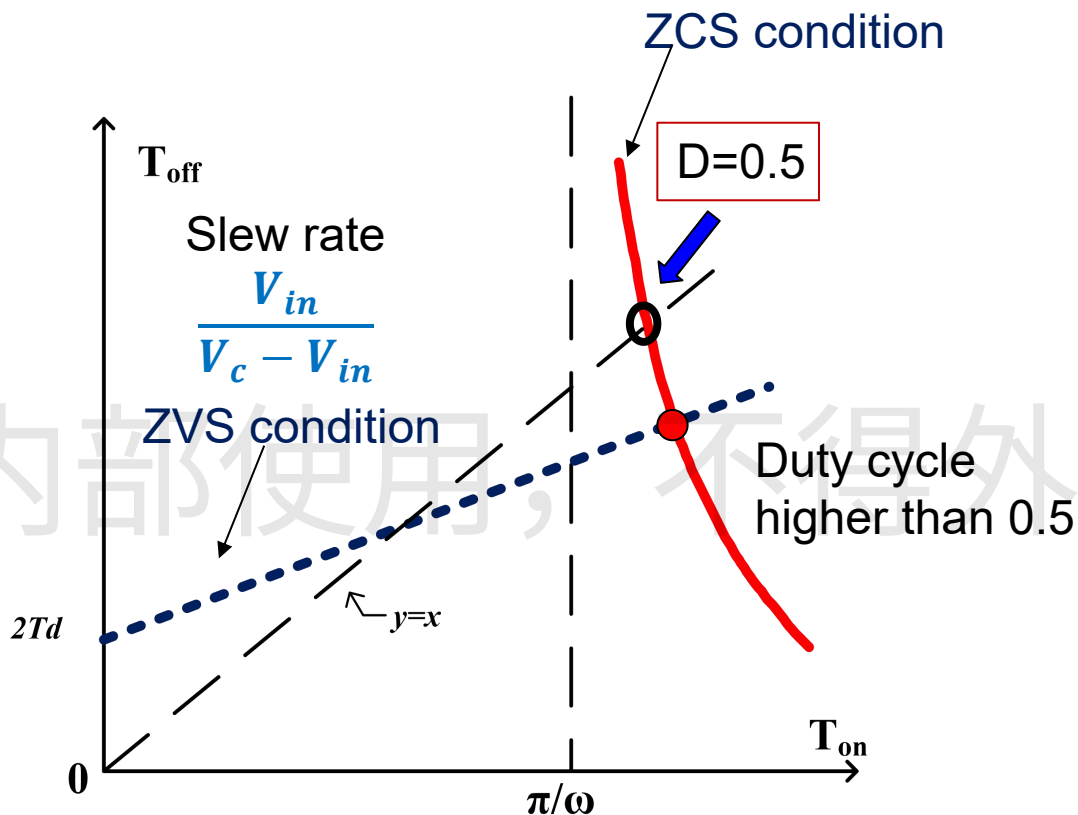
$$T_{off} = -\frac{\sin \omega T_{on}}{\omega} - \frac{(\cos \omega T_{on} - 1)^2}{\omega \sin \omega T_{on}}$$

ZVS condition

$$T_{off} = \frac{V_{in_max} \cdot T_{on}}{V_{c_max} - V_{in_max}} + 2T_d$$

$$D = T_{on} / (T_{on} + T_{off})$$

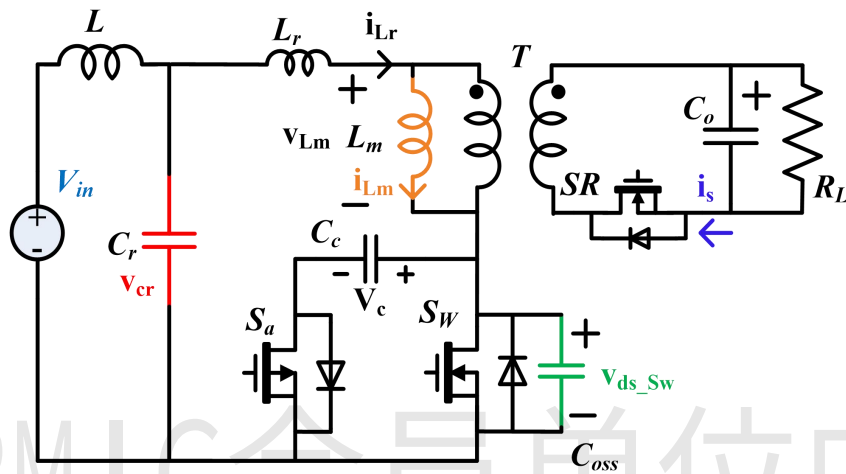
$$f_s = 1 / (T_{on} + T_{off})$$



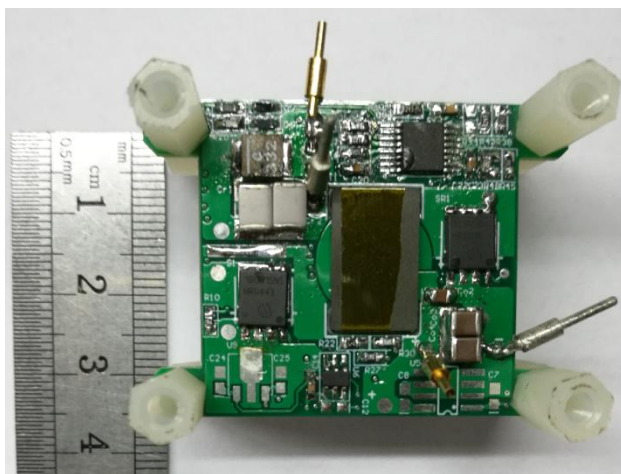
□ ZCS off and ZVS on are both load independent



Key parameters of ACF Prototype



<i>Prototype parameters</i>	
N-channel MOSFET	BSC190N15NS
P-channel MOSFET	FDMC86259P 150V-137m- 20nC
Secondary SR	BSC052N08NS
Transformer	EC14.5C/ Turns ratio: 2:1
Resonant Capacitor	141nF

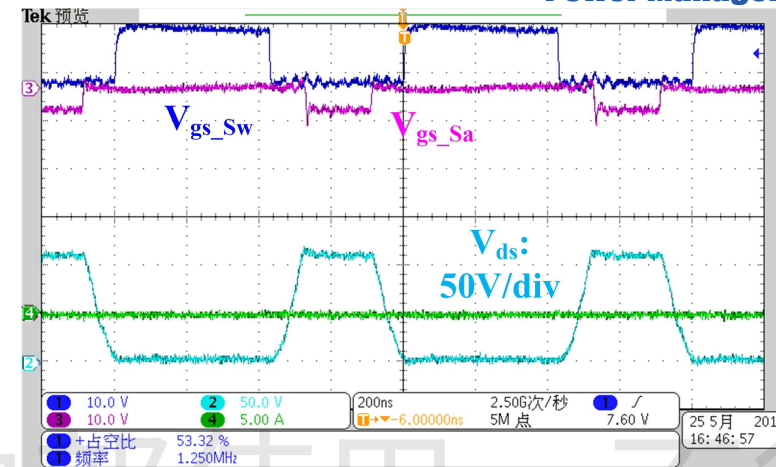
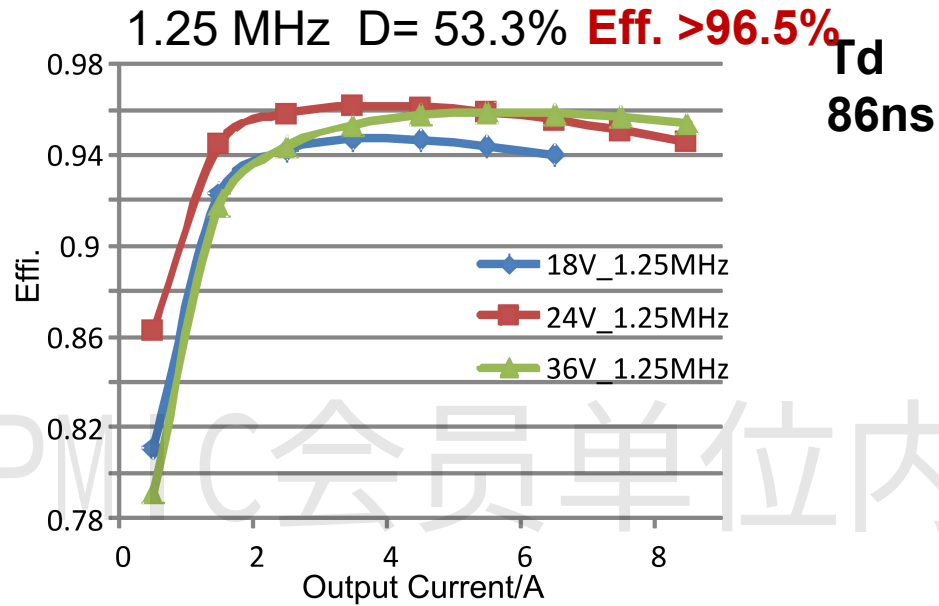


f_s : 1.25MHz

D : 53.3%

Efficiency: >96.5%

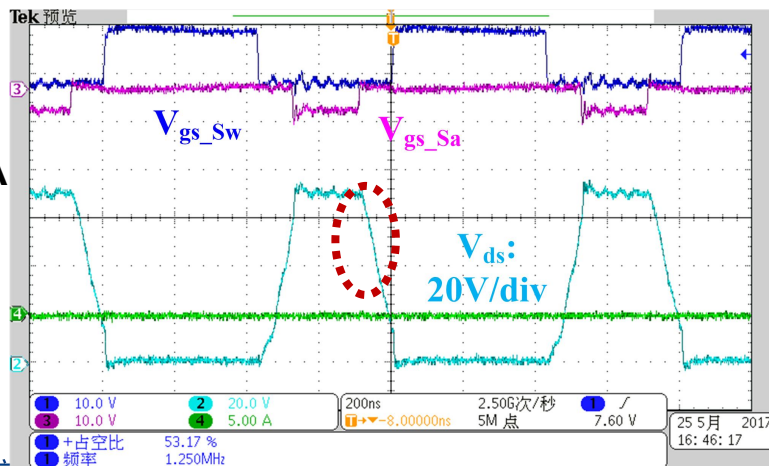
Measured waveforms at Fixed T_{on} , T_{off} and T_d



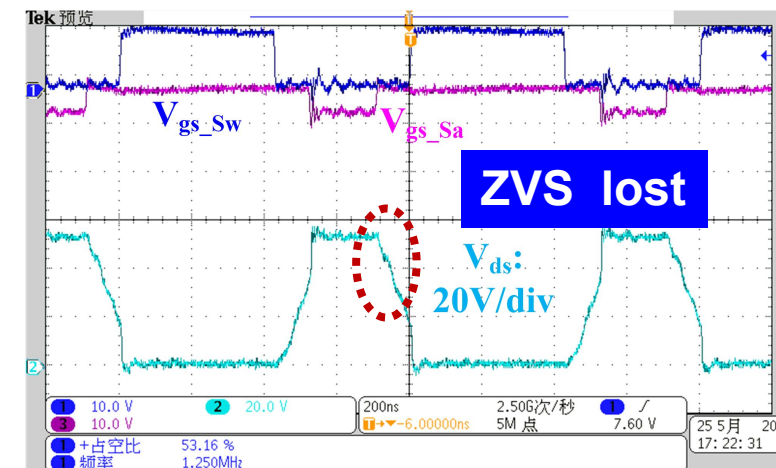
36V In, $I_o=5.5A$

Fixed t_d

24V In, $I_o=5.5A$

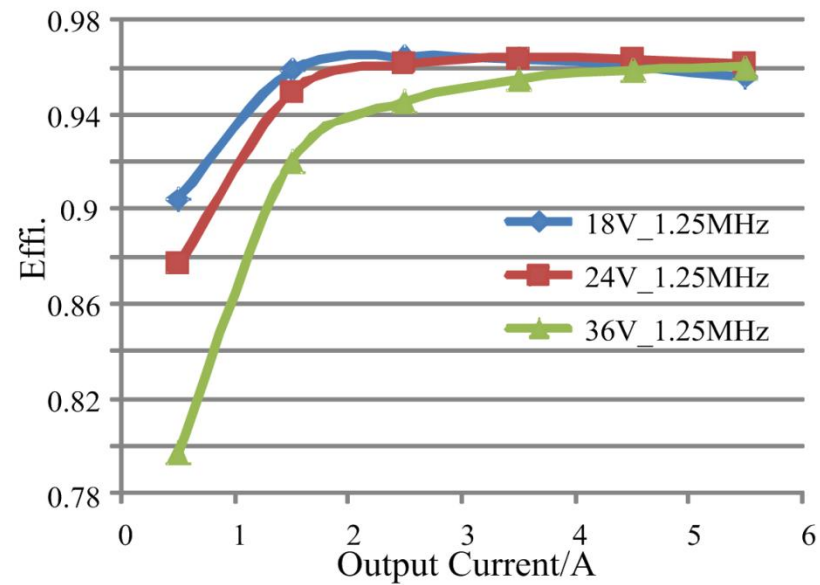
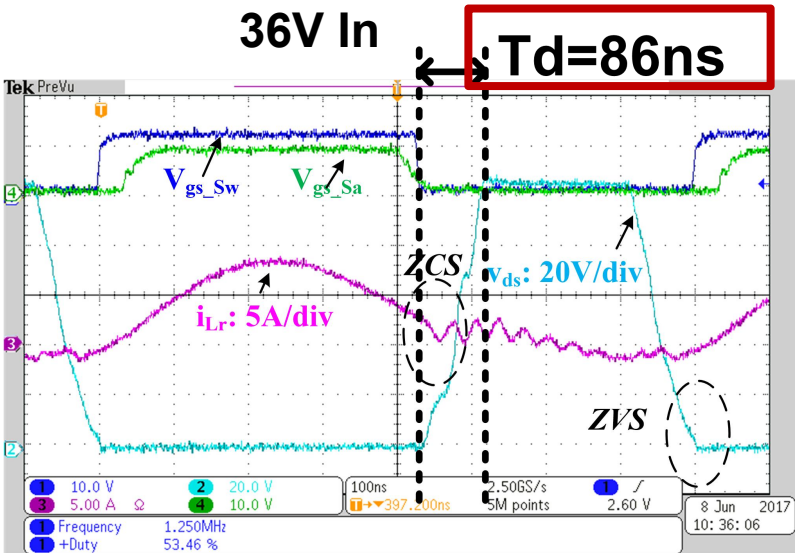
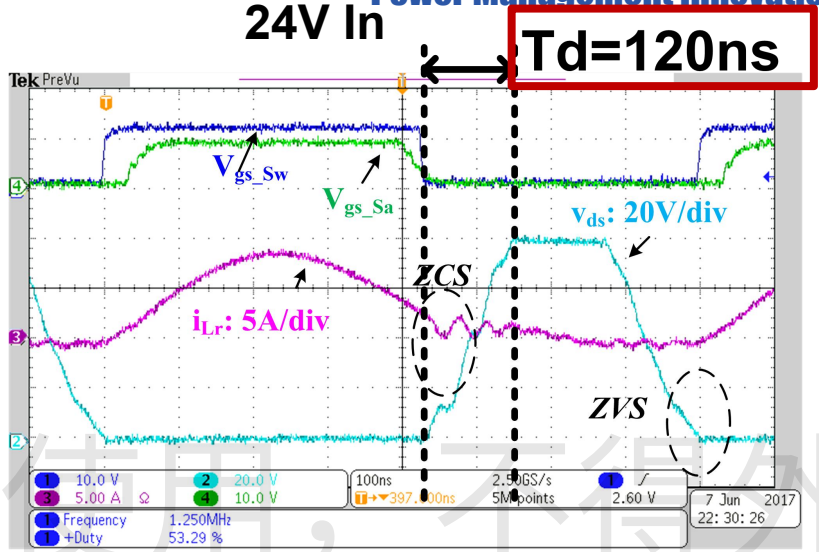
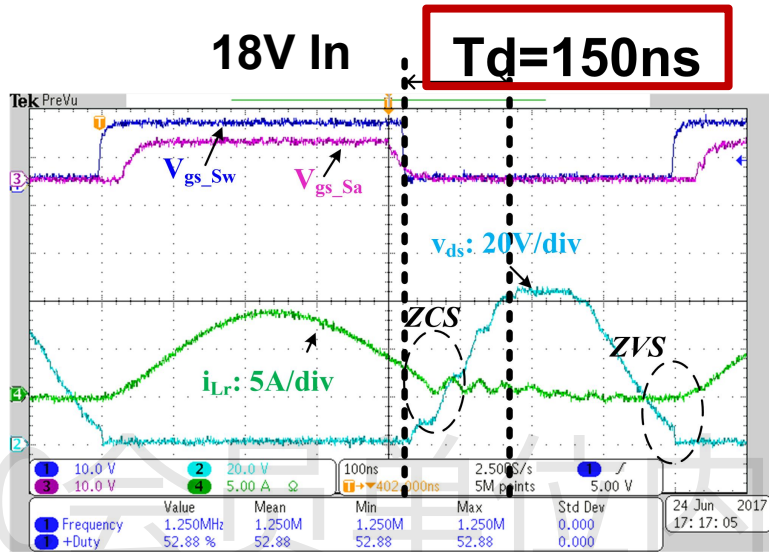


T_d 86ns

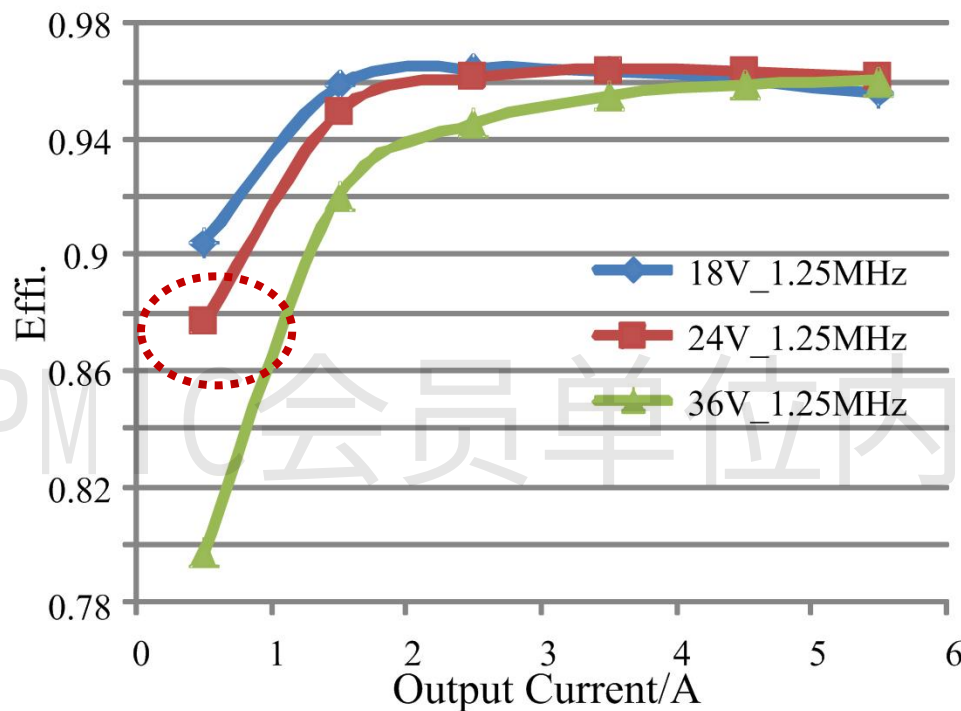


18V In, $I_o=5.5A$

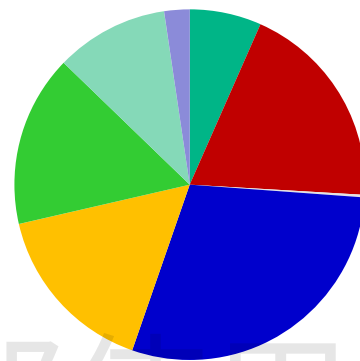
Adaptive dead time (T_d) control to Achieve Full Range ZVS



Light load efficiency deteriorate with Fixed **Ton**

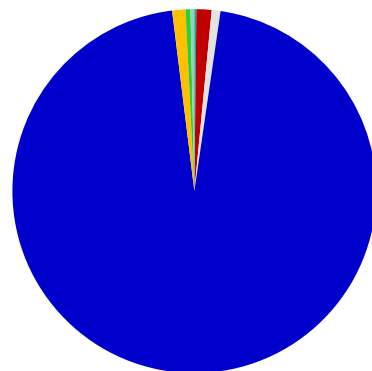


Full Load--5.5A



- L
- con_N
- con_P
- core
- winding_pri
- winding_sec
- con_sec
- Co

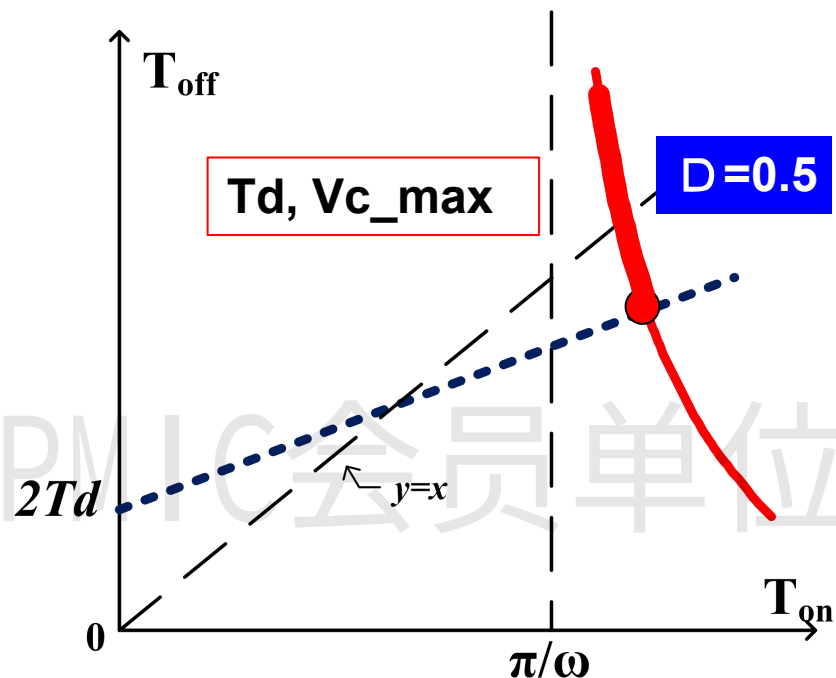
Light Load--0.5A



- L
- con_N
- con_P
- core
- winding_pri
- winding_sec
- con_sec
- Co

Voltage - Second Can be Reduced for Core Loss Reduction PMIC

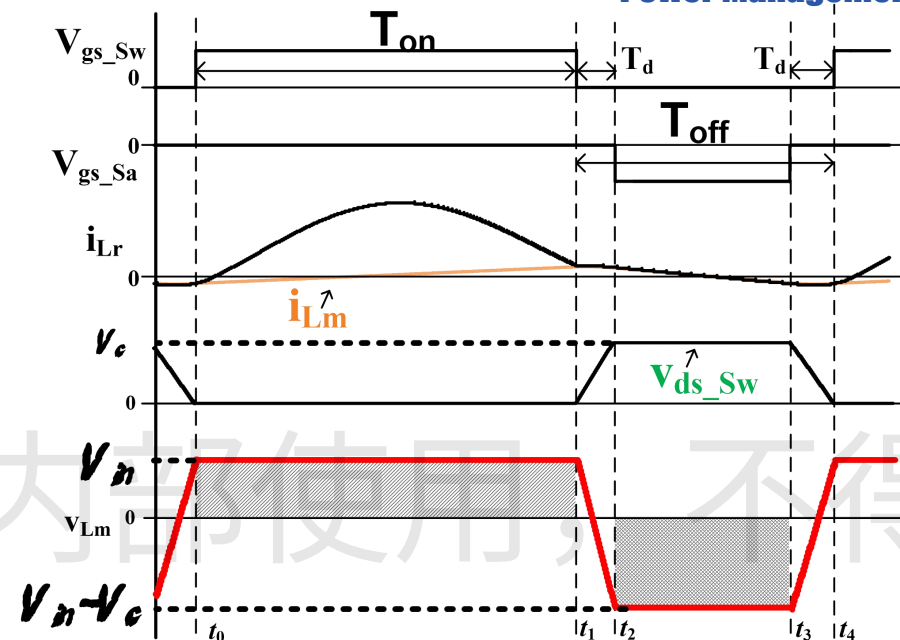
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Larger D , less conduction loss

Lm , volt-second balance

$$\frac{V_c}{V_{in}} = \frac{T_{on}}{T_{off} - 2T_d} + 1 \approx 1 / (1 - D)$$

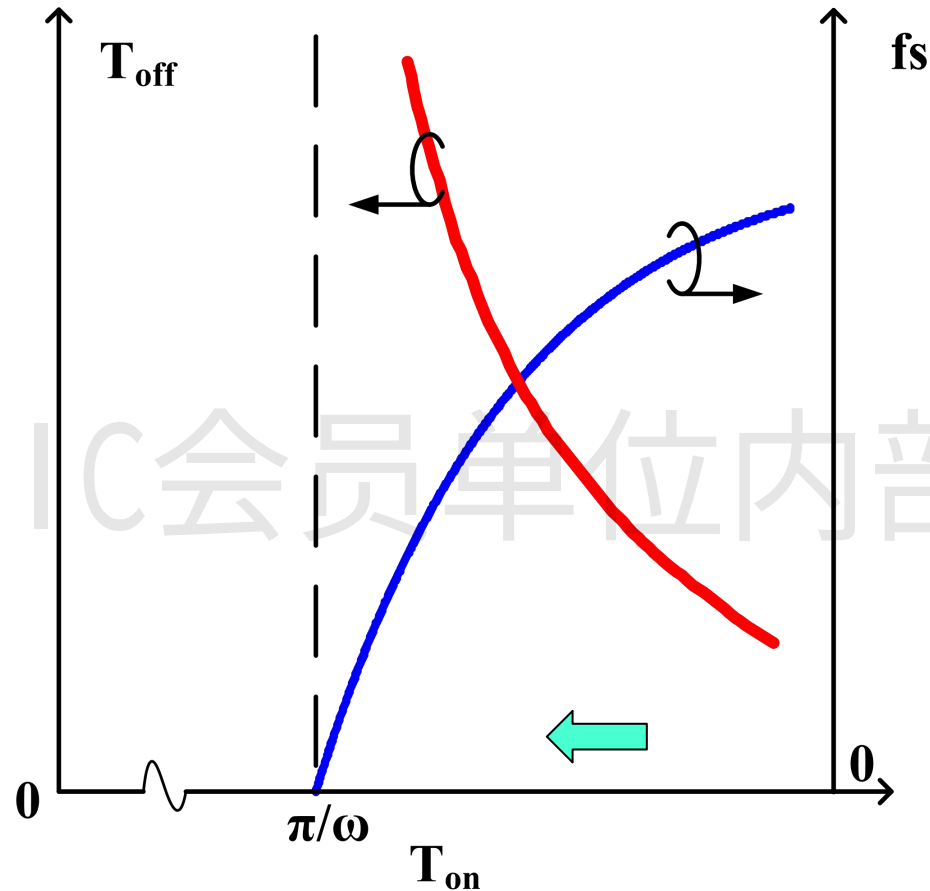


- T_{on} Can be Reduced to Reduce Transformer Voltage – Second
- T_{off} will increase that leads to lower Switching frequency

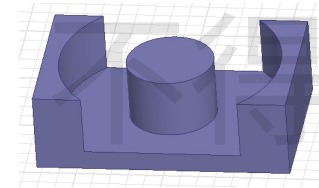


Relationship Between Duty Cycle (D) & Frequency (fs)

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$$\Delta B = \frac{V_{in} \cdot T_{on}}{NAe}$$

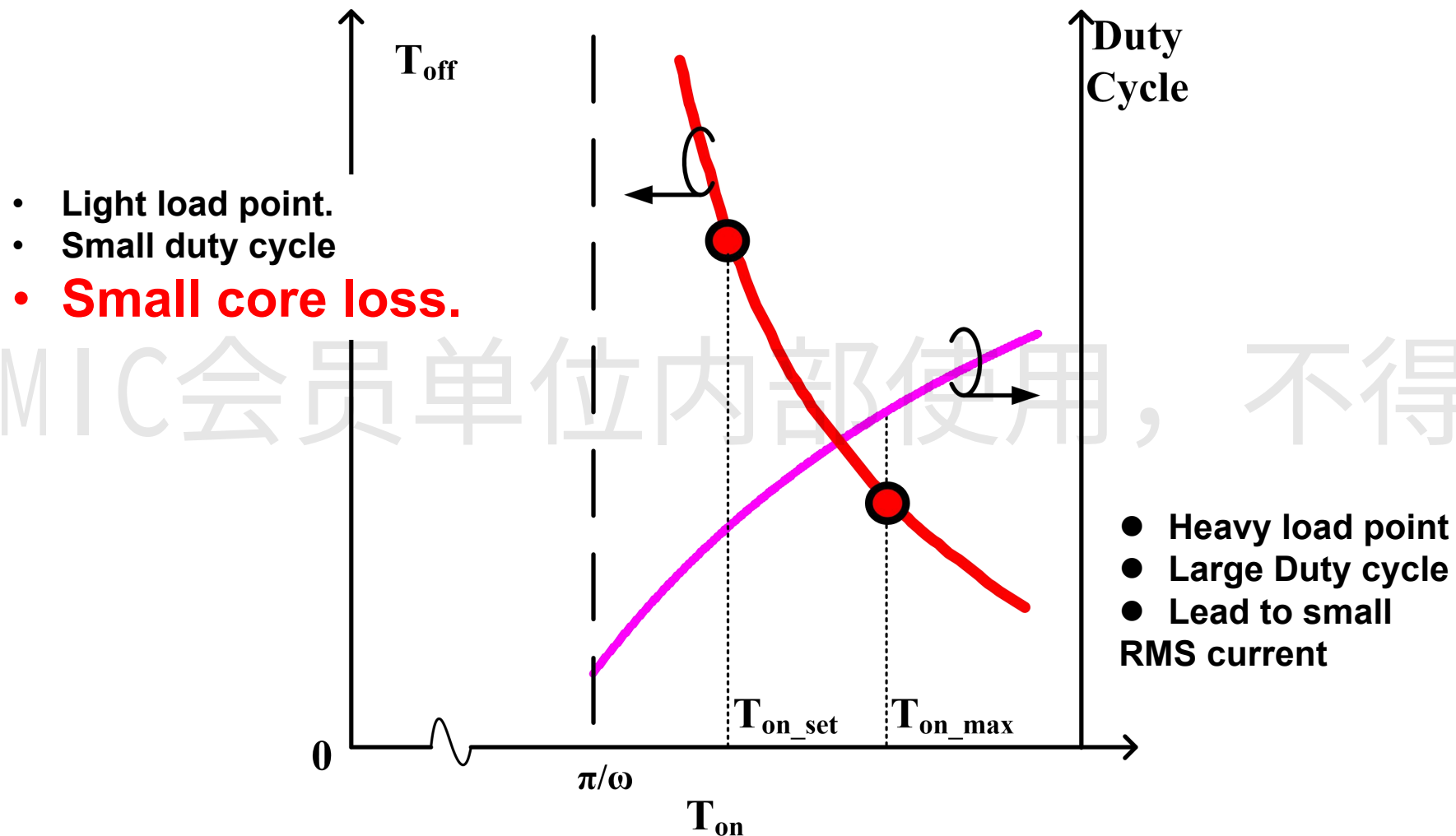


$$p_v = C \cdot \Delta B^\alpha f^\beta$$

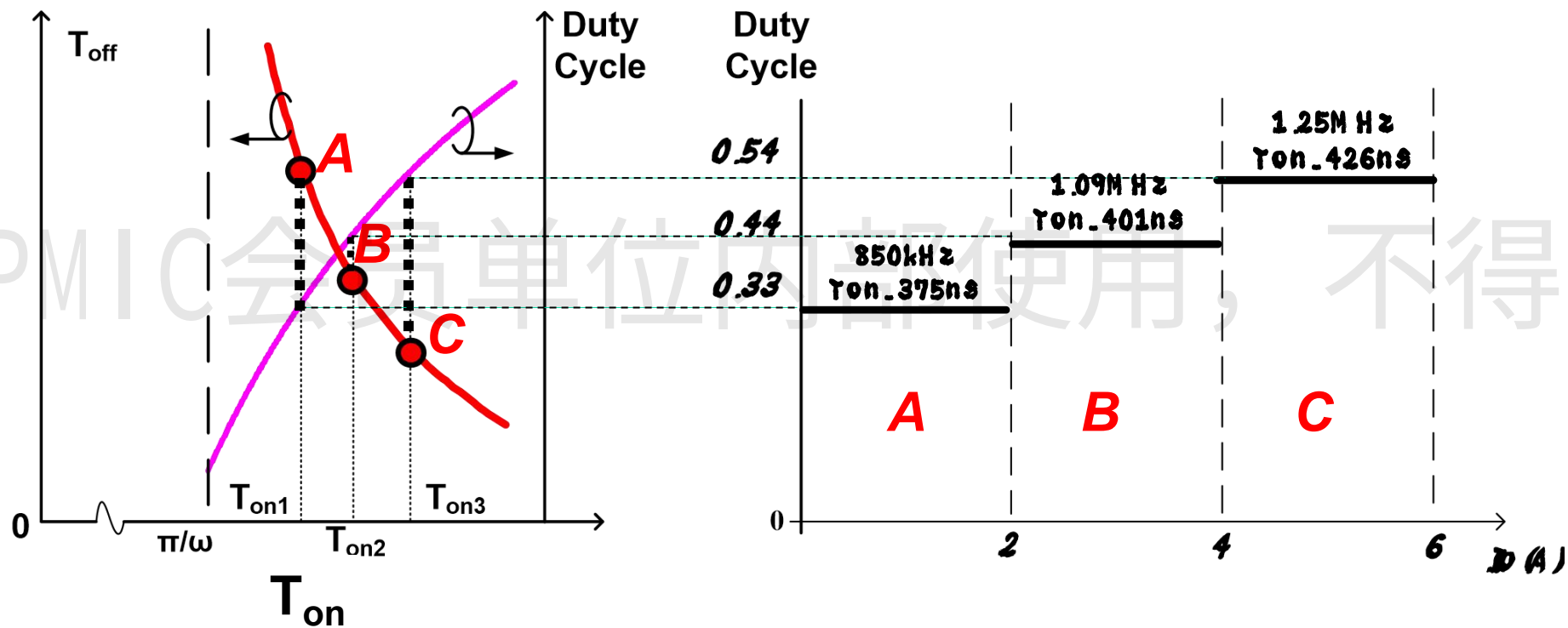



- Core loss decreases.

Adaptive **Ton** Control with Different Loads

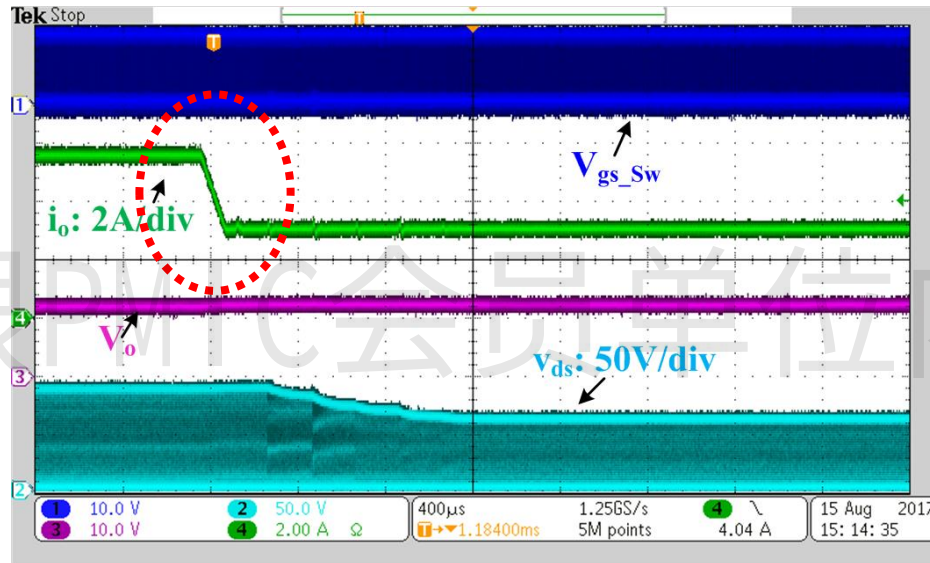


• Load adaptive Ton control.

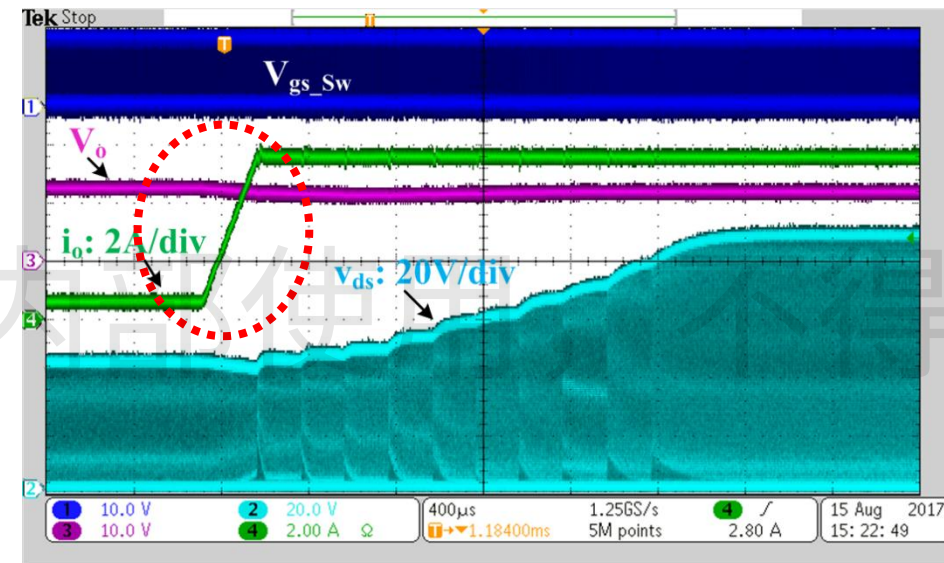


Duty Cycle Slow Adjustment won't Affect Voltage Stress

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Load Step-down

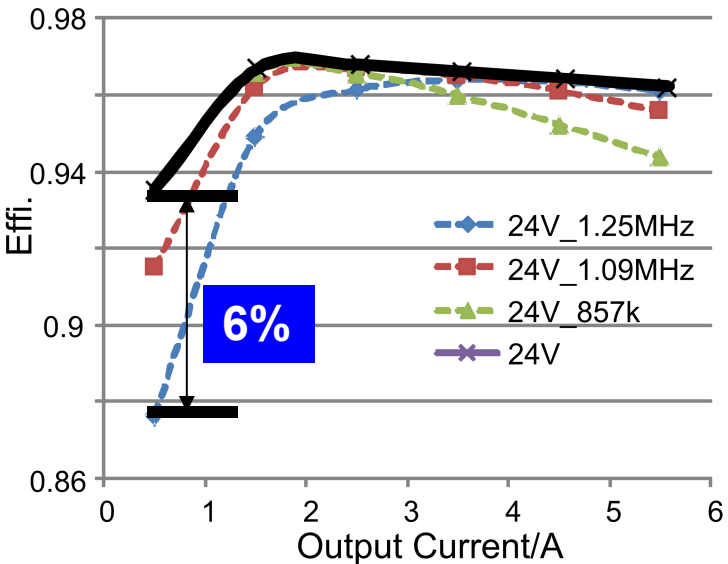
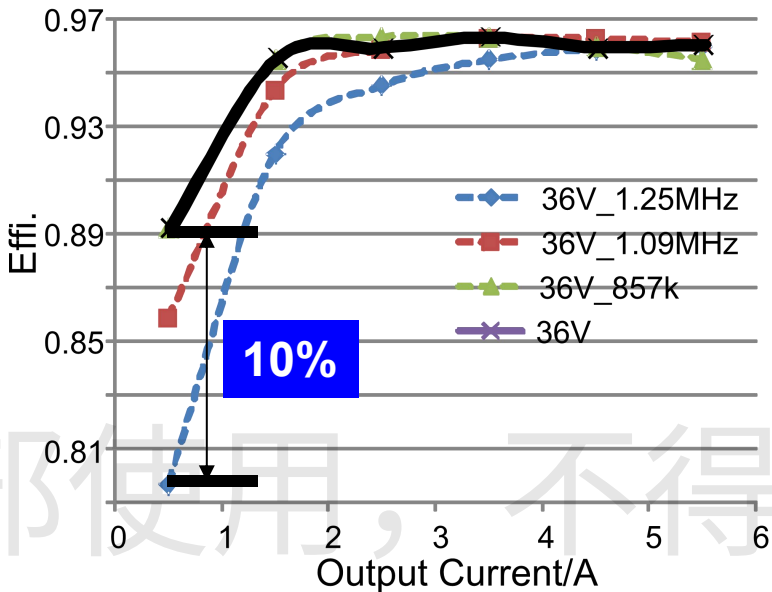
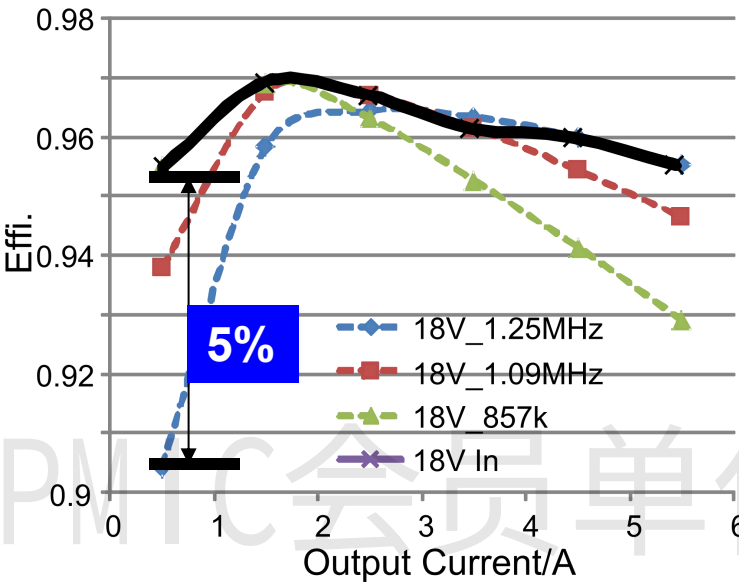


Load Step-up

Adaptive Ton Control Achieving Maximum Efficiency Envelop



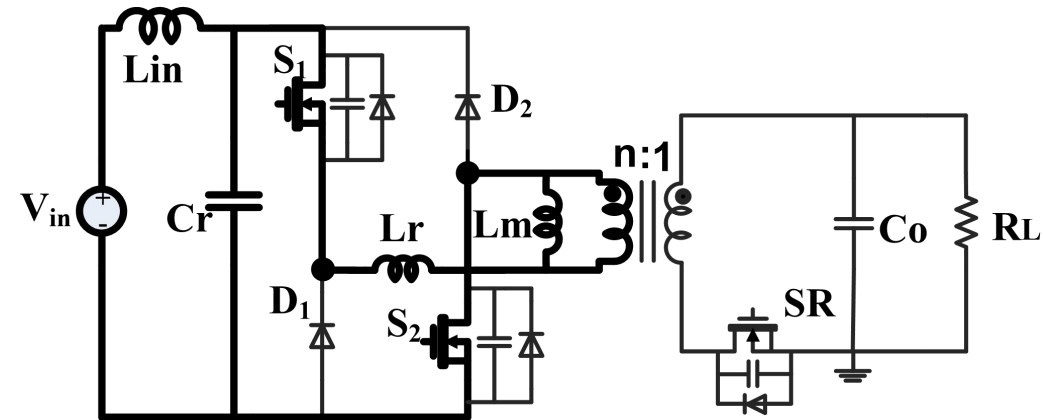
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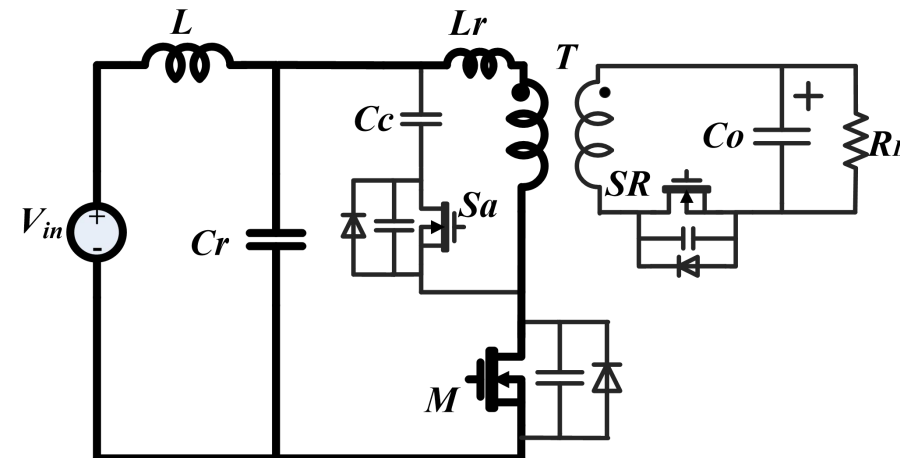
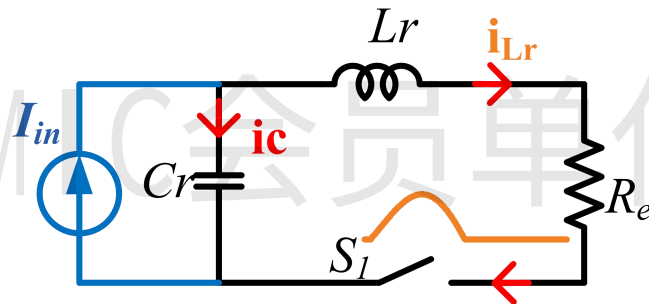
D~0.5

Topology	Without clamping	Secondary clamping	active clamping
Voltage stress	$3 \cdot V_{in}$	$2.5 \cdot V_{in}$	$2 \cdot V_{in}$
Duty cycle	< 0.5 .	< 0.5 .	> 0.5
Ton flexibility	No	No	Yes

Family of Forward DCX Topologies

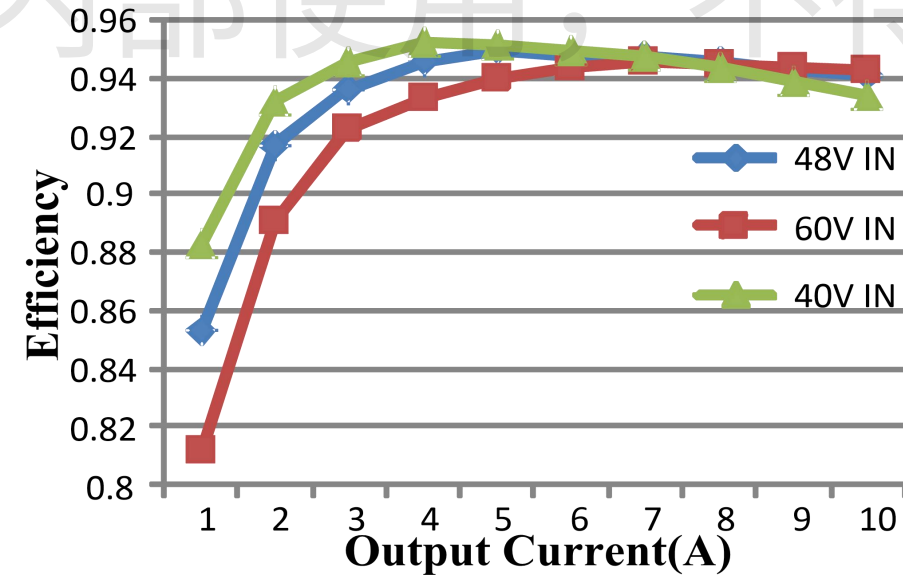
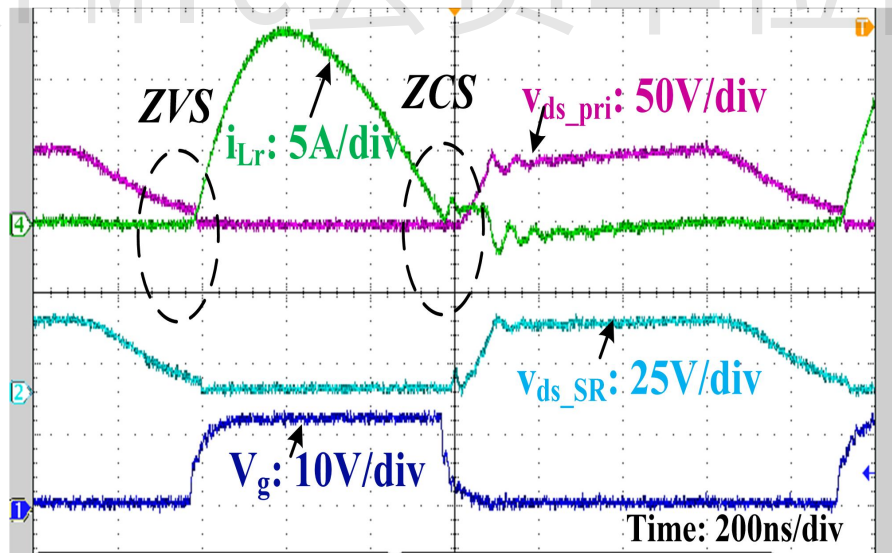
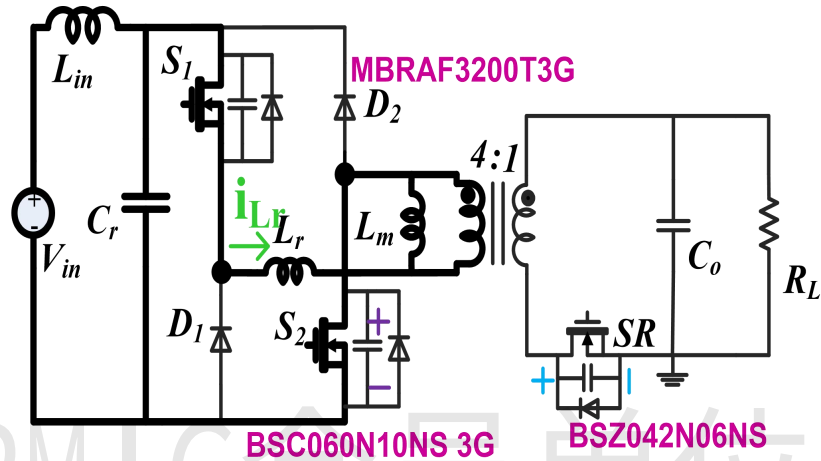


Two Switch Forward DCX

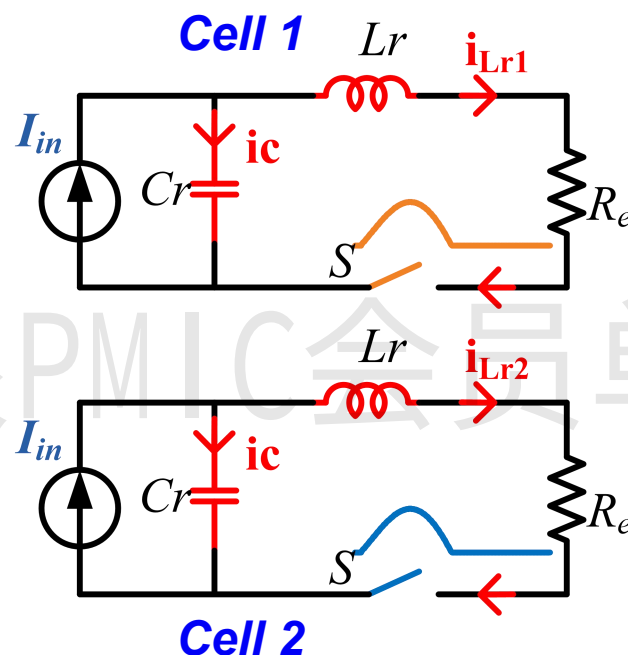


Active Clamp Forward DCX

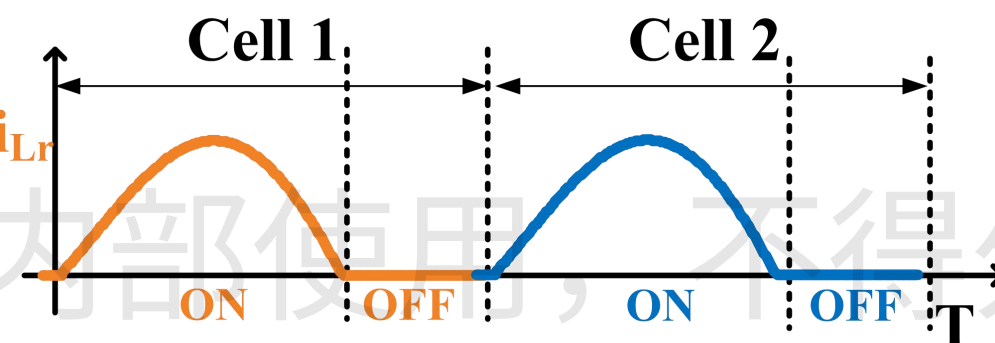
Verifications of Two-switch Forward DCX



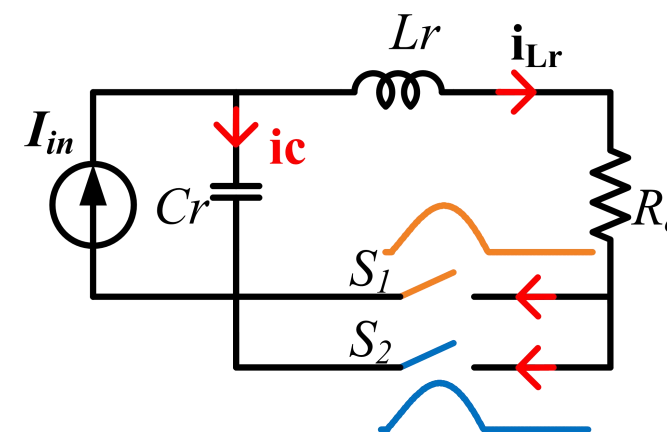
For higher power level



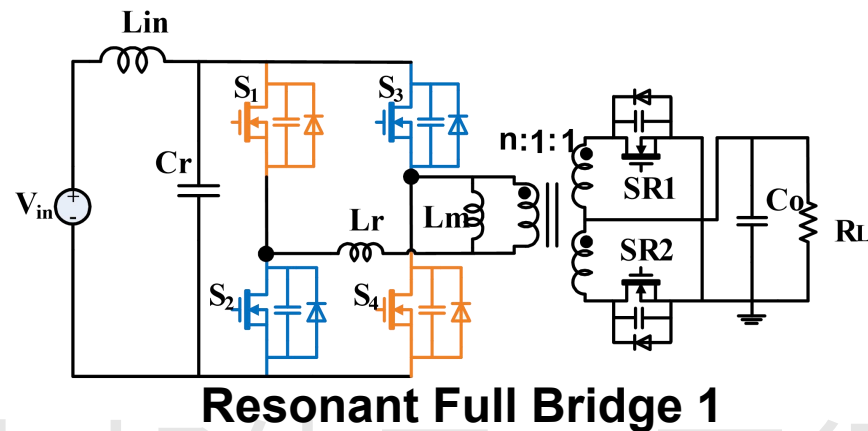
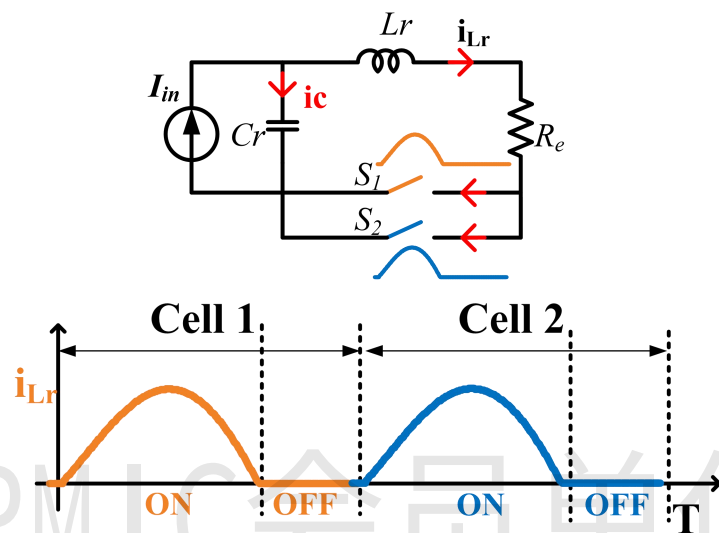
Integration I



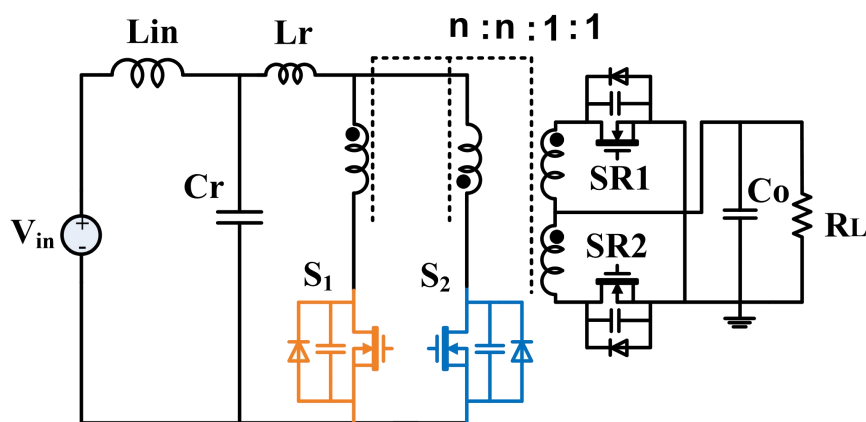
Common Resonant Cap.



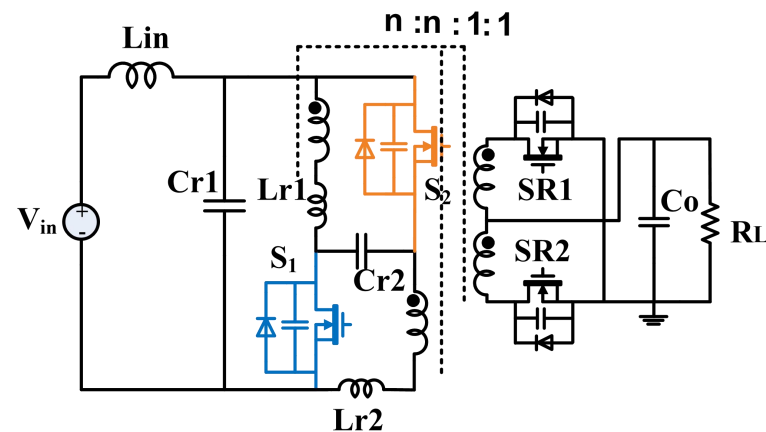
Topologies with Resonant Tank I



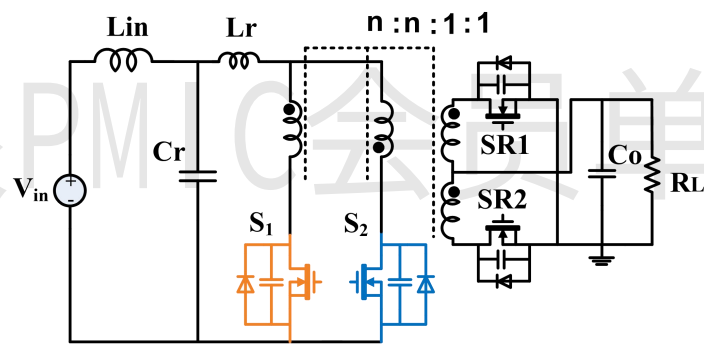
Resonant Full Bridge 1



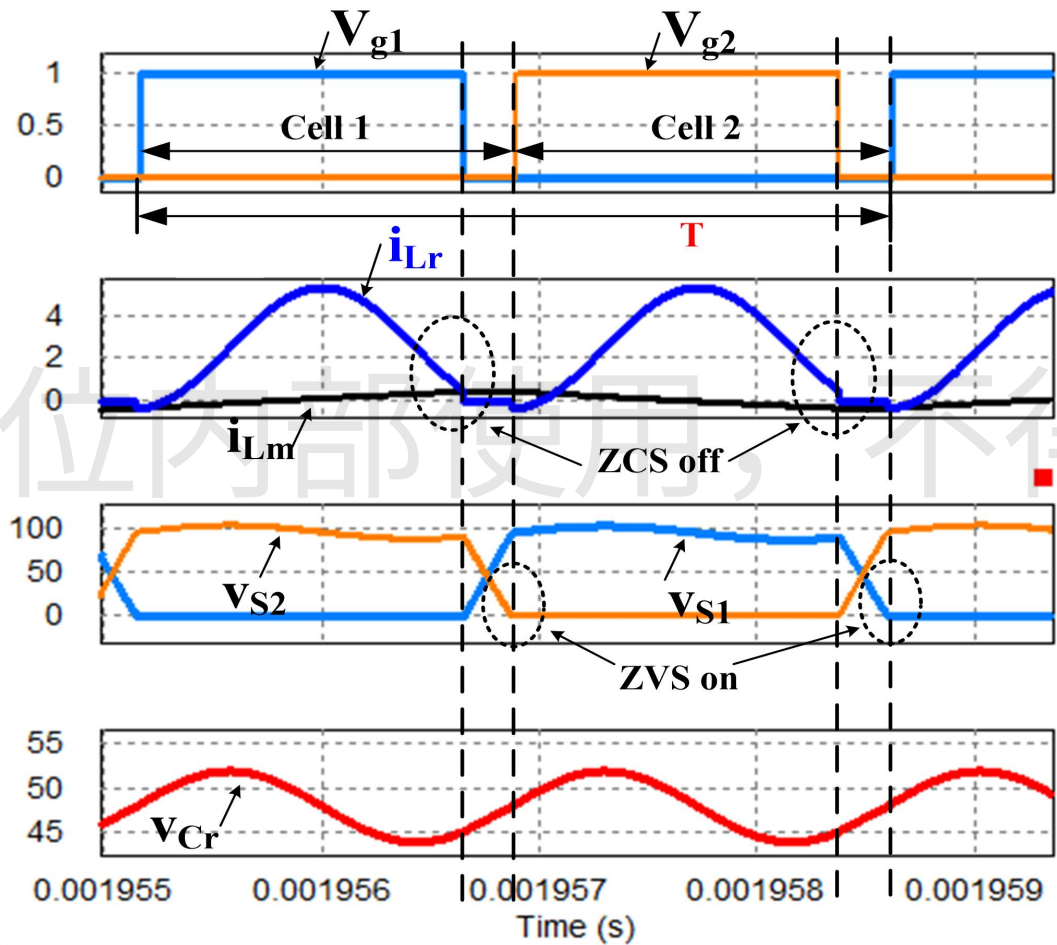
Resonant Push-pull 1



Resonant Push-Pull Forward

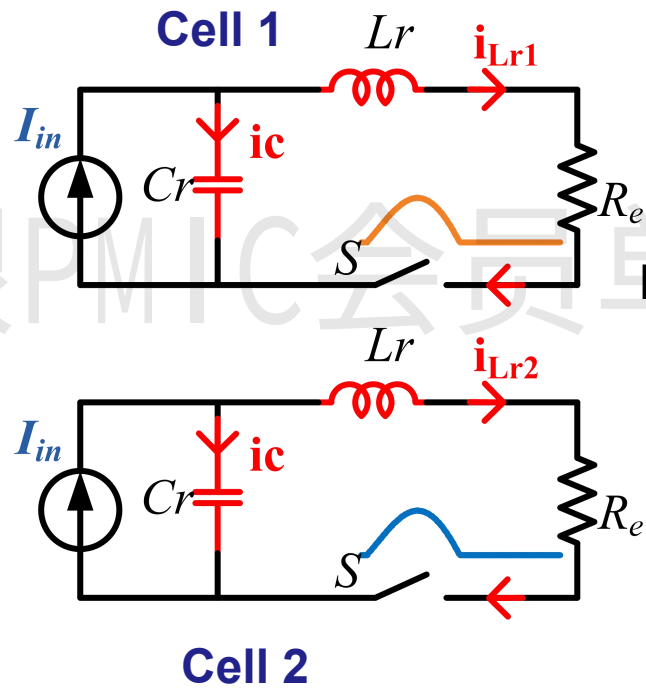


Push-pull DCX

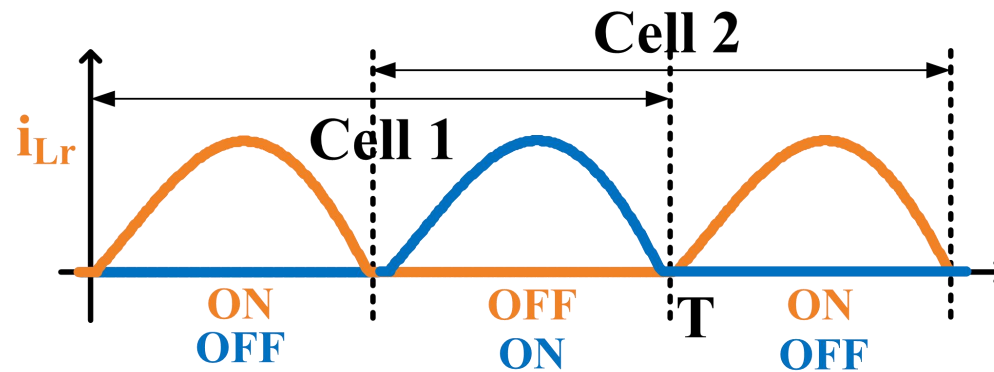
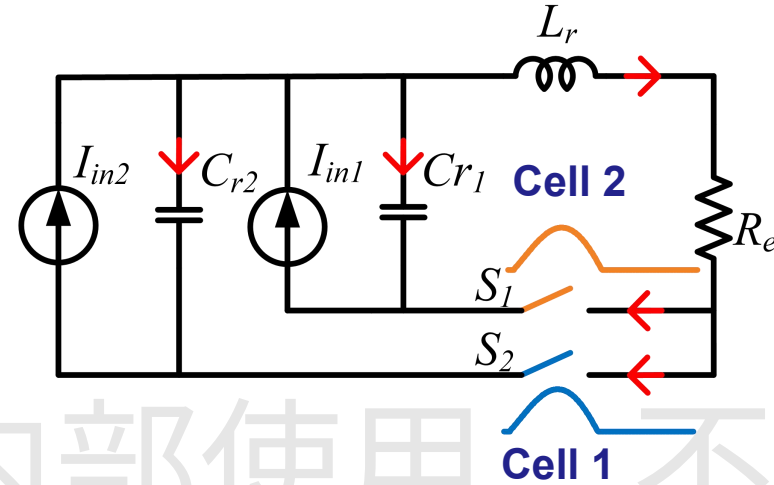


Extension II-

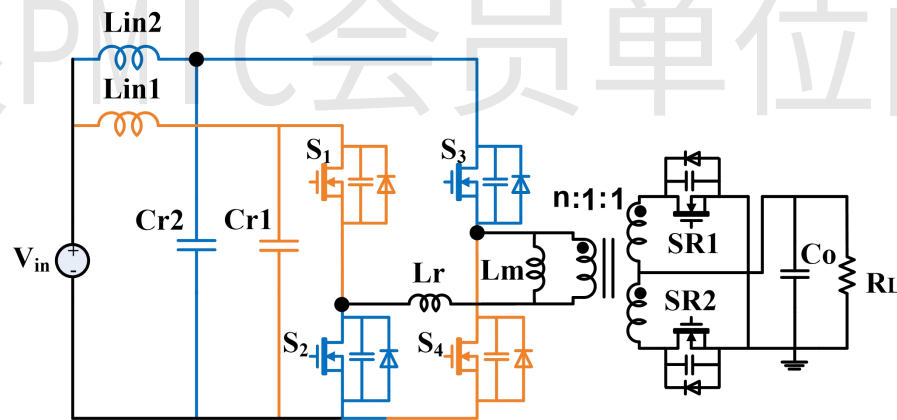
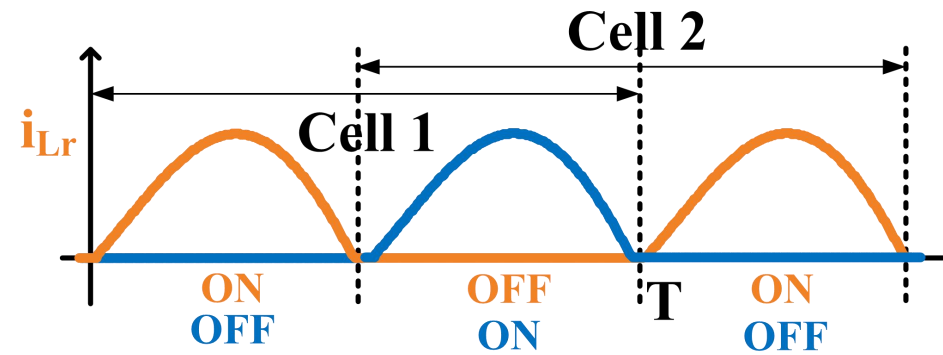
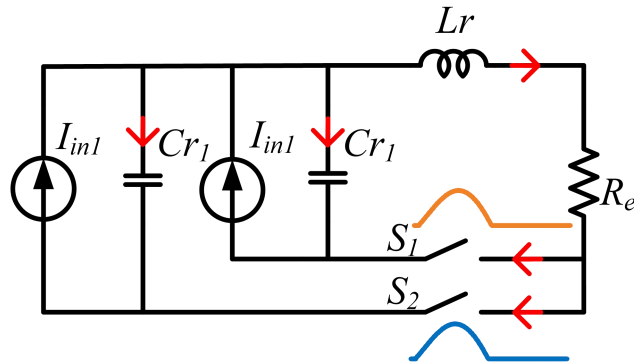
Integrating method--
independent resonant Cap.



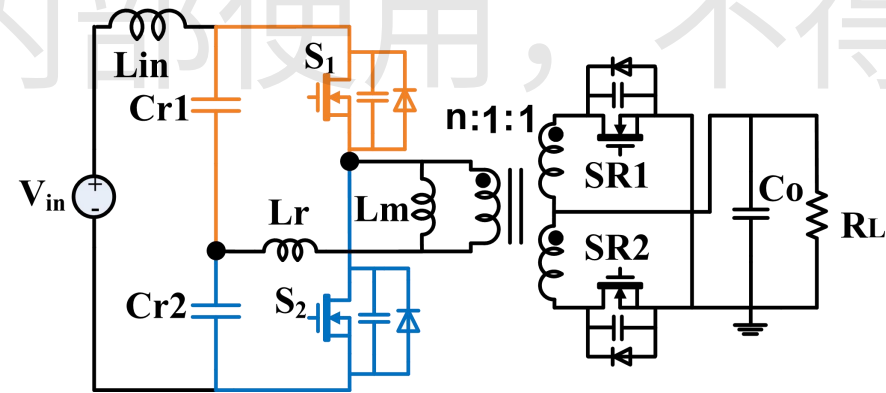
Integration II



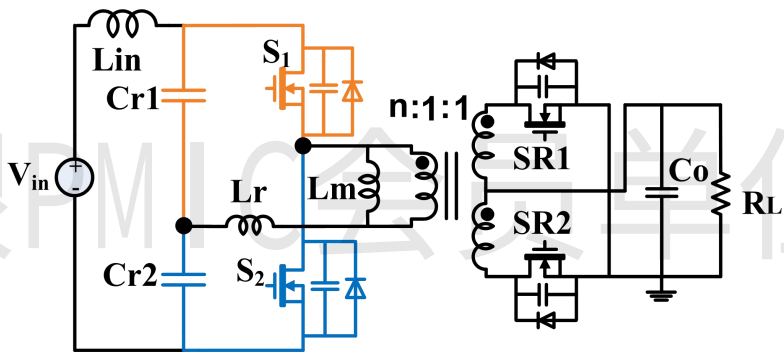
Family Topologies of Resonant Tank II



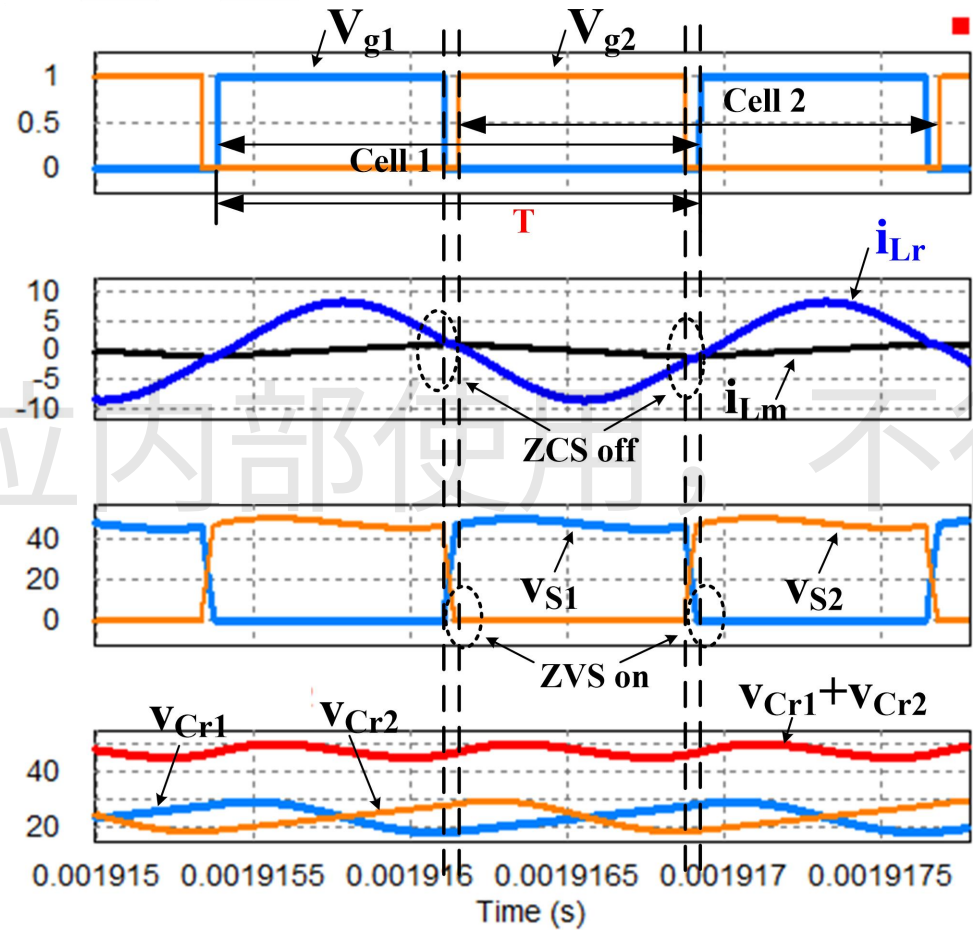
Resonant Full Bridge 2



Resonant half-bridge



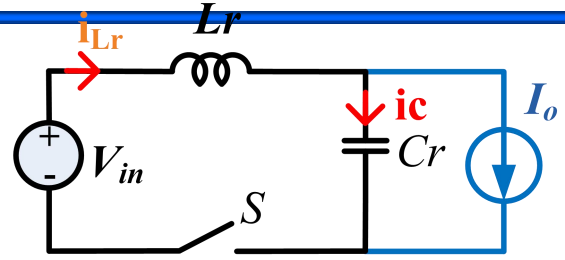
Resonant half-bridge
DCX



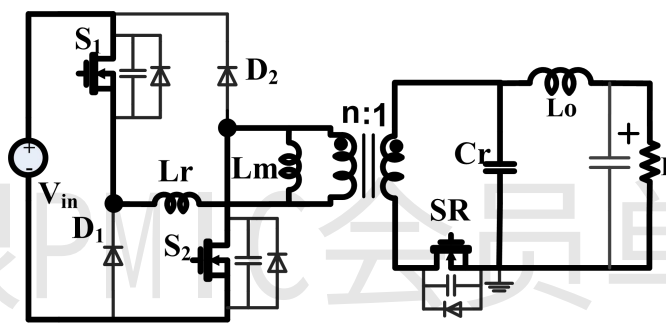
Topologies of Resonant DCX with output DC current source



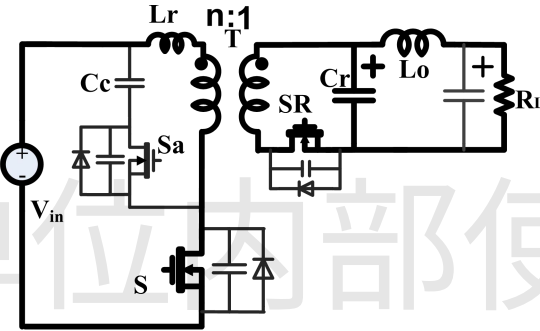
Power Management Innovation Consortium



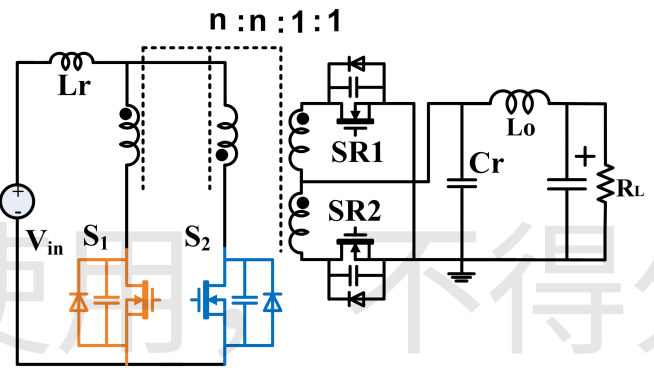
Resonant cell with output current feed



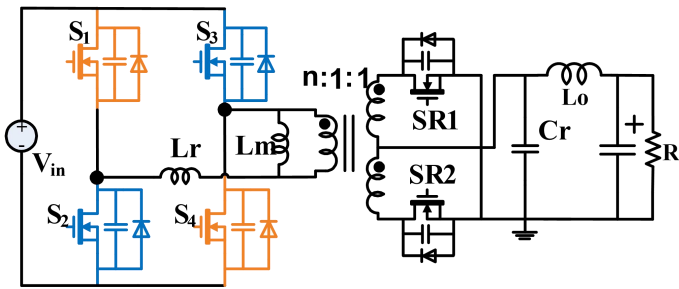
Two-switch forward



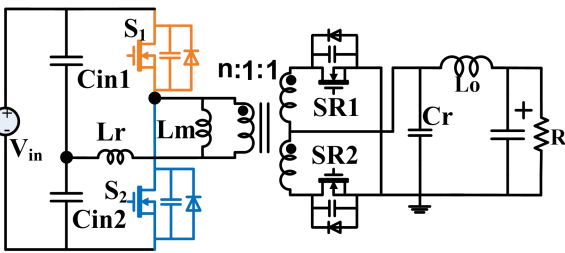
Active clamping forward



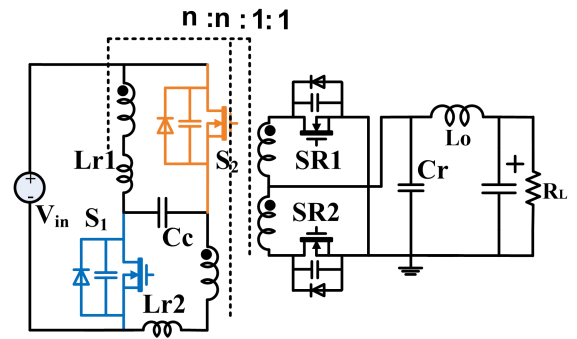
Push-pull



Full bridge



Half bridge



Push-pull forward

□ The unidirectional resonant tank with DC current source has following features:

- The single switch forward DCX achieves ZVSZCS for low power low voltage applications. MHz frequency is easily implemented with high efficiency.
- The active clamping forward DCX can reduce the voltage stress and improve the light load efficiency with adaptive on time control at MHz frequency.
- Based on the proposed unidirectional resonant tank and tank integrating method, more resonant topologies are derived for high power applications, which are also competitive with conventional LC resonant DCXs.

1. Introduction of power supply architecture of internet datacenter and popular high density high efficiency applications.
2. Topology for MHz high efficiency 380V-48V/12V power conversion
 - 2.1 Unregulated DC-DC techniques
 - 2.2 EMI design considerations of planar PCB transformer
 - 2.3 Tight regulated 380V-12V conversion
3. MHz high efficiency 48/12V/XV power converters
 - 3.1 Low power DCX converter for intermedia bus application.
 - 3.2 Tight regulated DC-DC converter for 48V-12V in server
 - 3.3 High Density Transformer Design for 48V MHz DC-DC converter
4. Conclusions

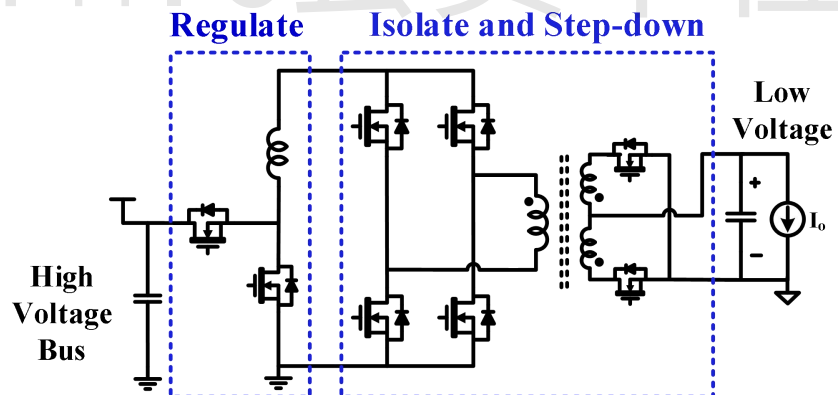


Two-stage Converter

48V/12V:



96% 242W/in³



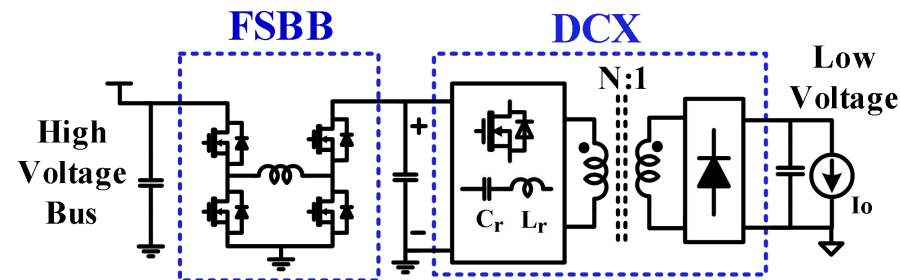
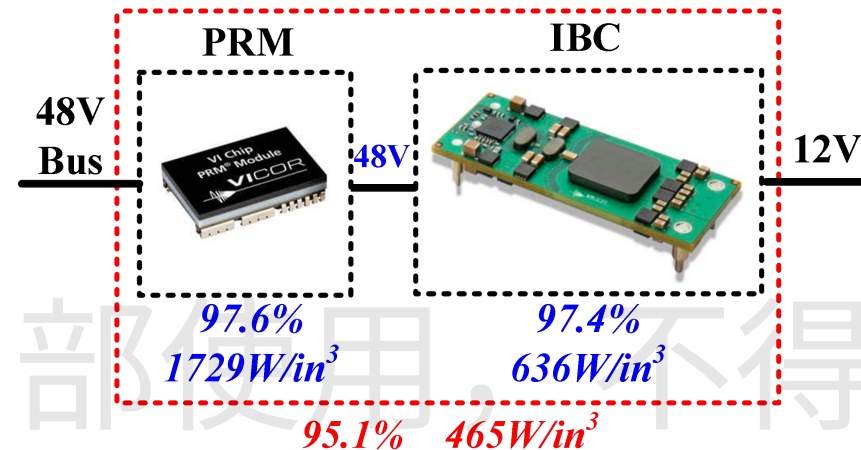
PRM: PRM48by480x500A00

IBC: IB0xE120T40xx-xx

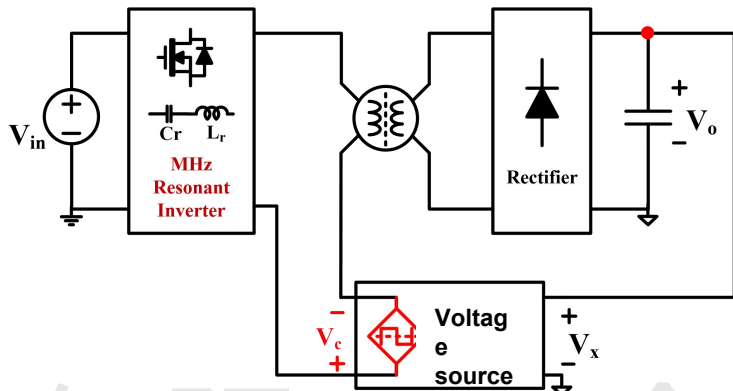
SynQor: PQ6012QZB33



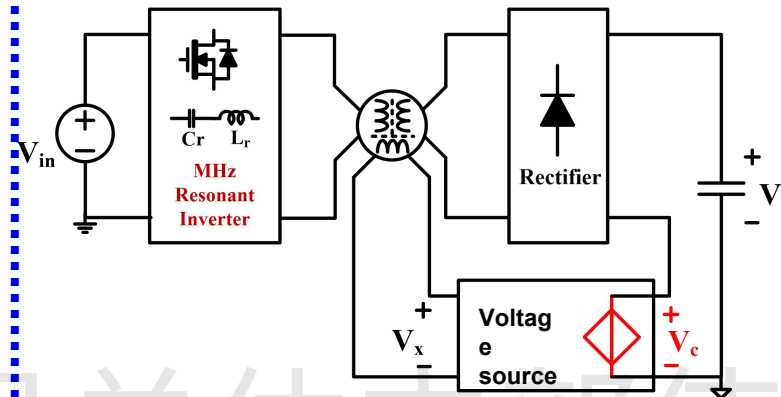
- System efficiency sacrifice
- Power density decrease



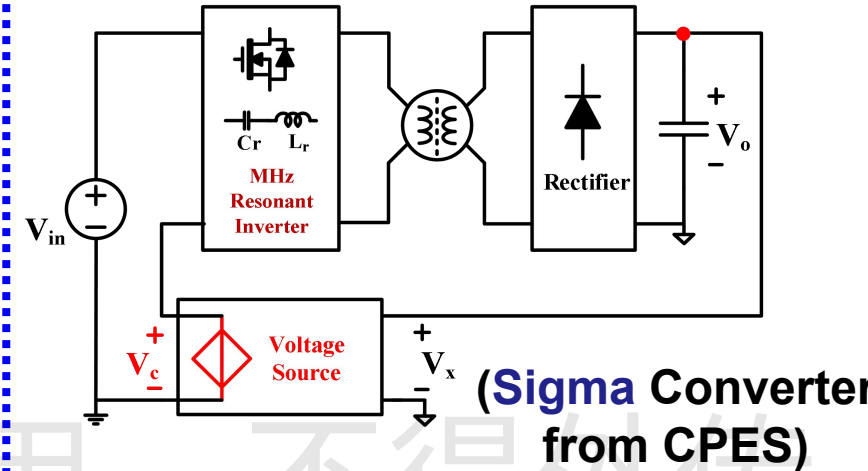
Three Types of Tight Regulated DCXs (RDCX)



Two-port network



Two-port network



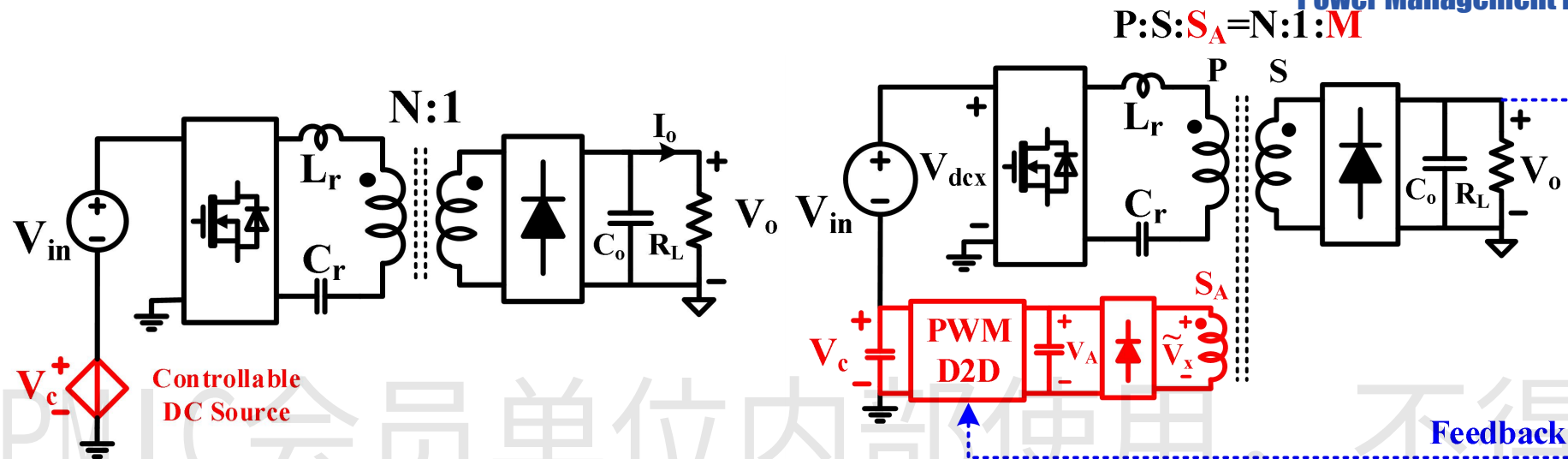
Two-port network



2. AC Parallel / DC in series

3. DC parallel / DC in series

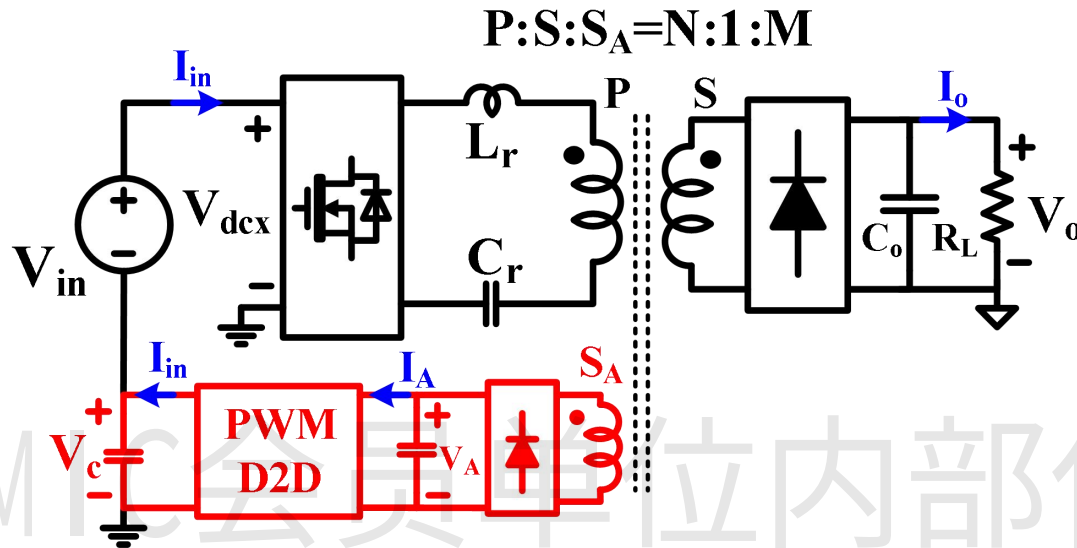
RDCX --- DC In Series AC In Parallel



- Regulated V_o
- Part power regulation
- Without additional transformer
- Suitable for high normal input voltage

Steady State Voltage Gain RDCX with Primary in Series

Power Management Innovation Consortium



Voltage Relationship:

$$V_o = \frac{V_{in} + V_c}{N}$$

$$V_A = M \cdot V_o$$

Define Voltage
Gain of D2D:

$$G = \frac{V_c}{V_A} = \frac{N \cdot V_o - V_{in}}{M \cdot V_o} = f(D)$$

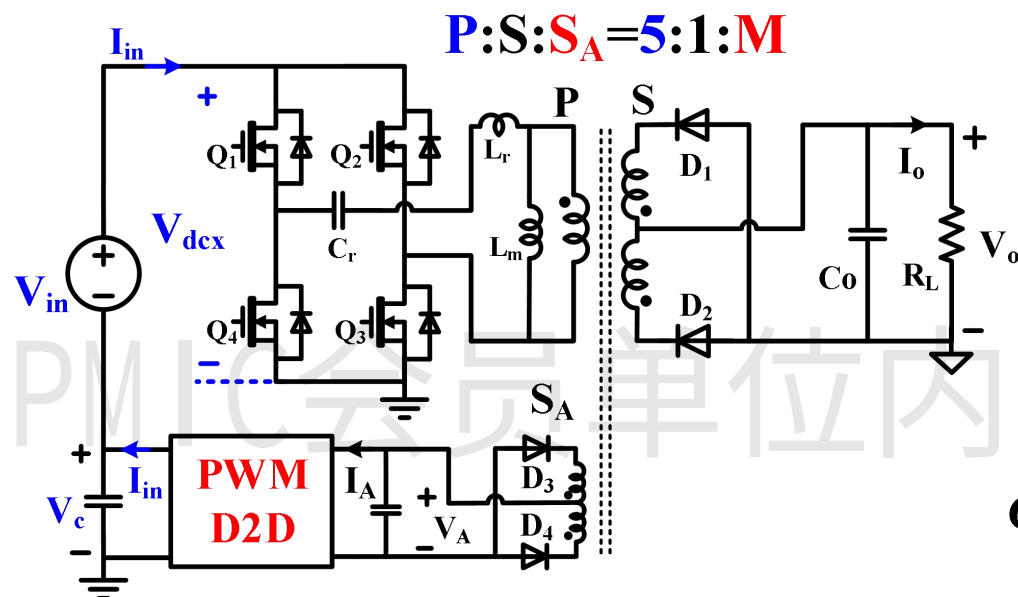
RDCX Voltage Gain:

$$\frac{V_o}{V_{in}} = \frac{1}{N - f(D) \cdot M}$$

Transformer Design: N, M

Auxiliary D2D Design: $f(D)$

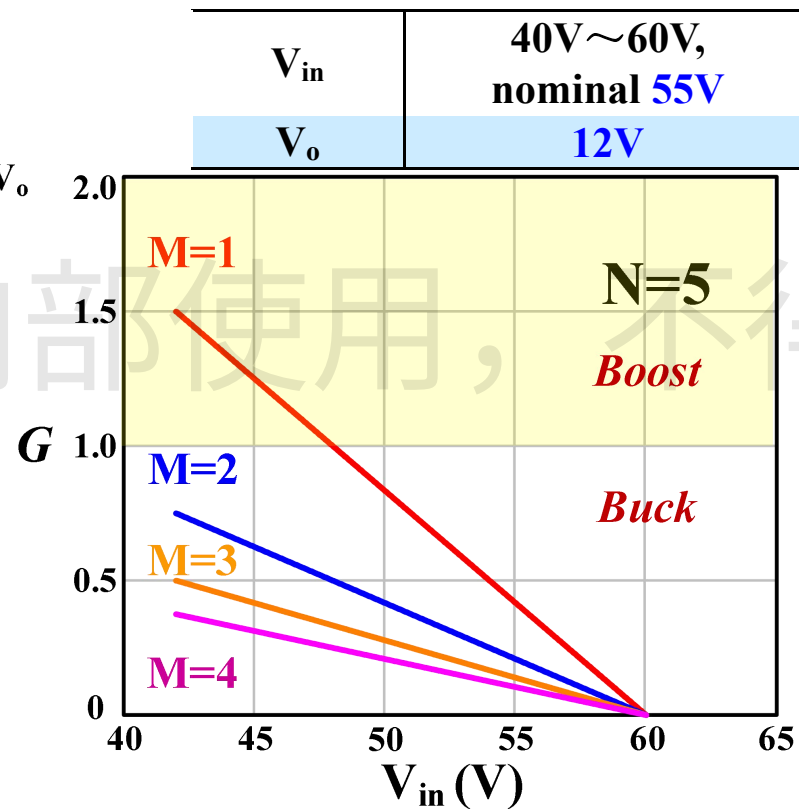
Relationship between M and D2D



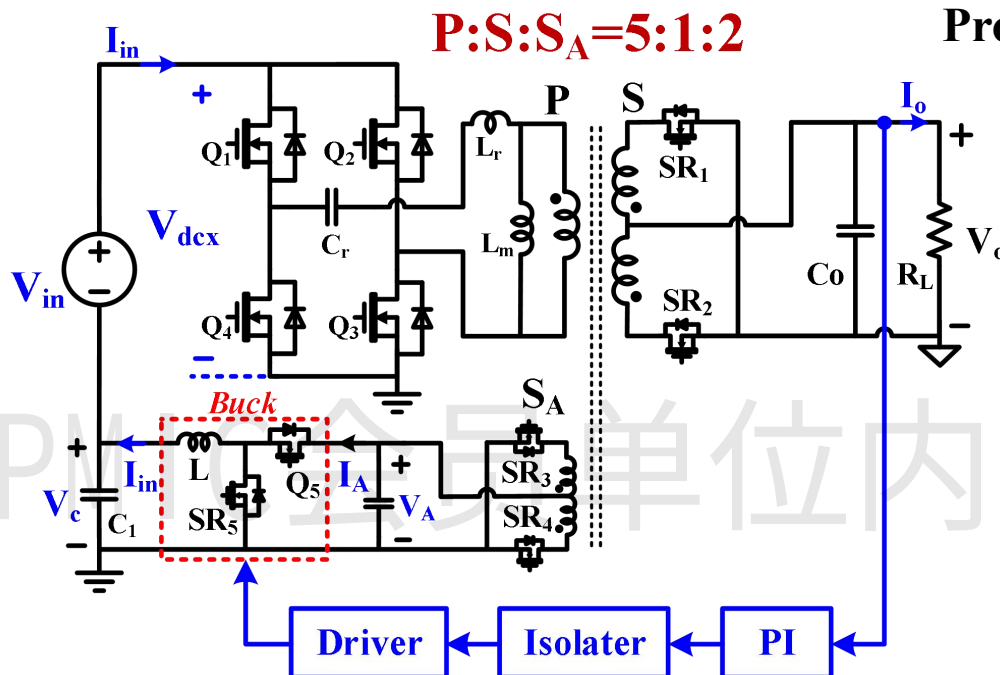
Voltage Gain of the D2D:

$$G = \frac{V_C}{V_A} = \frac{N \cdot V_o - V_{in}}{M \cdot V_o} = f(D)$$

Application:



Prototype:



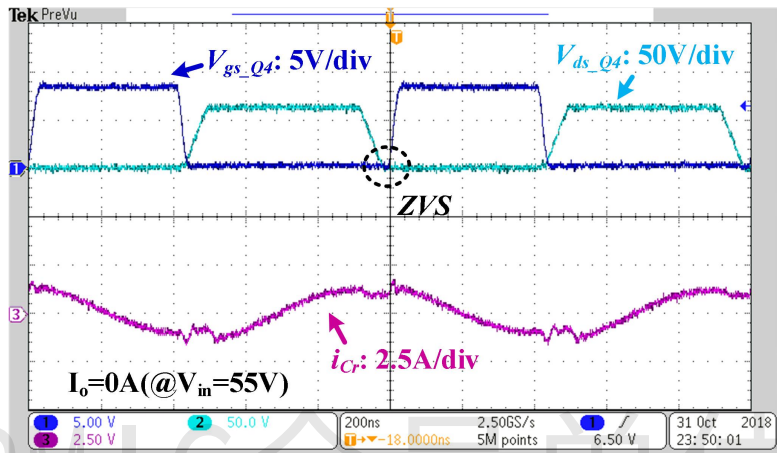
450W/in³

Size: 45.0*34.5*8.5mm³

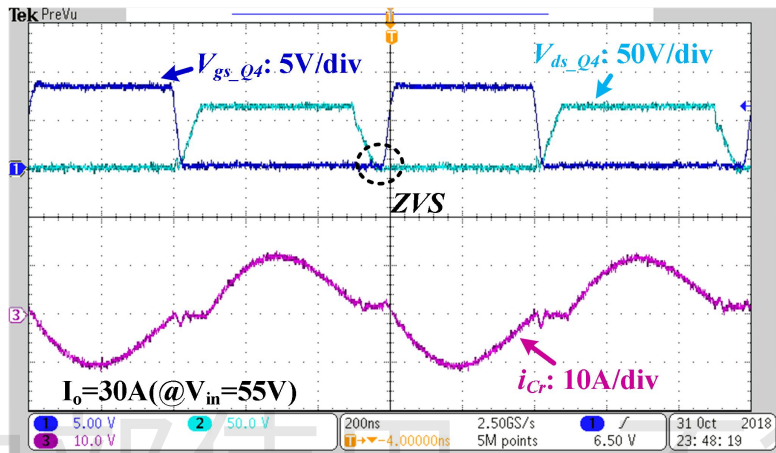
Based on 5*6mm² Si MOSFETs

V_{in}	42V~60V, 55V
V_o	12V
P_{out}	360W
f_s	1MHz

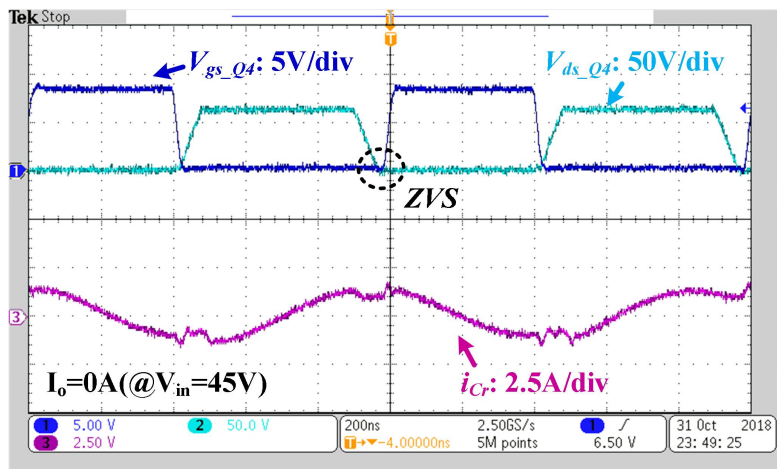
ZVS Waveforms at Different V_{in} or Load



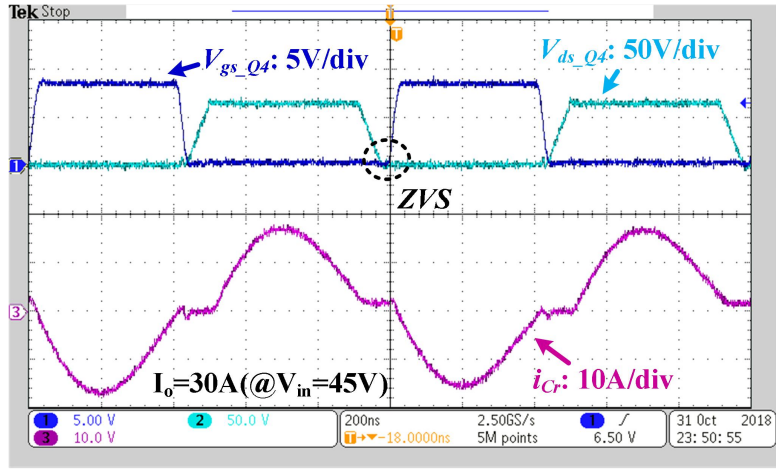
Waveforms @ $V_{in}=55V$ and $I_o=0A$



Waveforms @ $V_{in}=55V$ and $I_o=30A$



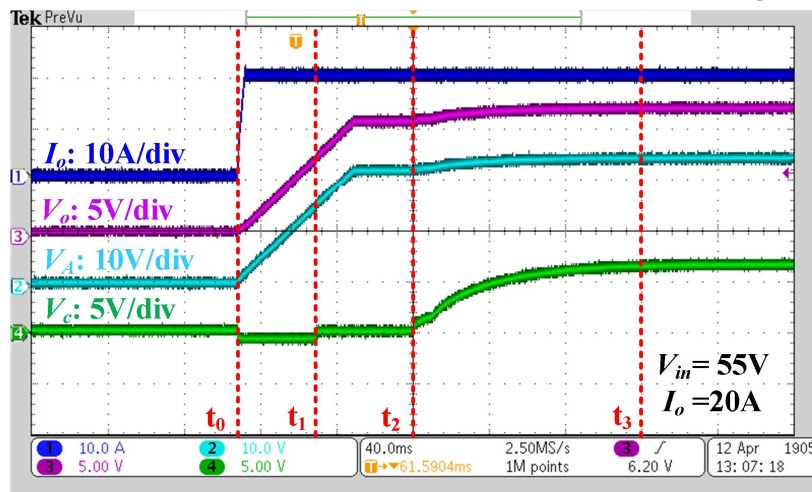
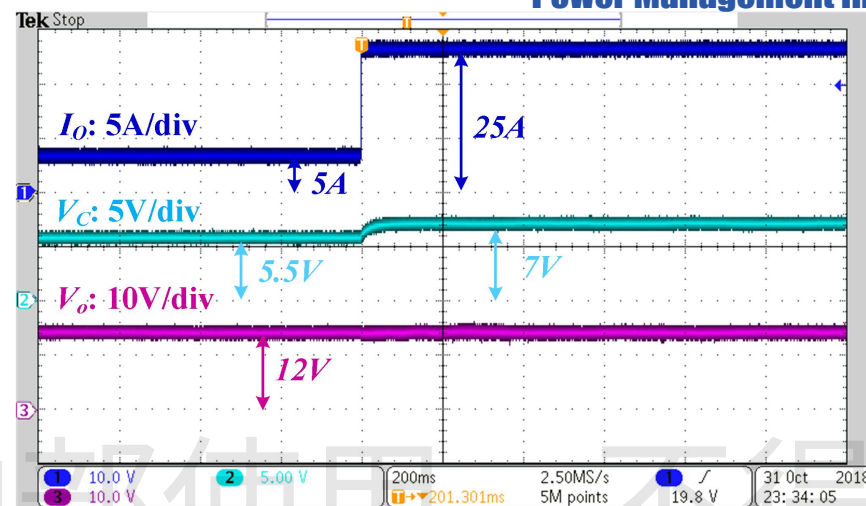
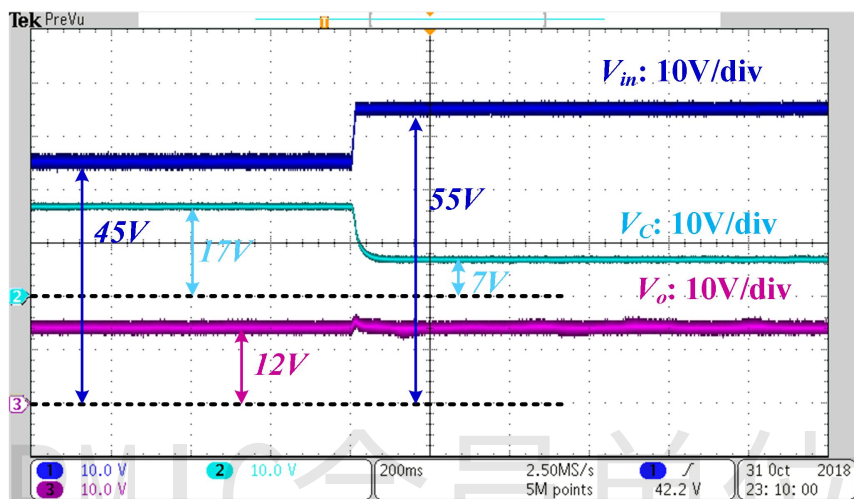
Waveforms @ $V_{in}=45V$ and $I_o=0A$



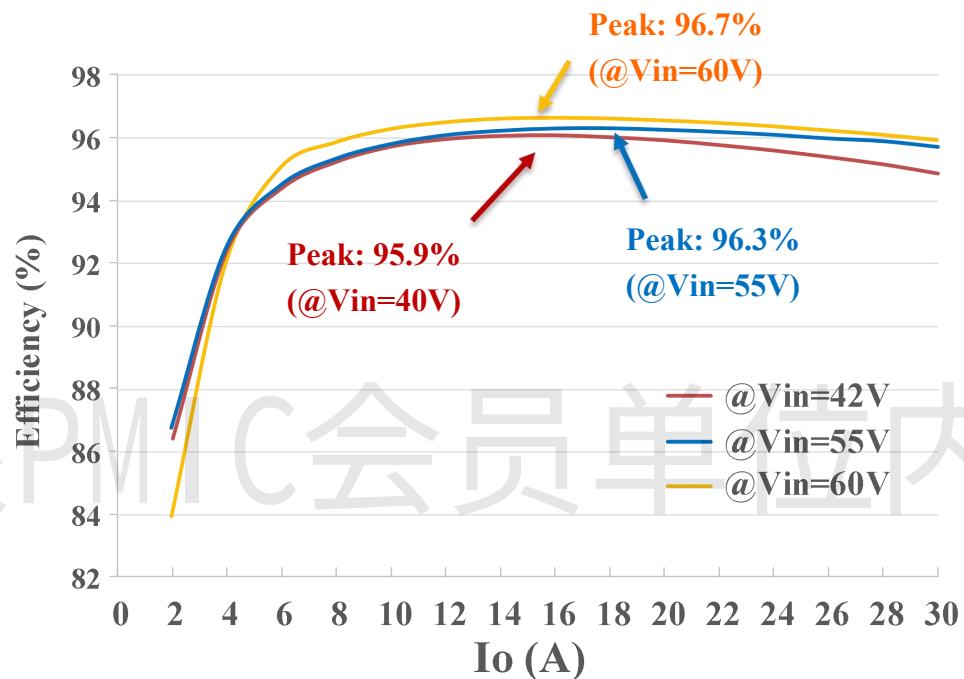
Waveforms @ $V_{in}=45V$ and $I_o=30A$



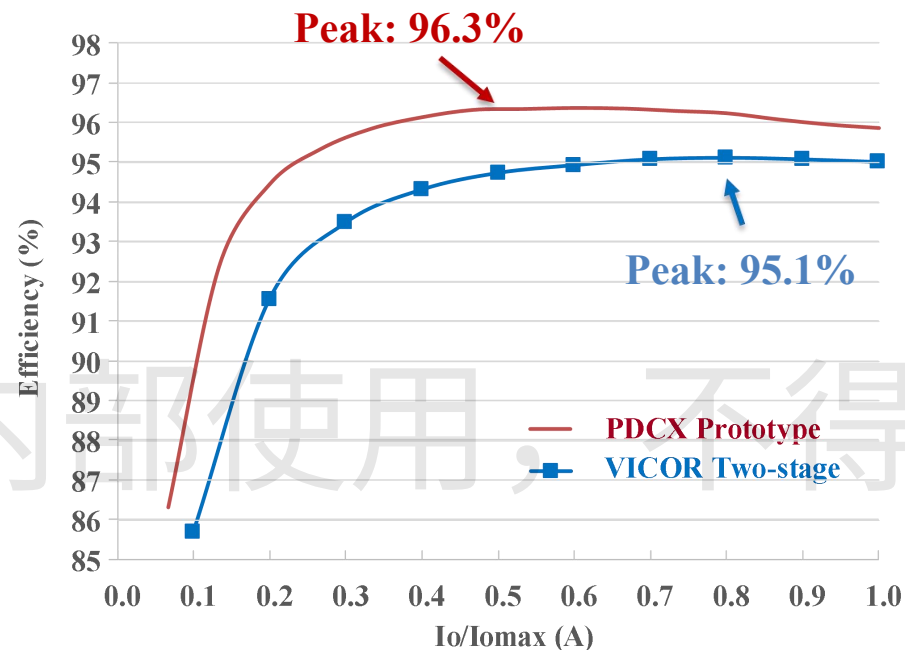
Dynamic and Startup Performance



Measured Efficiency— RDCX



Measured efficiency of RDCX at different input voltages



Measured efficiency of RDCX and calculated efficiency of two stage @ $V_{in}=55V$

PRM: PRM48by480x500A00, VICOR, 2015

IBC: IB0xE120T40xx-xx, VICOR, 2017

- A family of MHz RDCX converters with voltage regulation capability is proposed.
- High frequency, high power density and high efficiency are achieved in RDCX with tight regulating capability.
- The auxiliary transformer is not necessary to implement partial power regulation
- Different RDCXs have different sweet operating point.



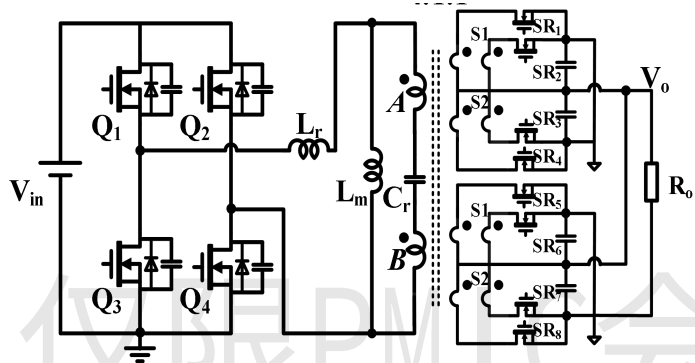
1. Introduction of power supply architecture of internet datacenter and popular high density high efficiency applications.
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Relationship between height and length of Planar Transformer

48V/12V isolated DCX converter

Turns ratio 4:1:1



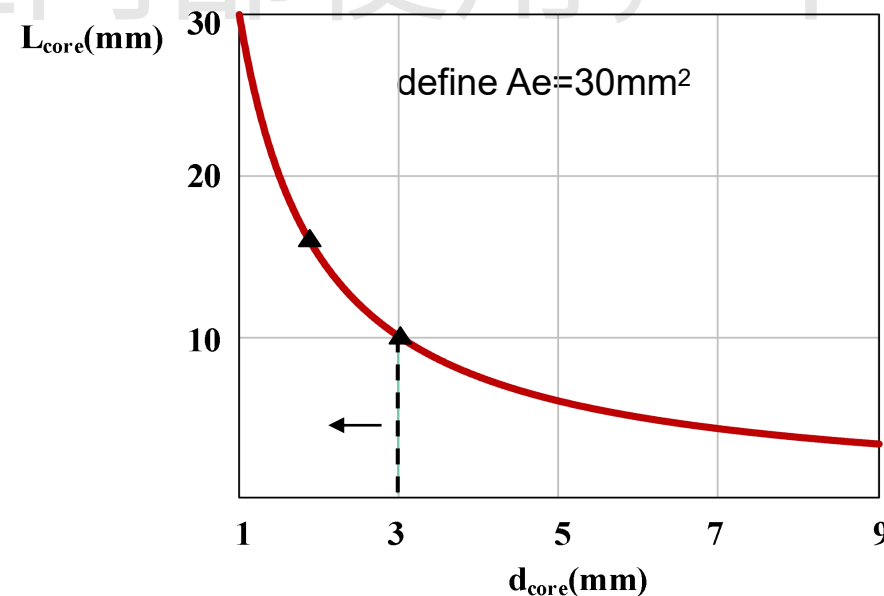
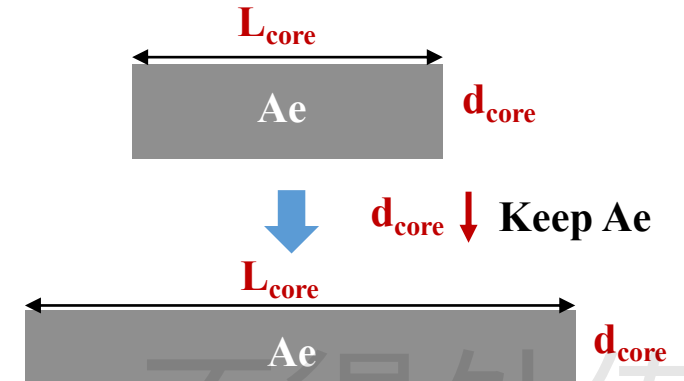
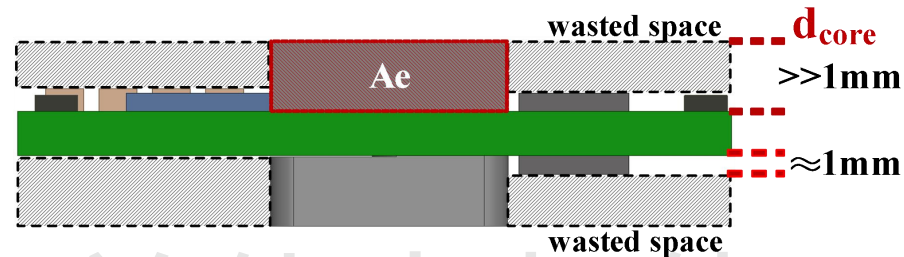
$$L_{\text{core}} = \frac{A_e}{d_{\text{core}}}$$

A_e - The equivalent cross area of the core

L_{core} - The length of the core

d_{core} - The thickness of the core

Side view of the transformer

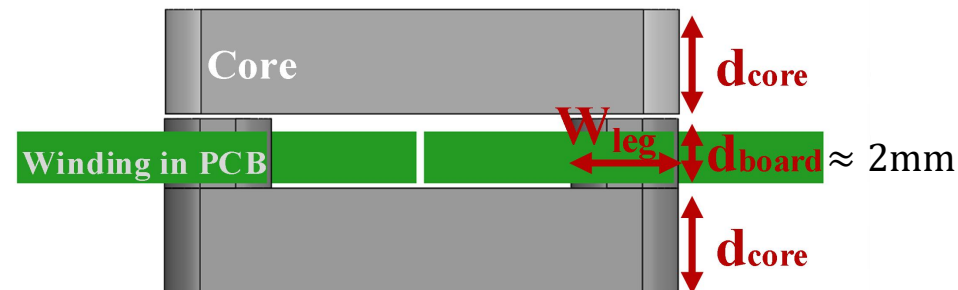
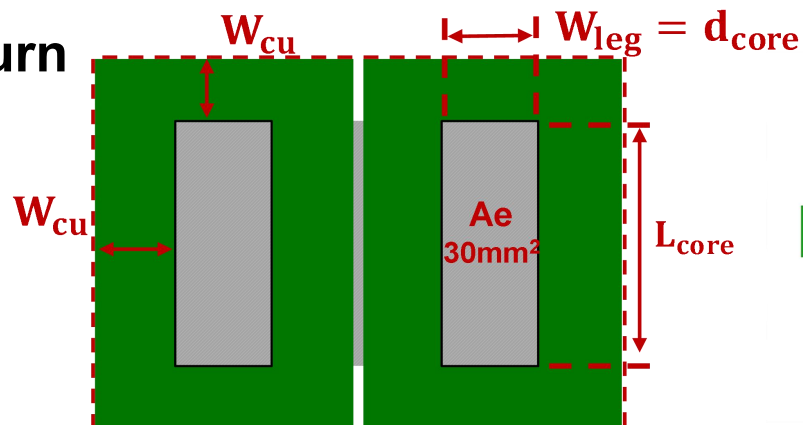


Limitation of Planar Transformer's Power Density

Given: $V_o=12V$, $N_s=1$ Turn
 $f_s=1.6MHz$

$$\Delta B : = \frac{V_o \cdot T_s / 2}{A_e \cdot N_s}$$

$$= \frac{12}{96} = 0.125 \text{ (T)}$$



Considering copper loss → Fixed R_{dc}

$$W_{cu}(d_{core}, R_{dc}) = \frac{2\rho}{d_{cu} \cdot R_{dc} - 4\rho} \cdot (d_{core} + \frac{A_e}{d_{core}})$$

$$V_{Tr}(d_{core}, R_{dc}) = (2L_{leg} + 4W_{cu})(L_{core} + 2W_{cu})(2d_{core} + 2d_{board})$$

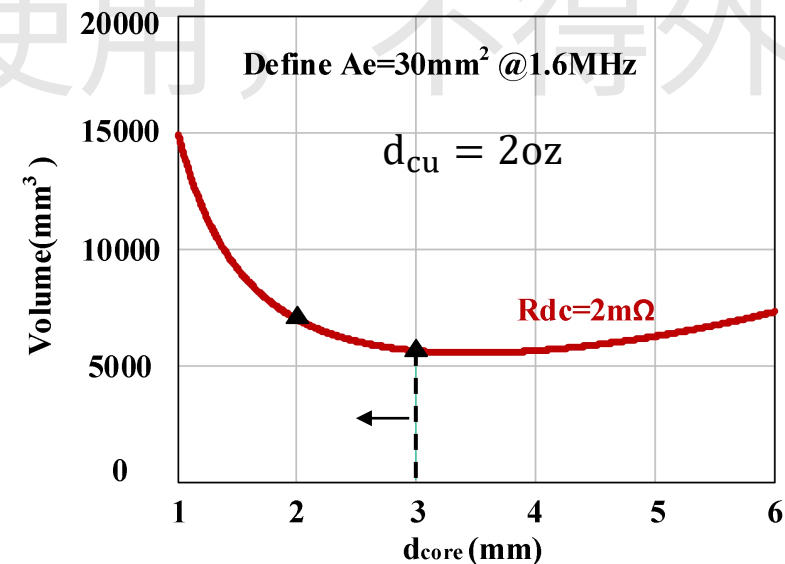
$$= 4 \left[M_e \left(d_{core}^2 + \frac{A_e^2}{d_{core}^2} \right) + N_e \right] (d_{core} + d_{board})$$

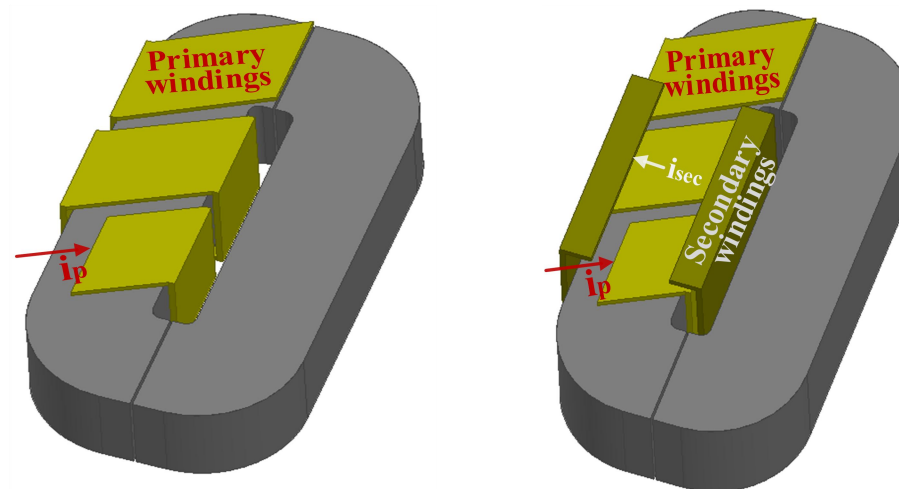
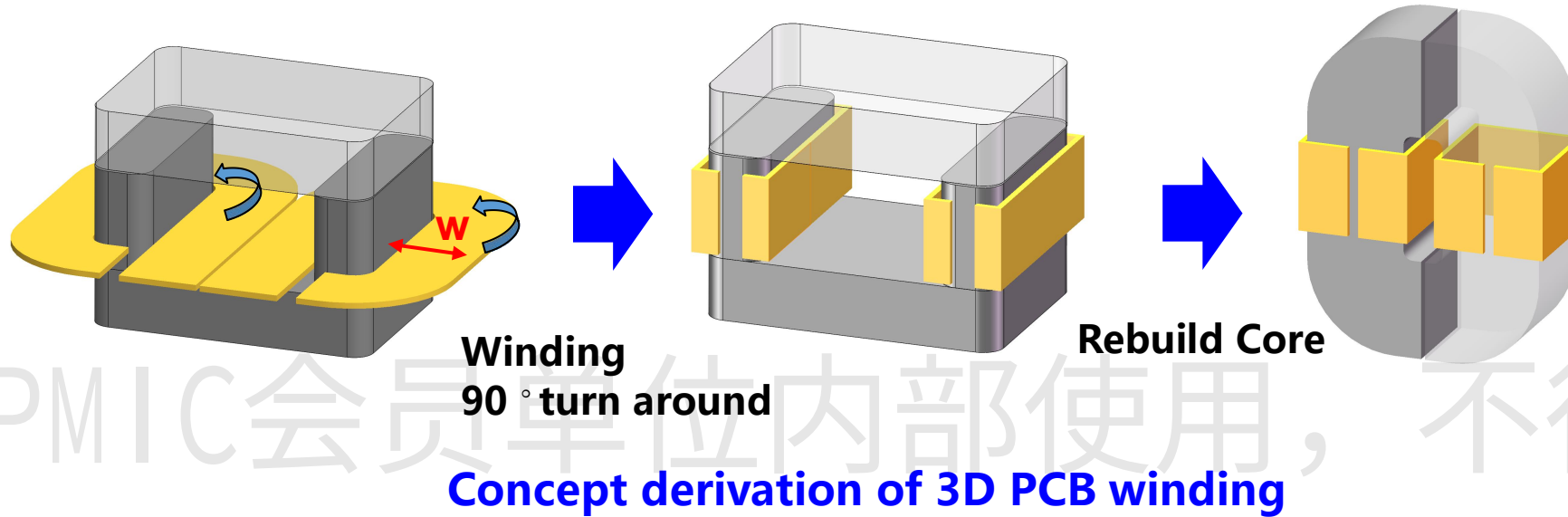
$$M_e = 2\alpha(2\alpha + 1), N_e = A_e[(2\alpha + 1)^2 + (2\alpha)^2], \alpha = \frac{2\rho}{d_{cu} \cdot R_{dc} - 4\rho}$$

R_{dc} - DC resistance for one turn of the winding

ρ - Resistivity of the copper

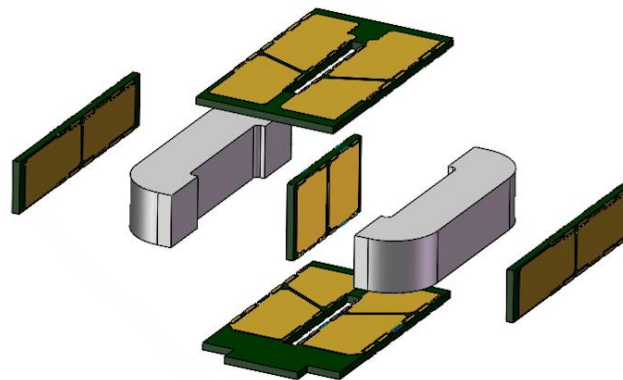
d_{cu} - Thickness of the copper



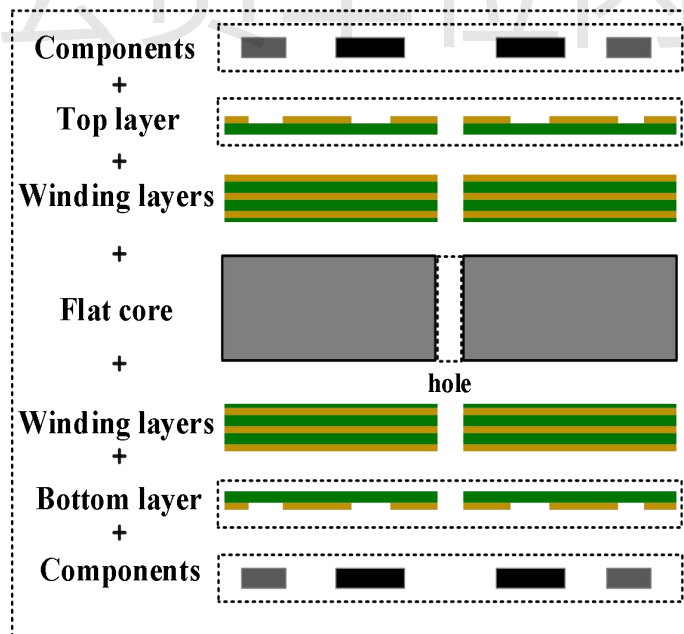


3D PCB windings of Transformer structure

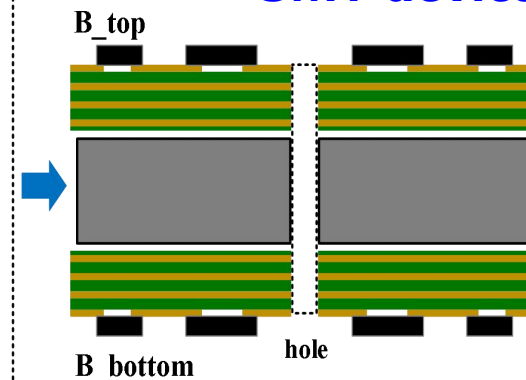
Multilayer PCB
winding



Cross Section

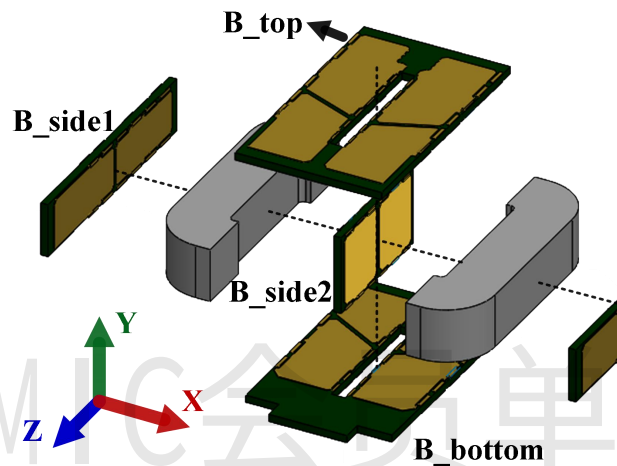


Integrated winding +
SMT devices

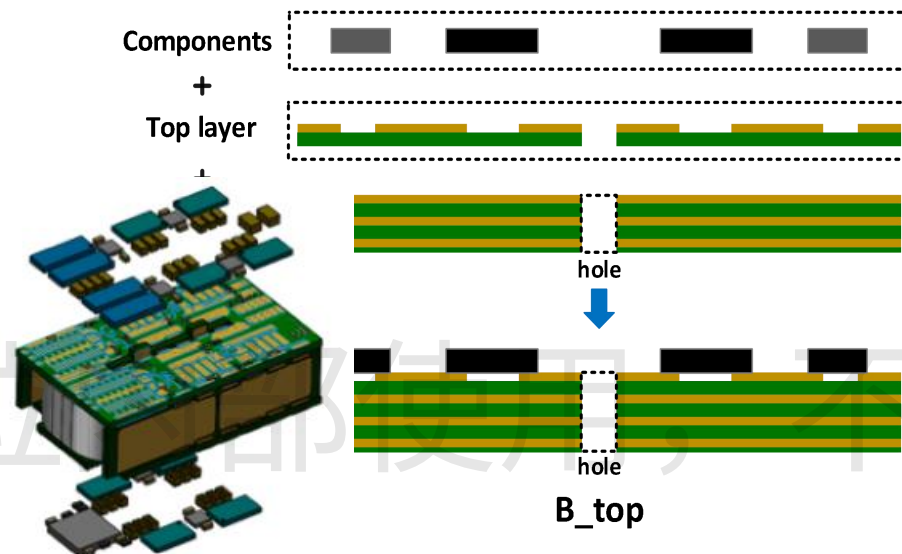


Construction of 3D-PCB Winding

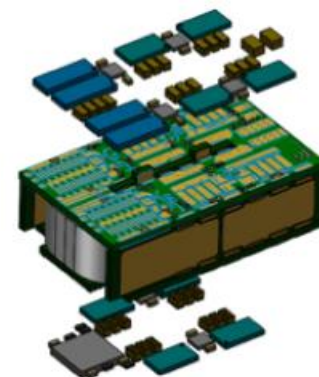
➤ Explosion diagram of the proposed transformer



3-D PCB winding transformer

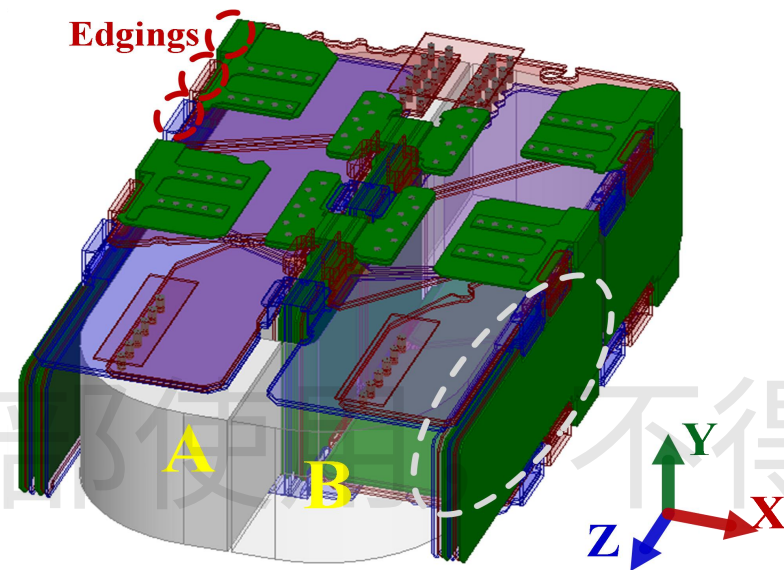
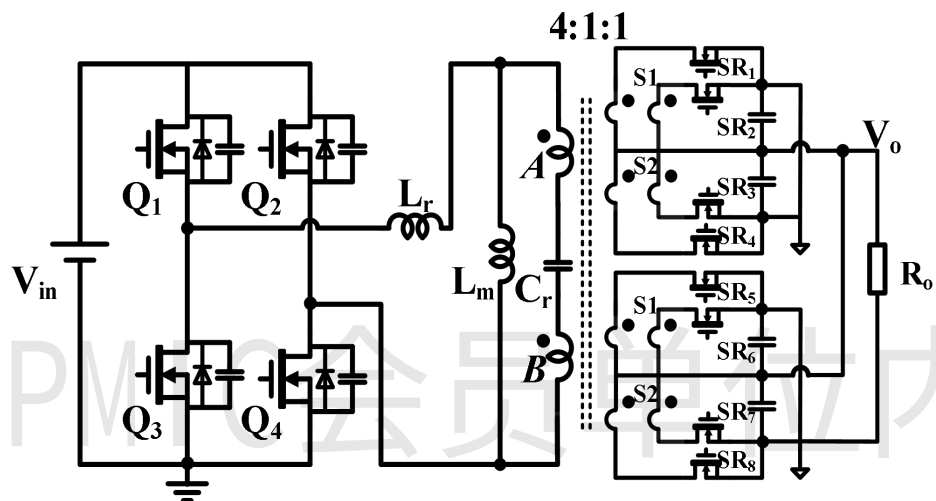


The space of the whole converter is used efficiently

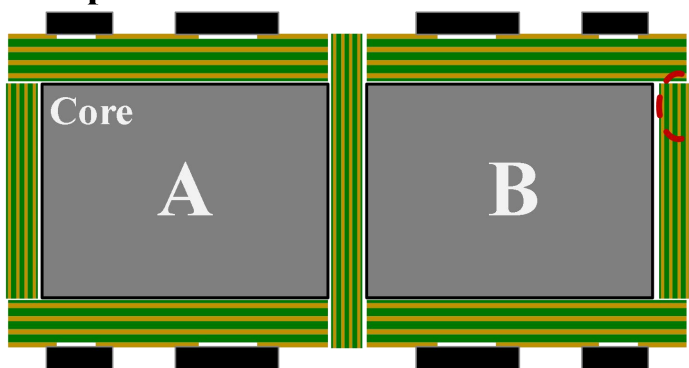


Design of the 3D PCB windings

➤ 48V/12V Series resonant converter



components



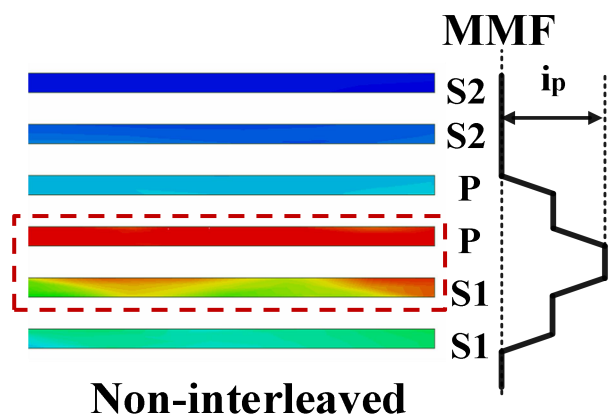
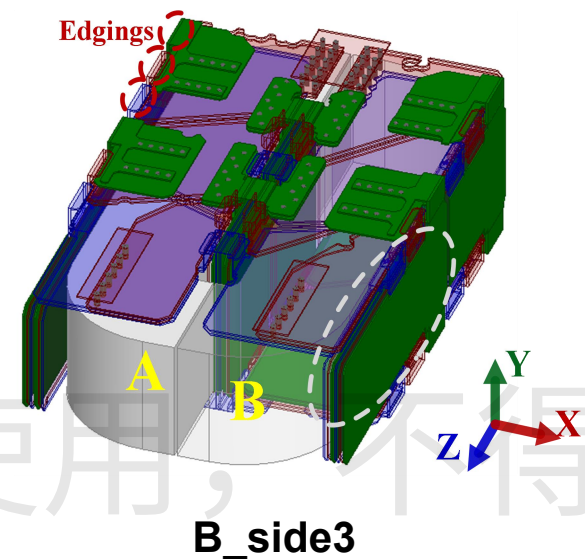
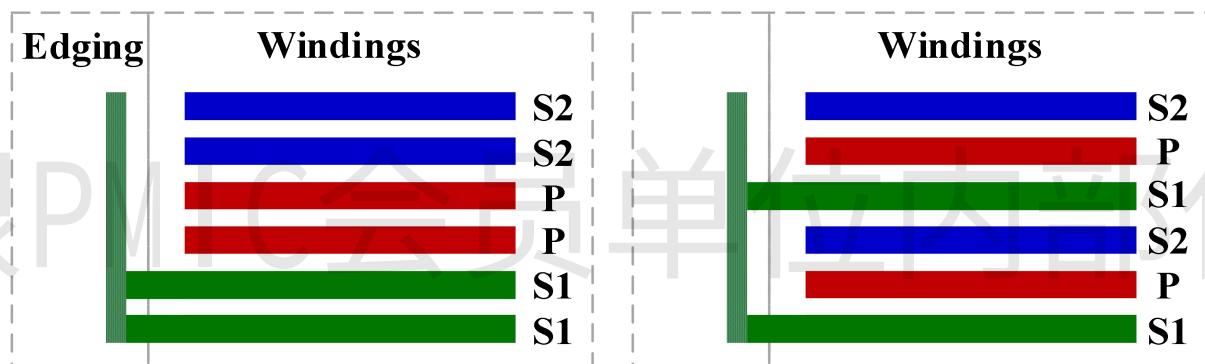
PCB layers
B_side3

B_side3

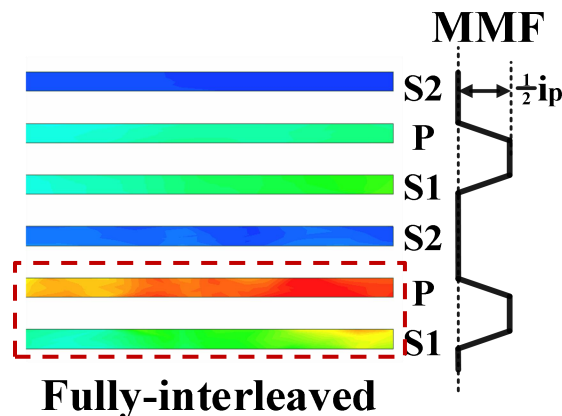
P - The primary windings
S1&S2 - The secondary windings

➤ Optimizing the winding arrangement

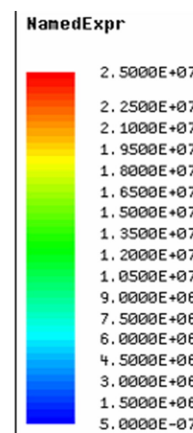
■ $F_s = 1.6\text{MHz}$



Non-interleaved

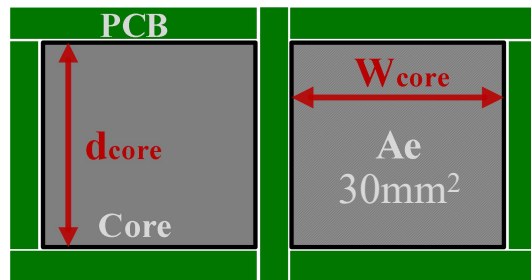


Fully-interleaved



Determination of the Core Height

■ $F_s=1.6\text{MHz}$, $A_e=30\text{mm}^2$



Larger D_{core}
Less W_{core}

Cross section

$$W_{\text{core}} = \frac{A_e}{d_{\text{core}}}$$

Same ac resistance coefficient → Fixed R_{dc}

$$V_{\text{Tr}}'(d_{\text{core}}, R_{\text{dc}}) =$$

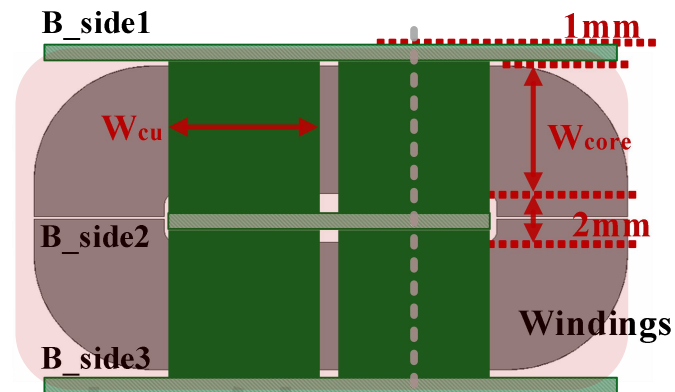
$$\left[(4\alpha' + 4) \frac{A_e^2}{d_{\text{core}}^2} + (8\alpha' + 8) \frac{A_e}{d_{\text{core}}} + 8\alpha' d_{\text{core}} + 4\alpha' A_e \right] (d_{\text{core}} + d_{\text{board}})$$

$$\alpha' = \frac{2\rho}{d_{\text{cu}} \cdot R_{\text{dc}}}$$

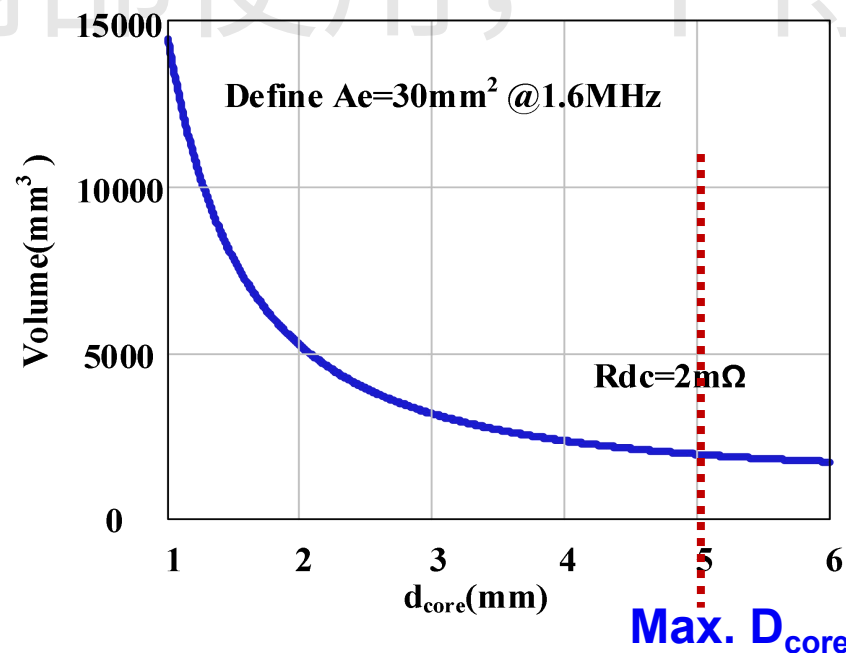
R_{dc} - DC resistance for one turn of the winding

d_{core} - thickness of the copper

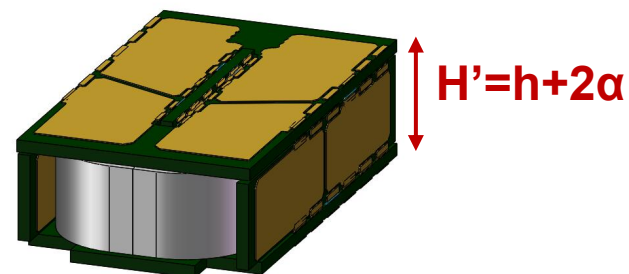
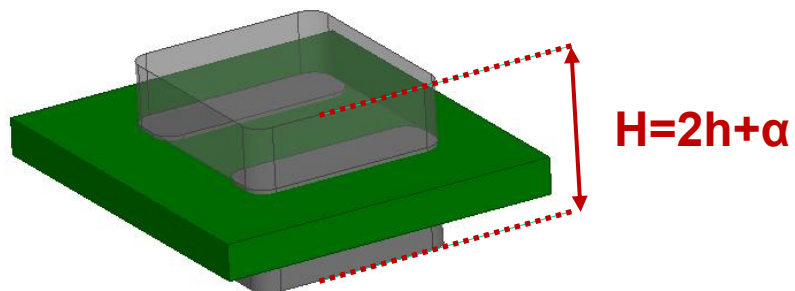
d_{board} - thickness of the PCB



Required surface area for components amount, leads to maximum D_{core}

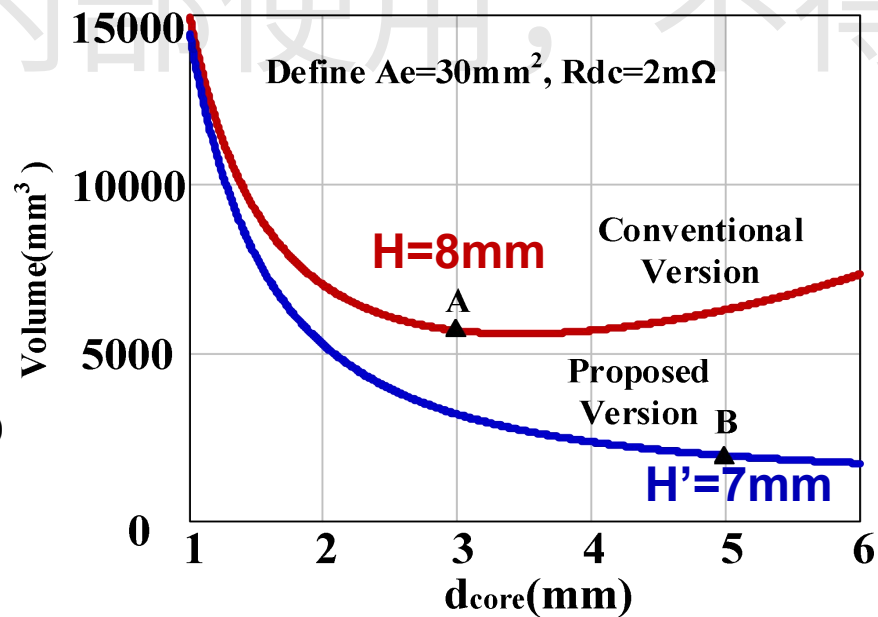


Design of the proposed transformer



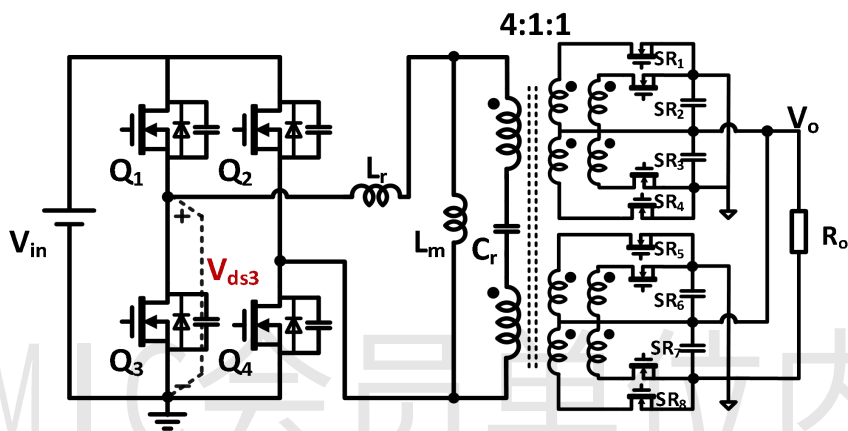
$$V_{Tr}(d_{core}, R_{dc}) = 4 \left[M_e \left(d_{core}^2 + \frac{Ae^2}{d_{core}^2} \right) + N_e \right] (d_{core} + d_{board})$$

$$V_{Tr}'(d_{core}, R_{dc}) = \left[(4\alpha' + 4) \frac{Ae^2}{d_{core}^2} + (8\alpha' + 8) \frac{Ae}{d_{core}} + 8\alpha' d_{core} + 4\alpha' Ae \right] (d_{core} + d_{board})$$

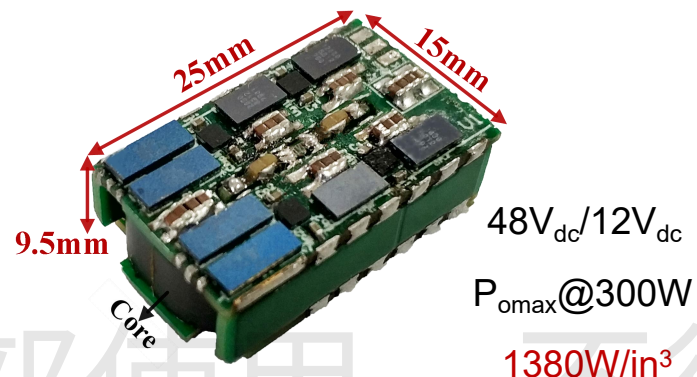


Prototype parameters and Specifications

➤ Main circuit

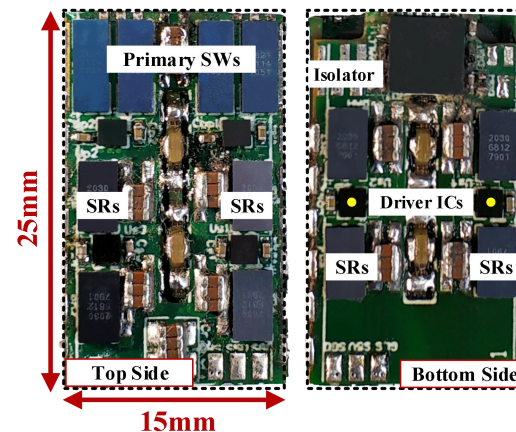


➤ Photo of the prototype



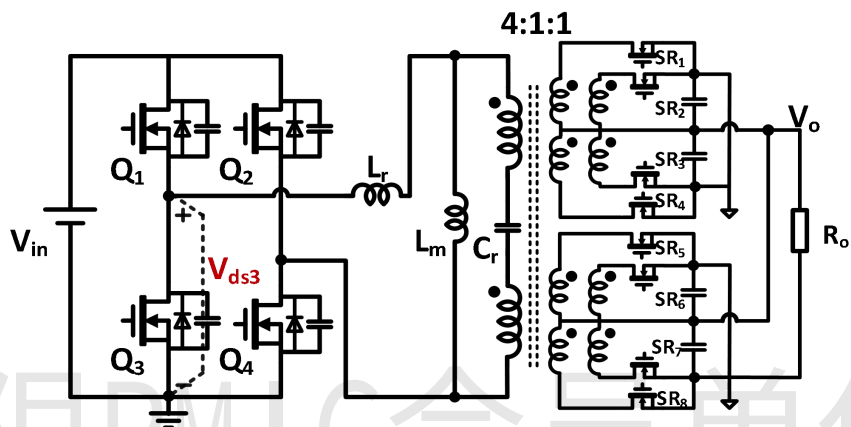
➤ Key parameters

V_{in}	48V	V_o	12V
I_o	25A	f_s	1.6MHz
Q1~Q4	EPC2021	T	4:1:1
SR1~SR8	EPC2030	Core	DMR51W



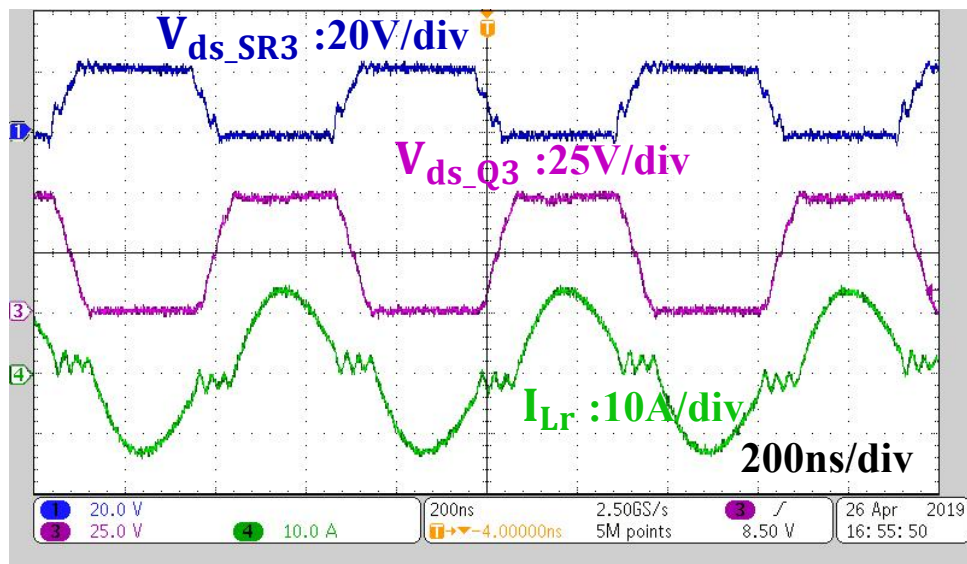
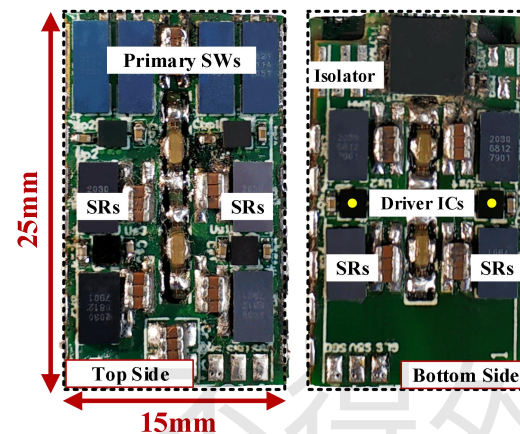
Prototype and Primary Key Waveforms

➤ Main circuit

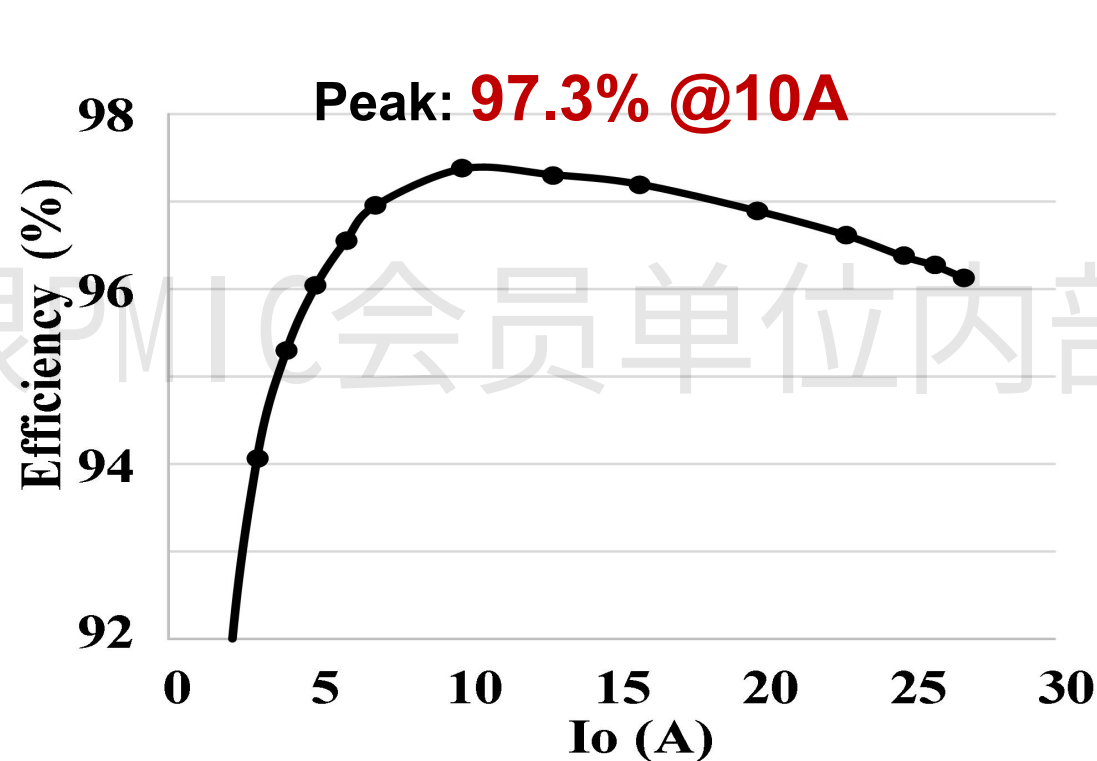


V_{in}	48V
V_o	12V
I_o	25A
f_s	1.6MHz

➤ Key parameters



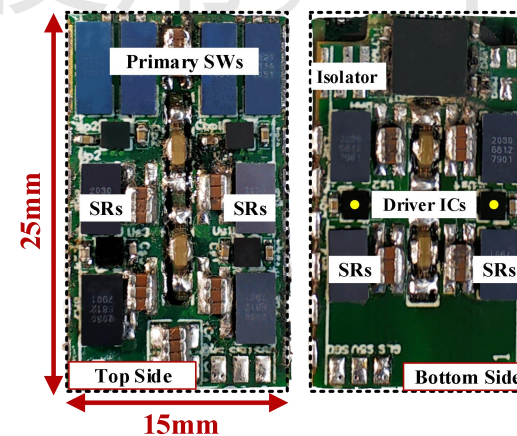
Efficiency and power density



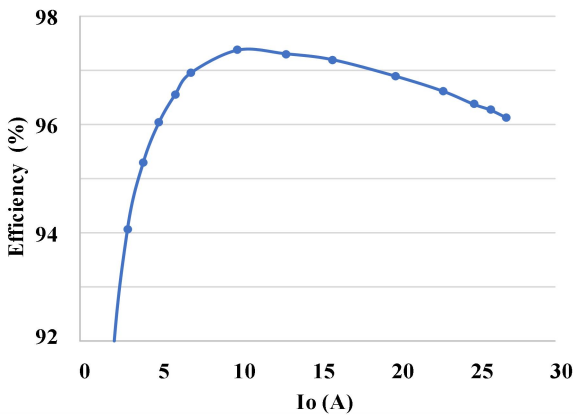
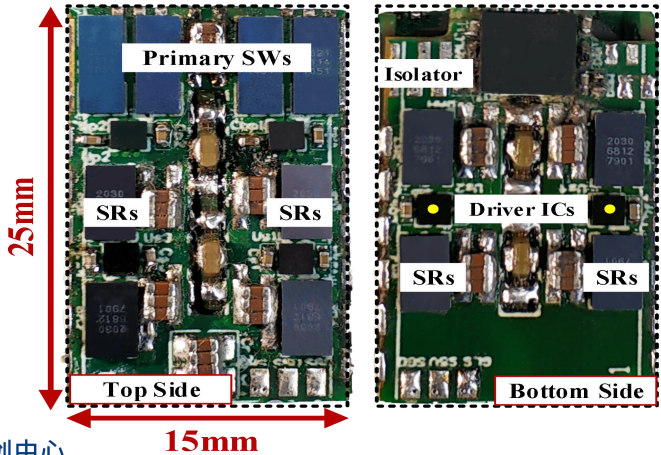
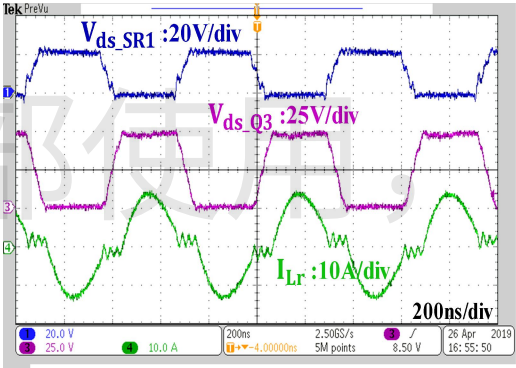
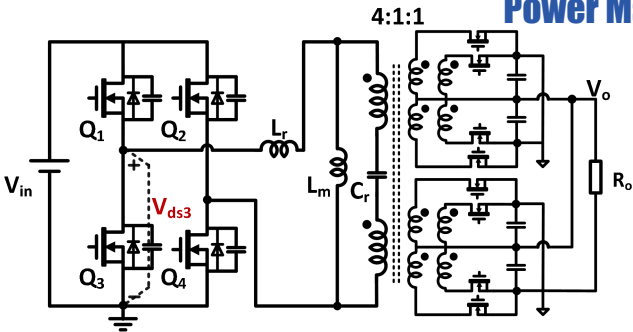
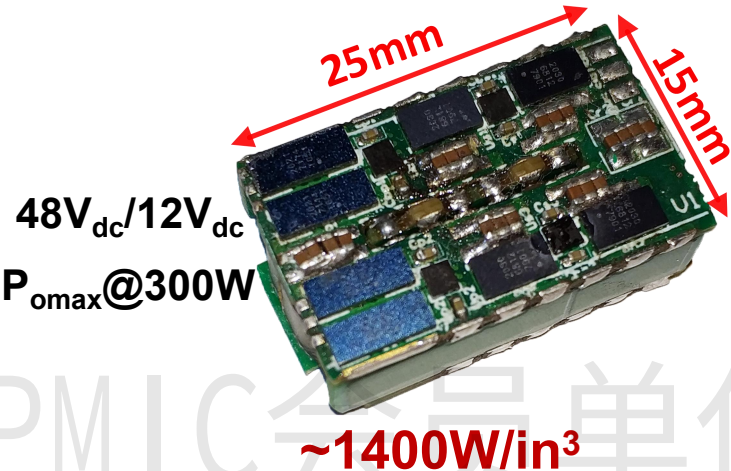
$48V_{dc}/12V_{dc}$

$P_{omax}@300W$

1380W/in³
without considering Bias



48V-12V DCX Prototype



- ❑ A 3-D PCB winding transformer is proposed for high density dcx converter
- ❑ The devices can be surface mounted on the PCB winding
- ❑ The manufacturing process should be further investigated

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1. The ZVS on and ZCS off for MHz DC-DC converter are necessary ,whatever for 48 or 380V applications.
2. Single switch DCX topologies are preferred for low power (<100W) low voltage application at MHz frequency.
3. The topologies for ZVSZCS MHz DCXs can be derived by integrating unidirectional resonant tanks.
4. The tight regulation of the MHz converter can be implemented by partial voltage (power) regulation.
5. The partial voltage (power) regulation topology (RDCX) can be derived according to the inserting points of two-ports network structure. Different RDCX topologies have different suitable voltage range and different nominal operating points.
6. Cellular circuit structure with low voltage MOSFETs can be utilized to improved the switching frequency and efficiency for high voltage applications at MHz frequency.



***Thank You _{for}
Your Attention***

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