高效率高密度AC/DC变流 技术研究

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高效高密度AC/DC变流技术应用

Power Management Innovation Consortium

空间电源

雷达电源

全电飞机

电动汽车

高密度
高效率

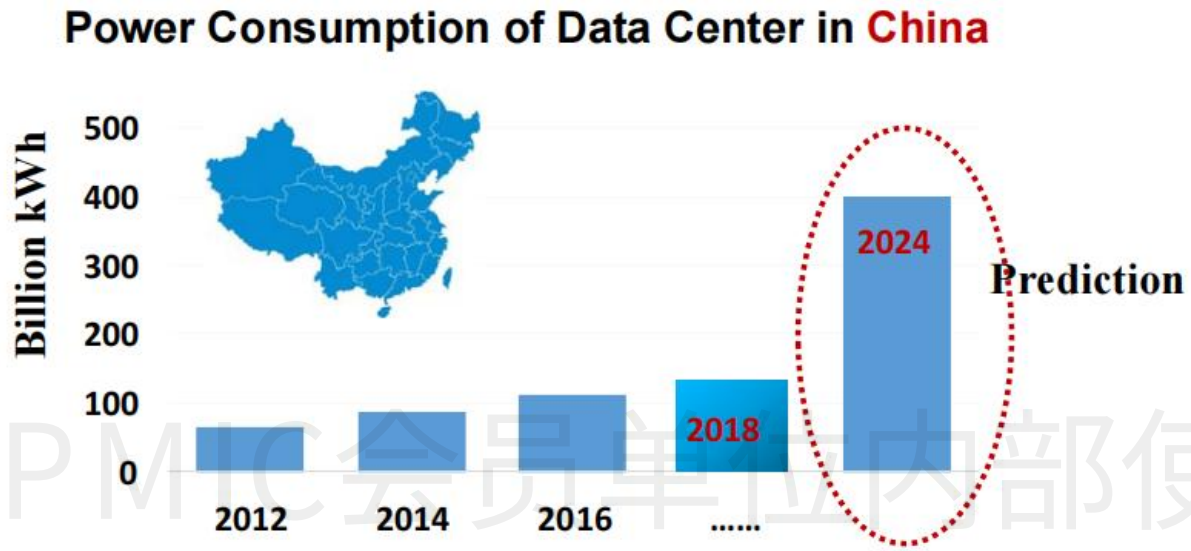
数据中心服务器电源

轨道交通

5G通讯电源

便携设备电源

中国数据中心的耗能



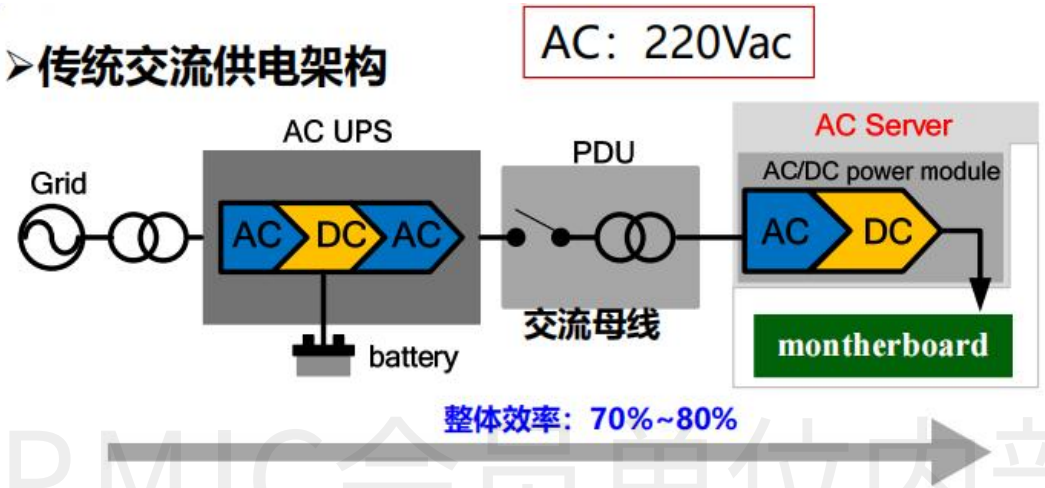
- > 4000亿 kWh
- 5%-8% 总耗电量

[1] 吕天文. 人工智能浪潮下的数据中心趋势分析, 2018, http://www.gdctech.org/c41581.jsp

[2]闫志强,中国能源报.数据中心粗放发展节能降耗潜力大, 2016, http://paper.people.com.cn/zgnyb/html/2016-05/30/content_1684451.htm

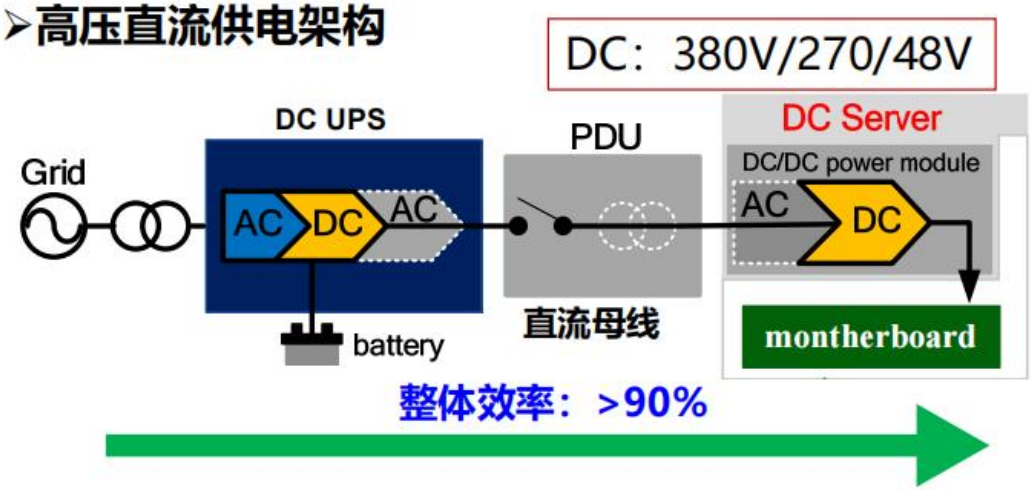
数据中心服务器的电源系统

➢传统交流供电架构



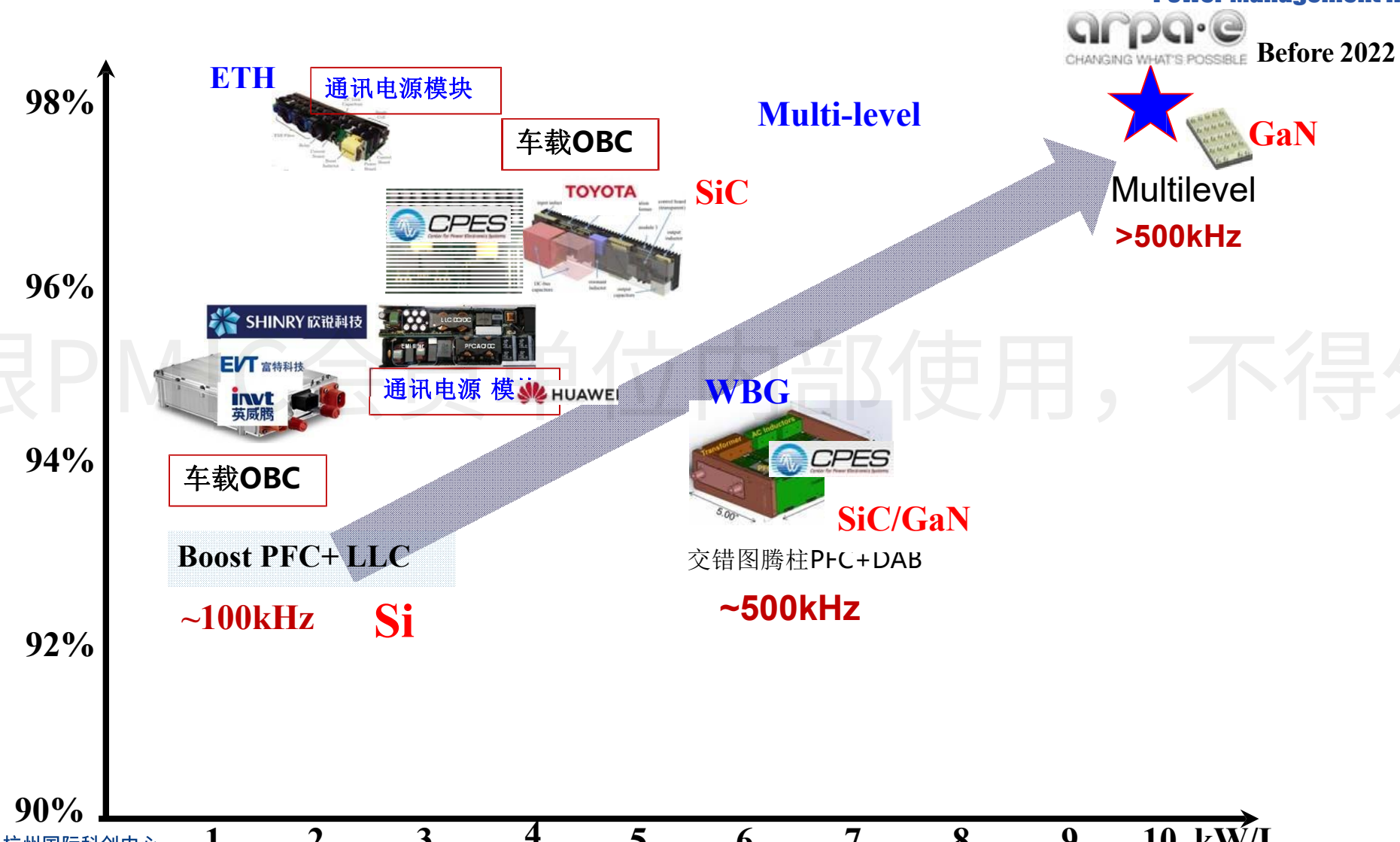
数据中心服务器

➢高压直流供电架构



- ◆转换级数少
- ◆整体效率高
- ◆成本低
- ◆易扩展

单相AC/DC变流器的功率密度和效率现状与趋势

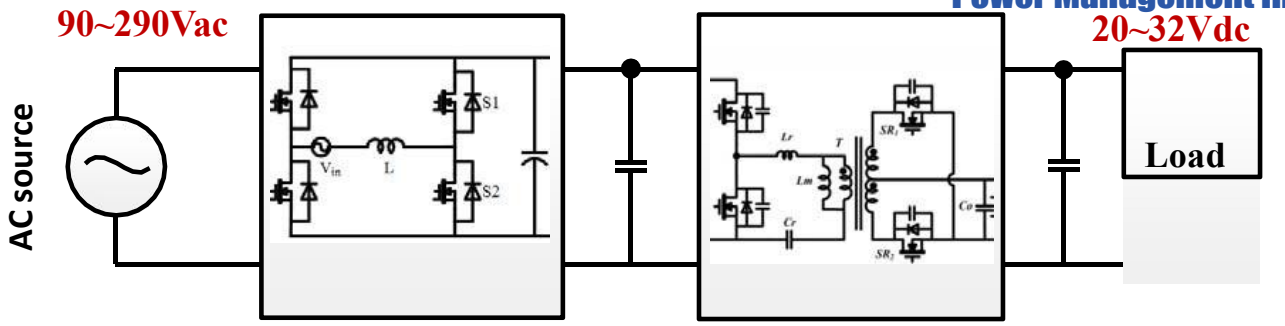


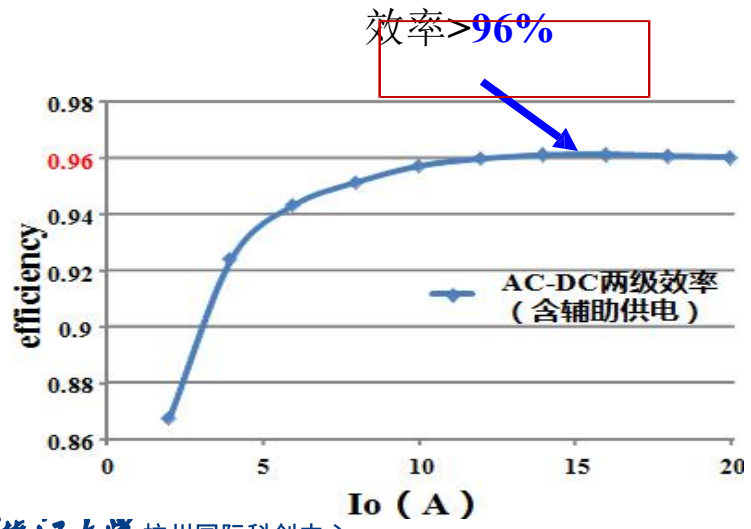
单相AC/DC电源的体积分析

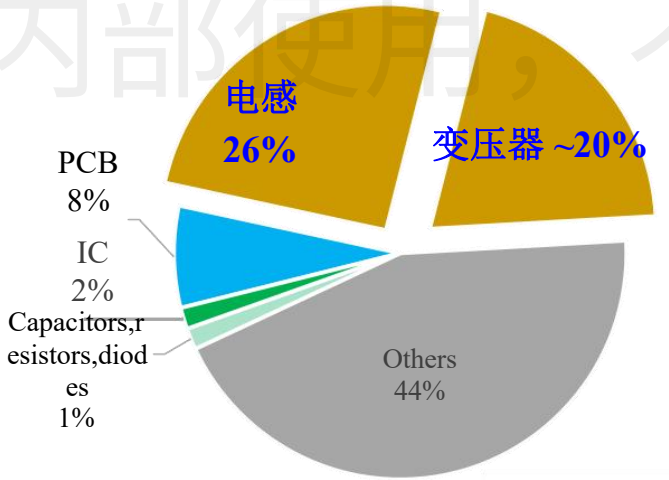
600W AC/DC 模块 (W/O E-Cap)

功率密度：~185 W/in³

80k~200kHz



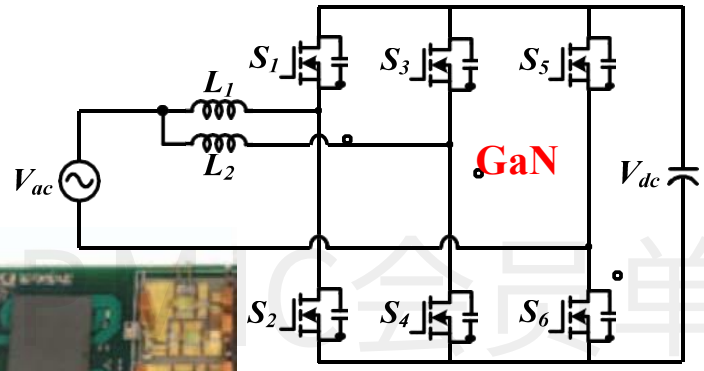


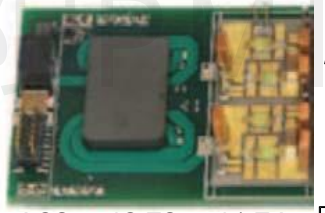


磁元件体积 >46%

基于GaN的高密度交错图腾柱 PFC

Two-level totem-pole PFC



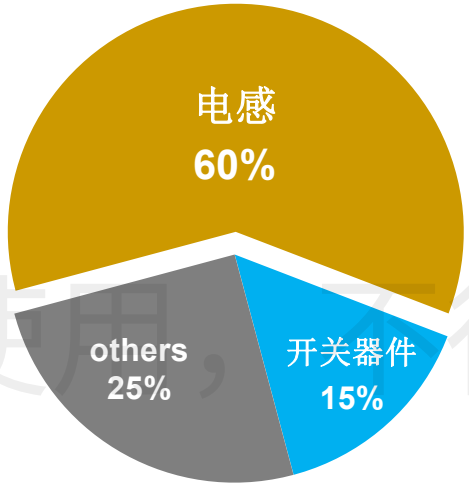


4.32cm*3.72cm*1.74cm

1 MHz frequency

功率密度：~550 W/in³

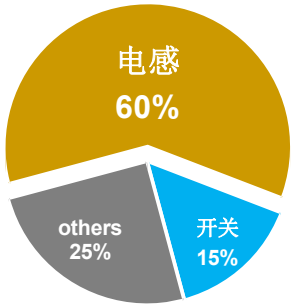
Volume breakdown



Inductor takes the largest volume

F. C. Lee, "Application of GaN devices for 1 kW server power supply with integrated magnetics," in CPSS Transactions on Power Electronics and Applications, vol. 1, no. 1, pp. 3-12, Dec. 2016.

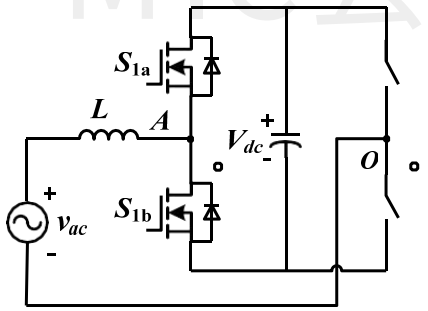
电感尺寸与多电平的关系



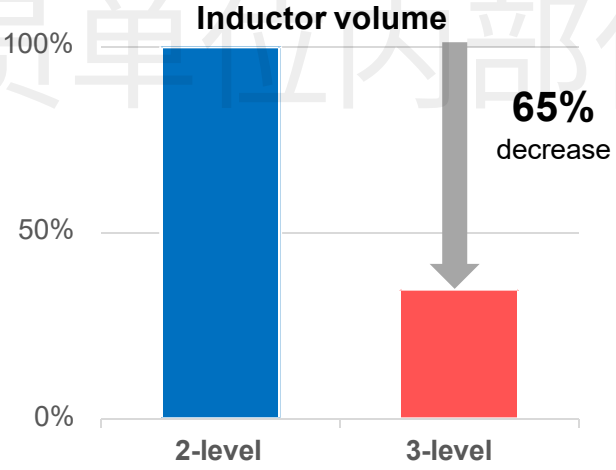
Volume breakdown

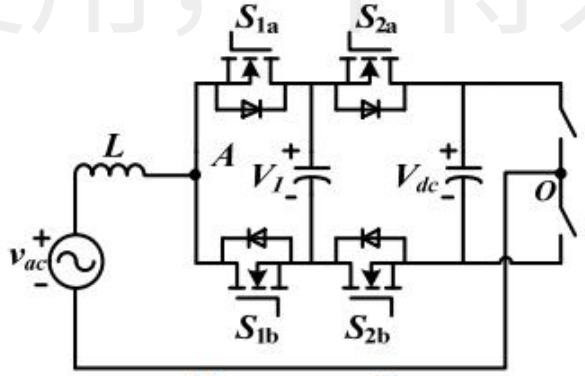
Inductance: $$L = \frac{1}{f_s} \frac{V_{dc}}{(N_{level}-1)^2} \frac{1}{4\Delta i_{L\_\max}}$$

$$Volume \approx k_L \left(\frac{I_p I_{RMS}}{k_w J B_m}\right)^{3/4} L^{3/4}$$



$N_{level} = 2$



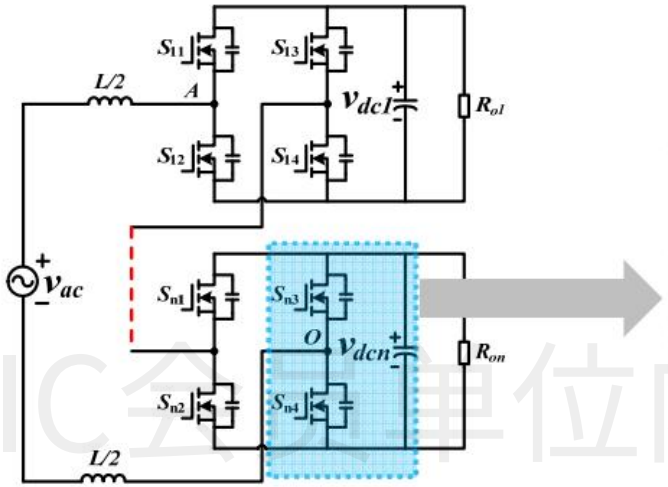


$N_{level} = 3$

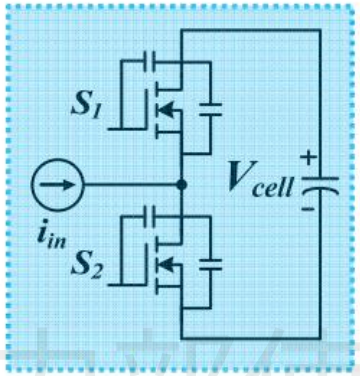
W. G. Hurley, “Transformers and inductors for power electronics :theory, design and applications,"
Y. Lei *et al*., "A 2-kW Single-Phase Seven-Level Flying Capacitor Multilevel Inverter With an Active Energy Buffer," TPEL, Nov. 2017.
Y. Lei, W. Liu and R. C. N. Pilawa-Podgurski, "An Analytical Method to Evaluate …," IEEE TPEL, March 2018.

基于GaN的多电平拓扑最小损耗建模

以CHB 拓扑为例



基于GaN器件的CHB 整流拓扑



$$V_{cell} = \frac{V_{dc}}{N_{cells}}$$

Cell numbers N_{cells}

$$P_{GaN} = k_{temp}k_{dyn}I_{in}^2R_{ds\_on} + \frac{V_{cell}(I_{in}k_gFoM_{HS} + FoM_{oss})f_s}{R_{ds\_on}}$$

单桥臂损耗

$$\begin{cases} FoM_{oss} = Q_{oss}R_{ds\_on} \\ FoM_{HS} = (Q_{gs2} + Q_{gd})R_{ds\_on} \end{cases}$$

$$P_{GaN\_\min} = 4I_{in}\sqrt{N_{cells}V_{dc}k_{temp}k_{dyn}(k_gI_{in}FoM_{HS} + k_2FoM_{oss})f_s}$$

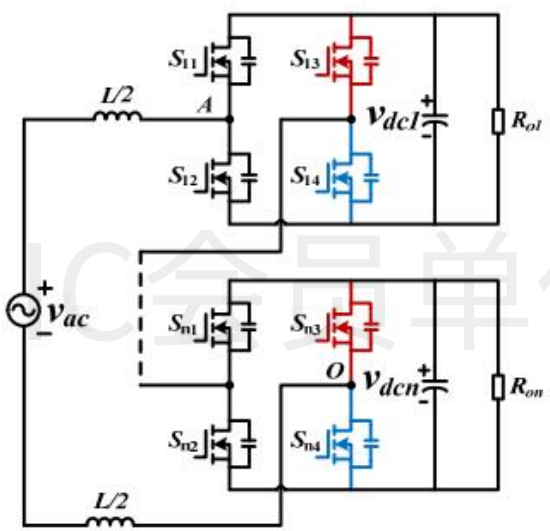
器件总损耗（最小值）

J. W . Wu and X.K Wu, "FoM Based Optimal Frequency and Voltage Level Design …," *IEEE APEC*, 2020, pp. 1911-1915.
D. Reusch, et_al, "Improving System Performance with eGaN® FETs in DC-DC Applications" ,IMAPS2013, pp.764-769.

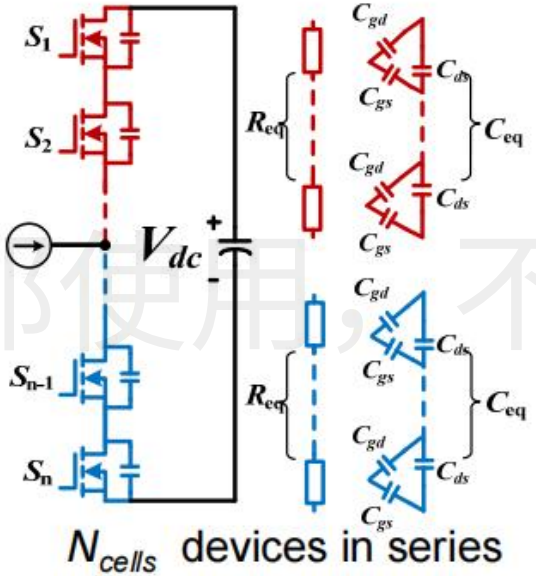
简化的多电平Boost电路最小损耗模型

简化后 $$P_{GaN\_min} = 4V_{dc}I_{in}\sqrt{k_{temp}k_{dyn}(k_g I_{in}(1+k_{g2d})C_{gd(tr)}R_{ds\_on} + C_{oss(er)}R_{ds\_on})f_s}$$

C：器件寄生电容



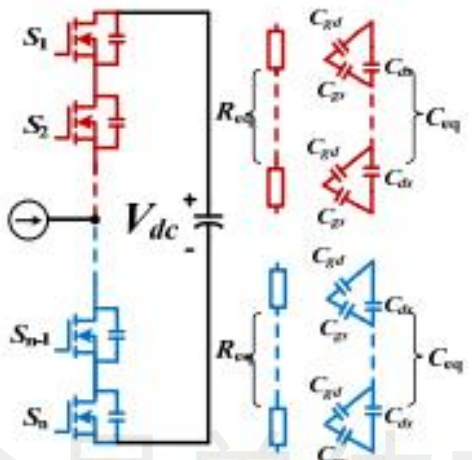
损耗等效



多个串联器件 $$C_{eq} \times R_{eq} = \frac{C_{oss(er)}}{N_{cells}} \times N_{cells} R_{ds\_on} = NFoM_{oss}$$ 单个低压器件

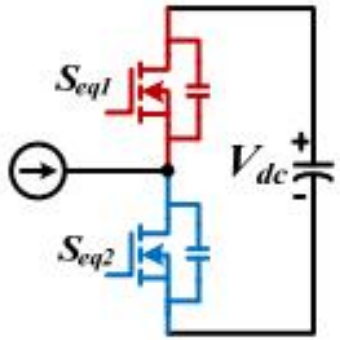
J. W . Wu and X.K Wu, “FoM Based Optimal Frequency and Voltage Level Design …,” *IEEE APEC*, 2020, pp. 1911-1915.

多电平Boost电路损耗的统一模型



N_{cells} devices in series

进一步等效



Two level bridge

多个串联器件 $C_{eq} \times R_{eq} = C_{oss(er)} R_{ds\_on} = NFoM_{oss}$ 单个低压器件

$$\begin{cases} NFoM_{sw} = C_{gd(tr)} R_{ds\_on} \\ NFoM_{oss} = C_{oss(er)} R_{ds\_on} \\ k_{sw} = k_g (1 + k_{gs}) \end{cases}$$

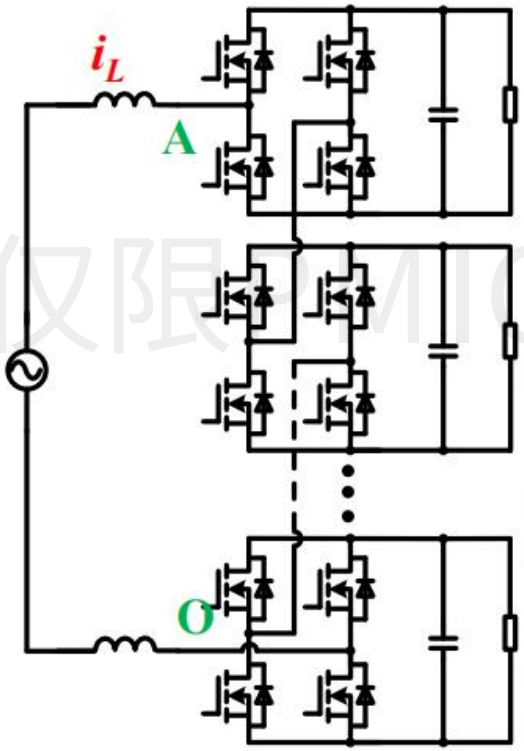
$$P_{GaN\_min} = 4 V_{dc} I_{in} \sqrt{k_{temp} k_{dyn} (k_{sw} I_{in} NFoM_{sw} + NFoM_{oss}) f_s}$$

Boost多电平拓扑的器件损耗统一模型

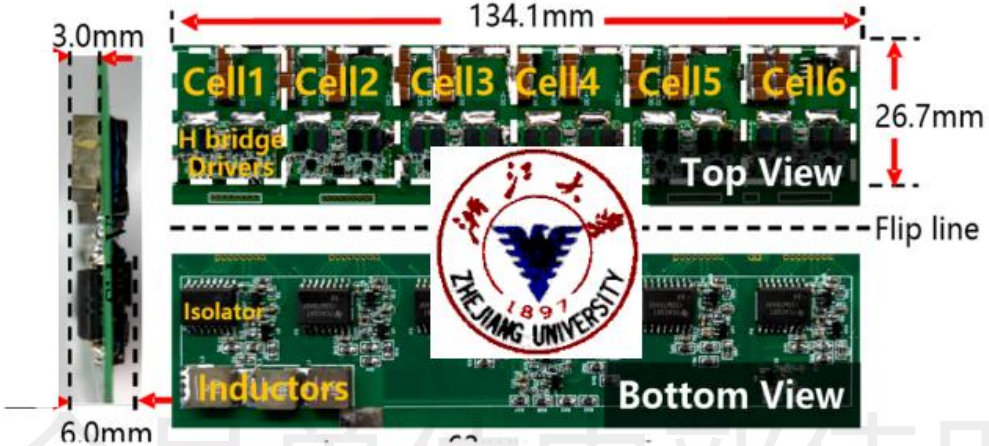
J. Wu and X. Wu, "FoM Based Optimal Frequency and Voltage Level Design ...," *IEEE APEC*, 2020, pp. 1911-1915.

基于CHB 拓扑的高效率高密度PFC

基于商业化GaN器件



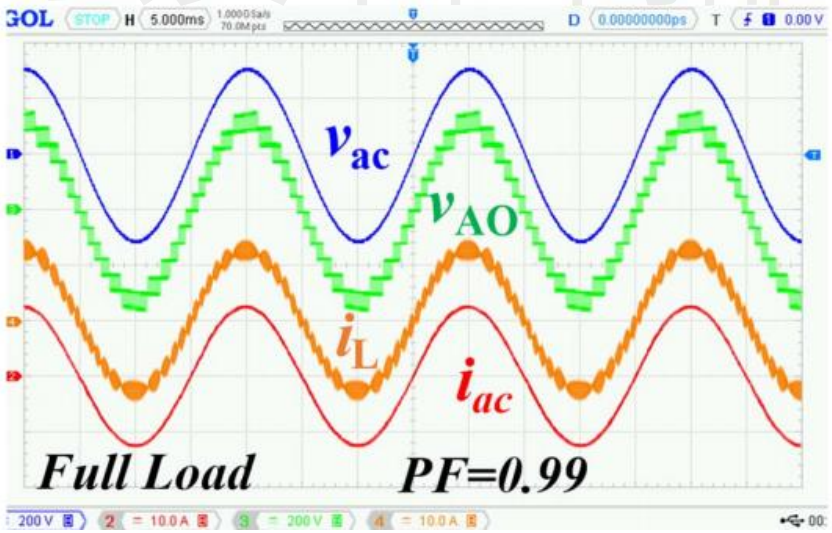
6-cell CHB PFC



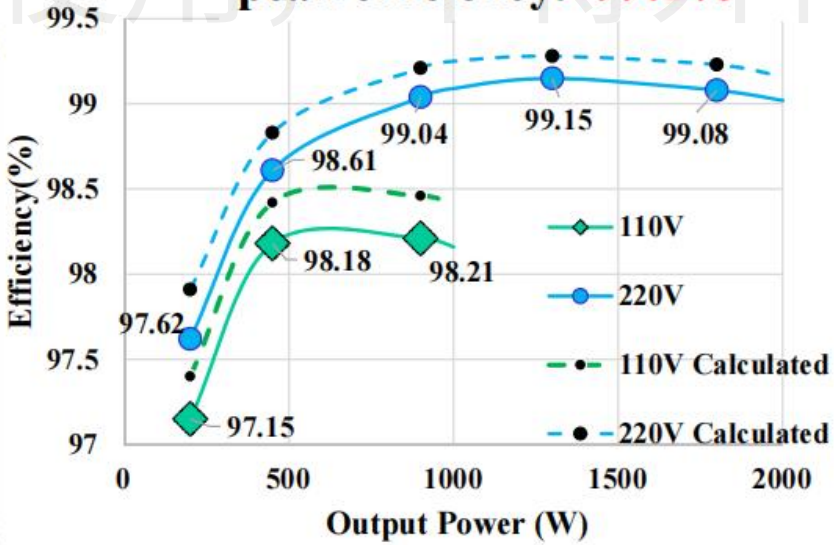
fs: ~60kHz

~1.3 kW/in³

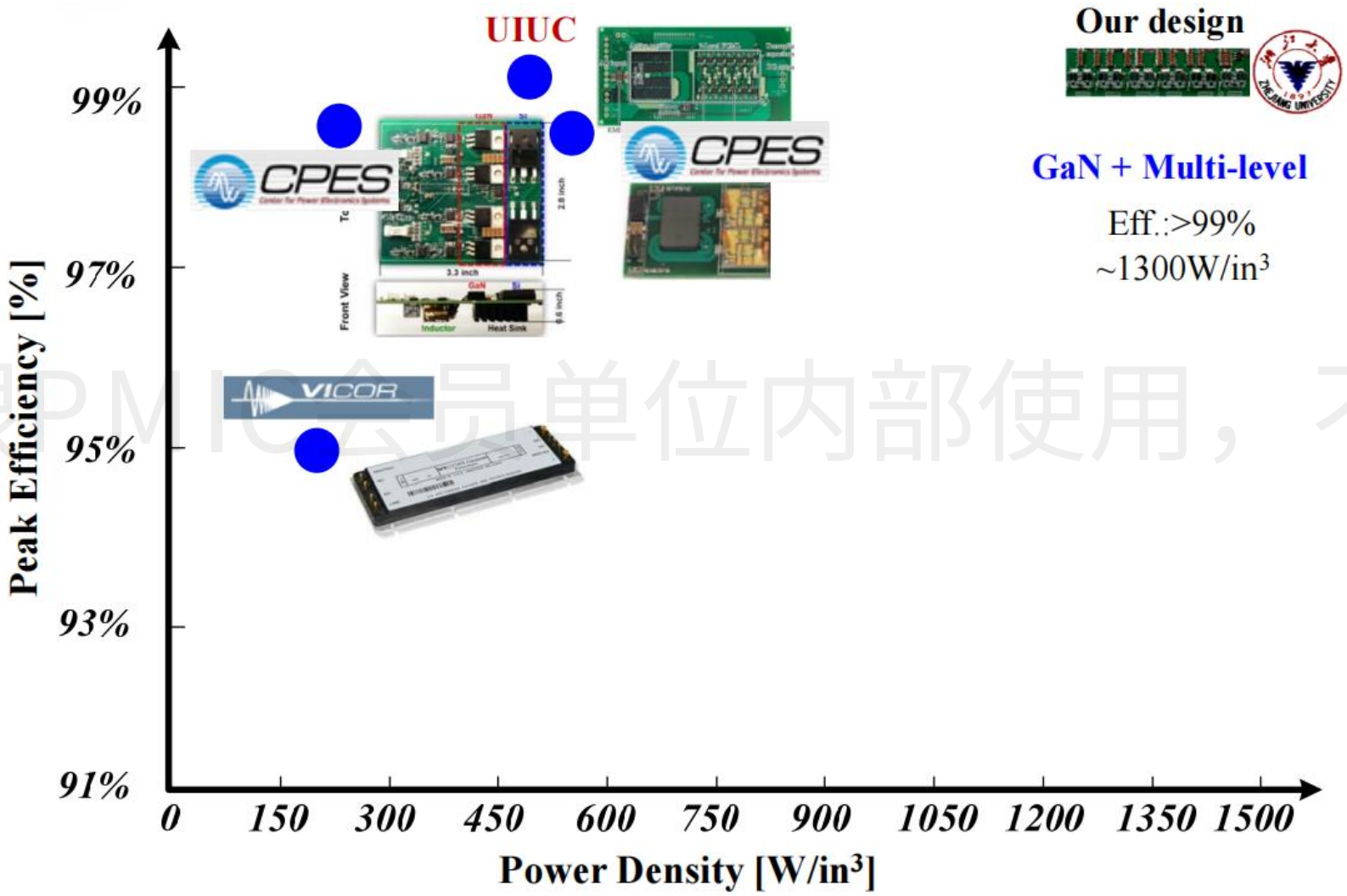
(Main circuit)



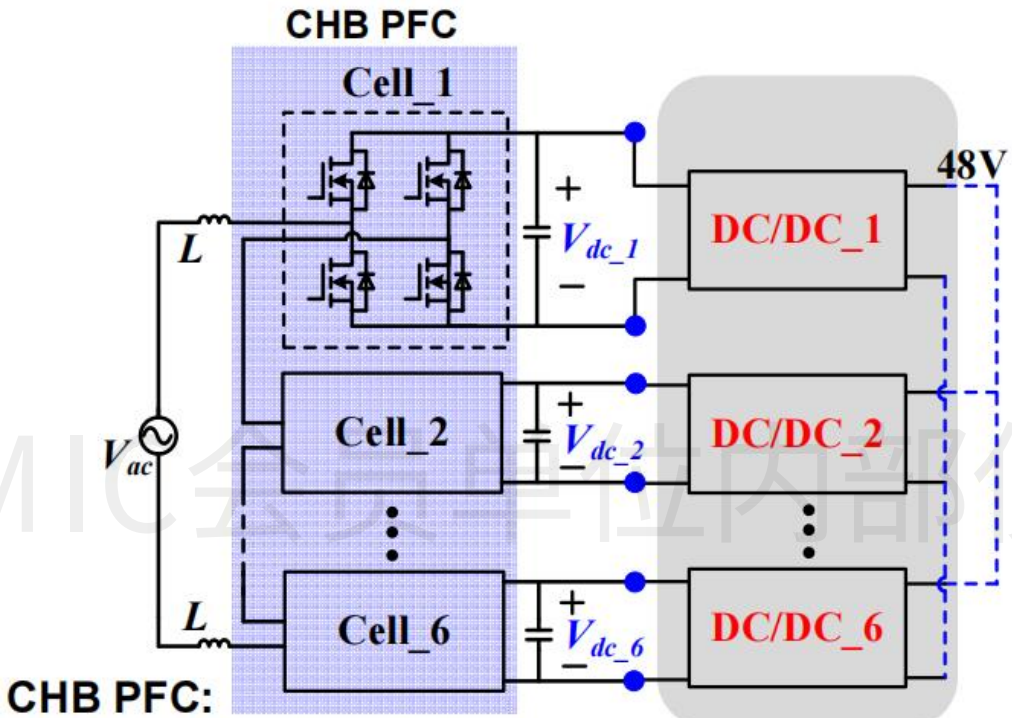
peak efficiency:>99.1%



单相PFC样机功率密度与效率比较



AC/DC: CHB单相多电平PFC拓扑+DC/DC

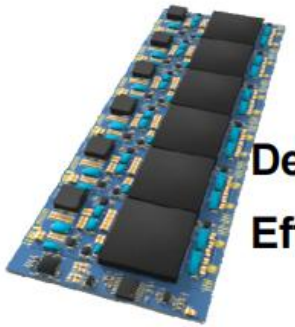


- 48V output series/parallel
- Tight regulated

CHB PFC:

Density: ~1300W/in³

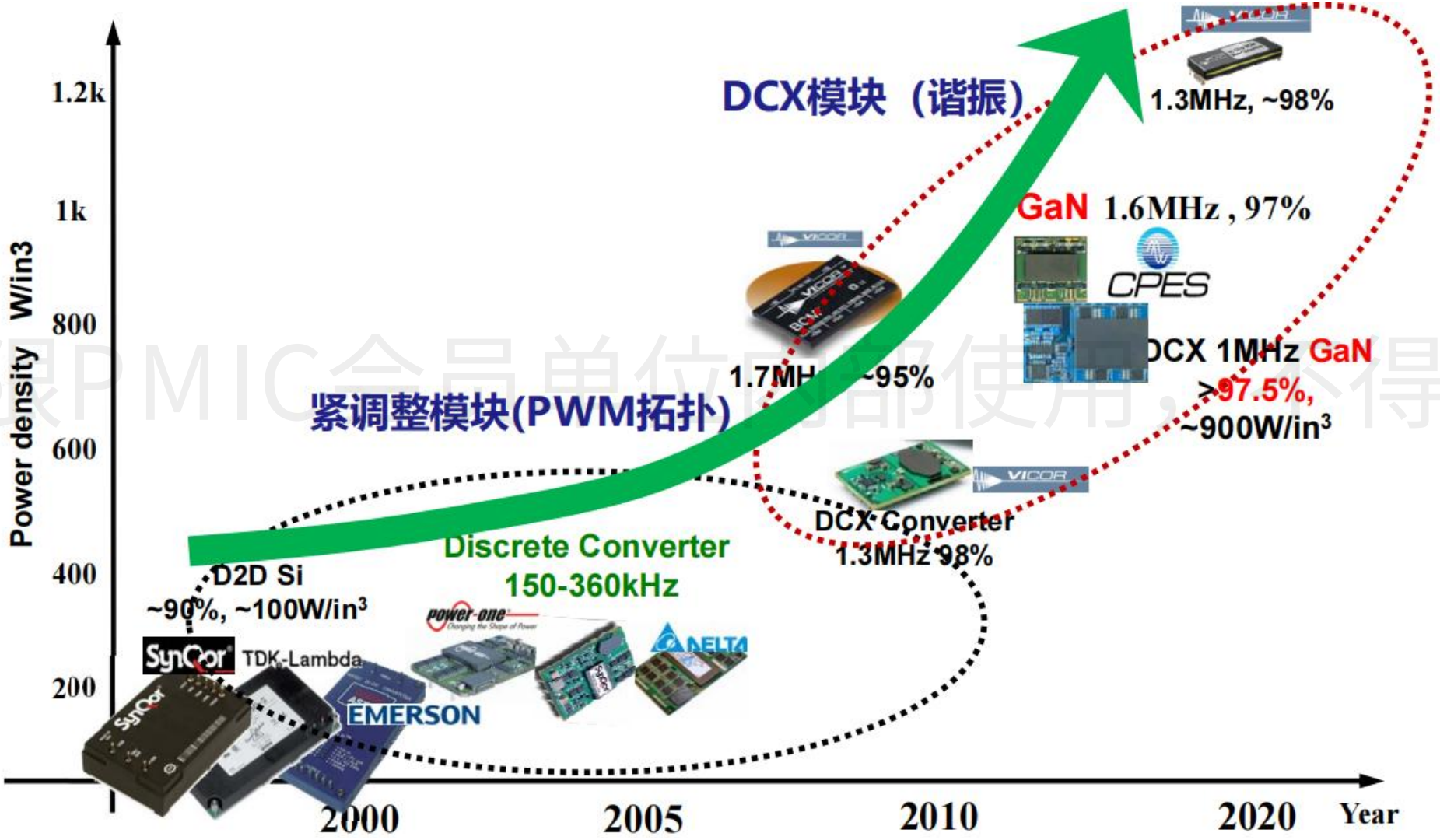
Efficiency: >99%(@220Vac)



Density: ~1300W/in³

Efficiency (@full load): >98% @1MHz

隔离型DC/DC模块的功率密度趋势



MHz高频谐振DCX模块的通用拓扑

VICOR

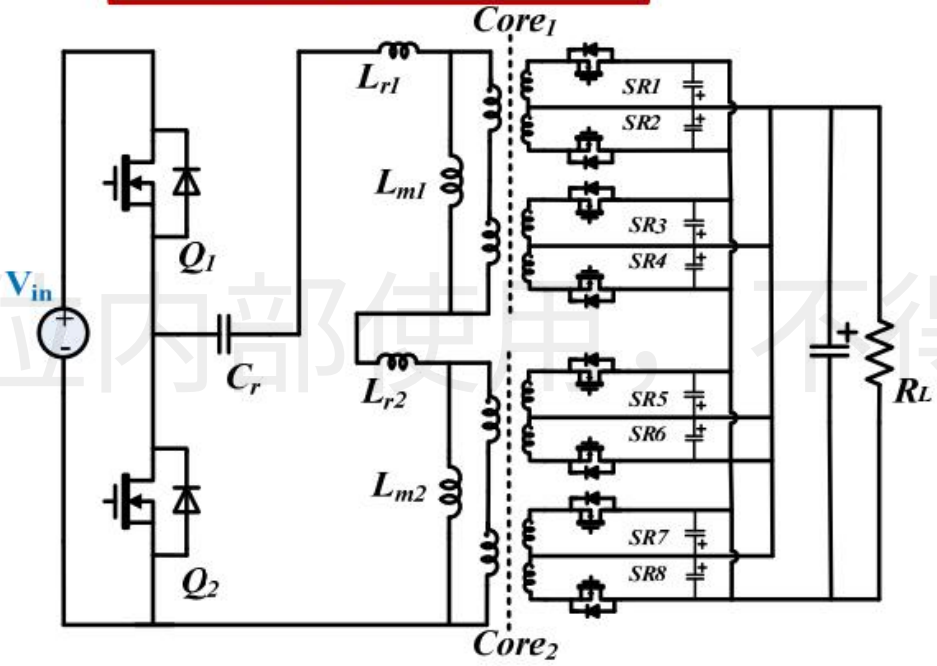
1.3MHz, ~98%

CPES GaN

DCX 1MHz GaN
4 Layer PCB
97.5%,900W/in³
(2016)

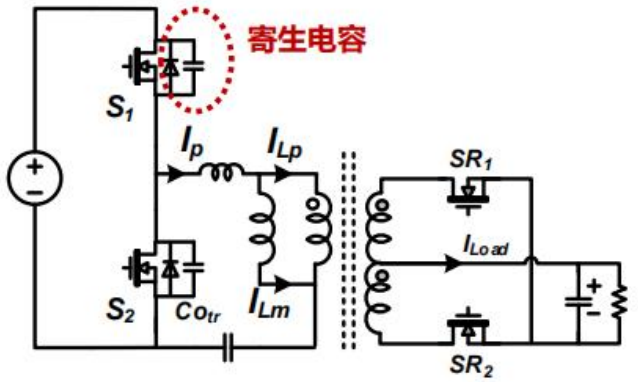
1.6MHz , 97%

- LC 串联谐振拓扑
- 矩阵变压器

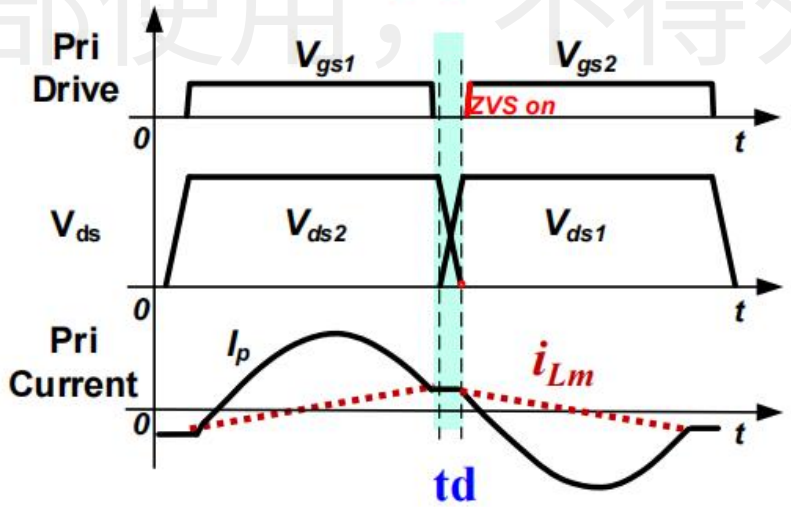


- ☺ 零电压开通 ZVS on
- ☺ 零电流关断 ZCS off
- ☺ 副边没有反向恢复损耗

超高功率密度DCX



fs≈fr



开关损耗可忽略

DCX导通损耗数学模型

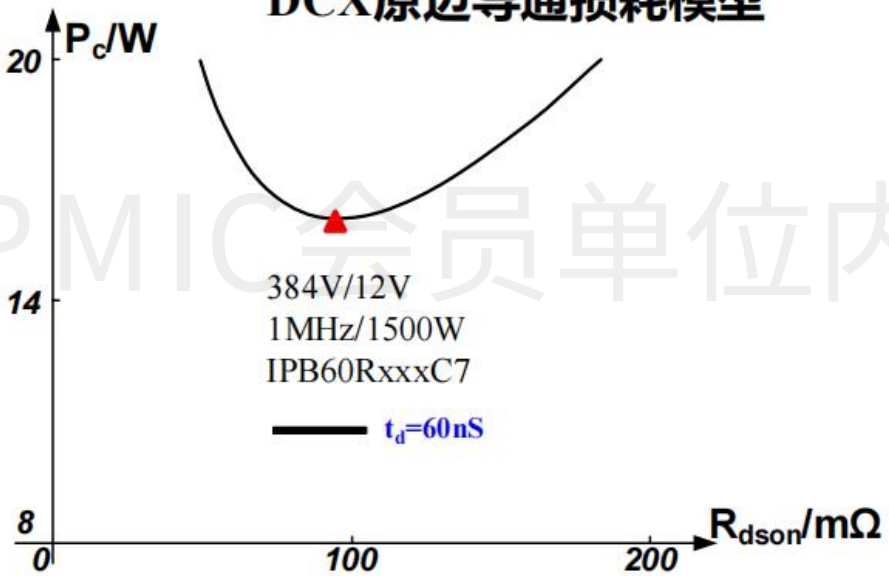
$$P_c(R_{dson}) = A * \frac{1}{R_{dson}} + B * R_{dson}$$

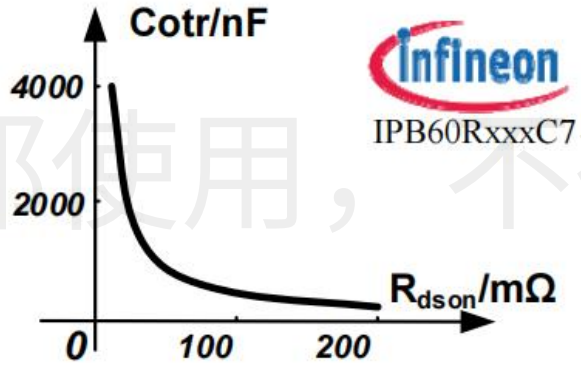
A and B: Constant

$$A = \frac{8n_T^2 V_o^2 T_r * NFoM^2}{t_d^2 T_s}$$

$$B = \frac{\pi^2 I_o^2 T_s}{8n_T^2 T_r}$$

DCX原边导通损耗模型





Infineon

IPB60RxxxC7

$$NFoM = R_{dson} * C_{otr}$$

最小损耗：

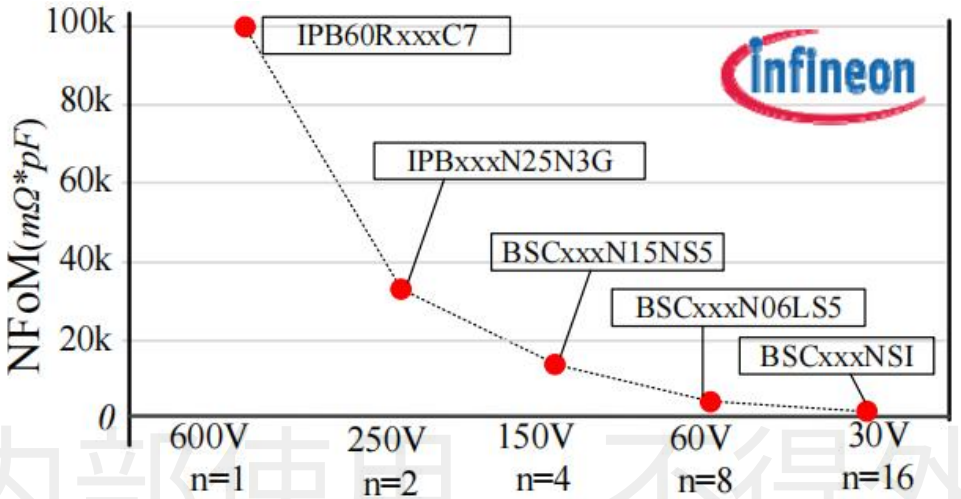
$$P_c(R_{dson}) \geq 2\sqrt{AB} = P_{Cmin} = \frac{2\pi V_o I_o * NFoM}{t_d}$$

给定桥臂死区 t_d

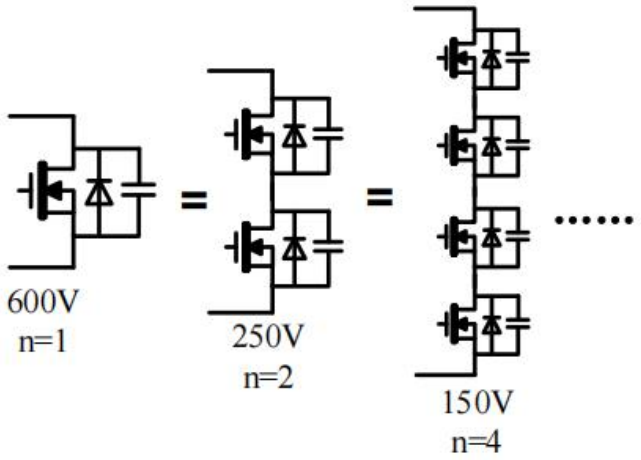
MOSFET的 NFoM 与 耐压 的关系

Low $V_{(BR)DSS}$ =Low NFoM

$$P_{Cmin} = \frac{2\pi * Po * NFoM}{t_d}$$



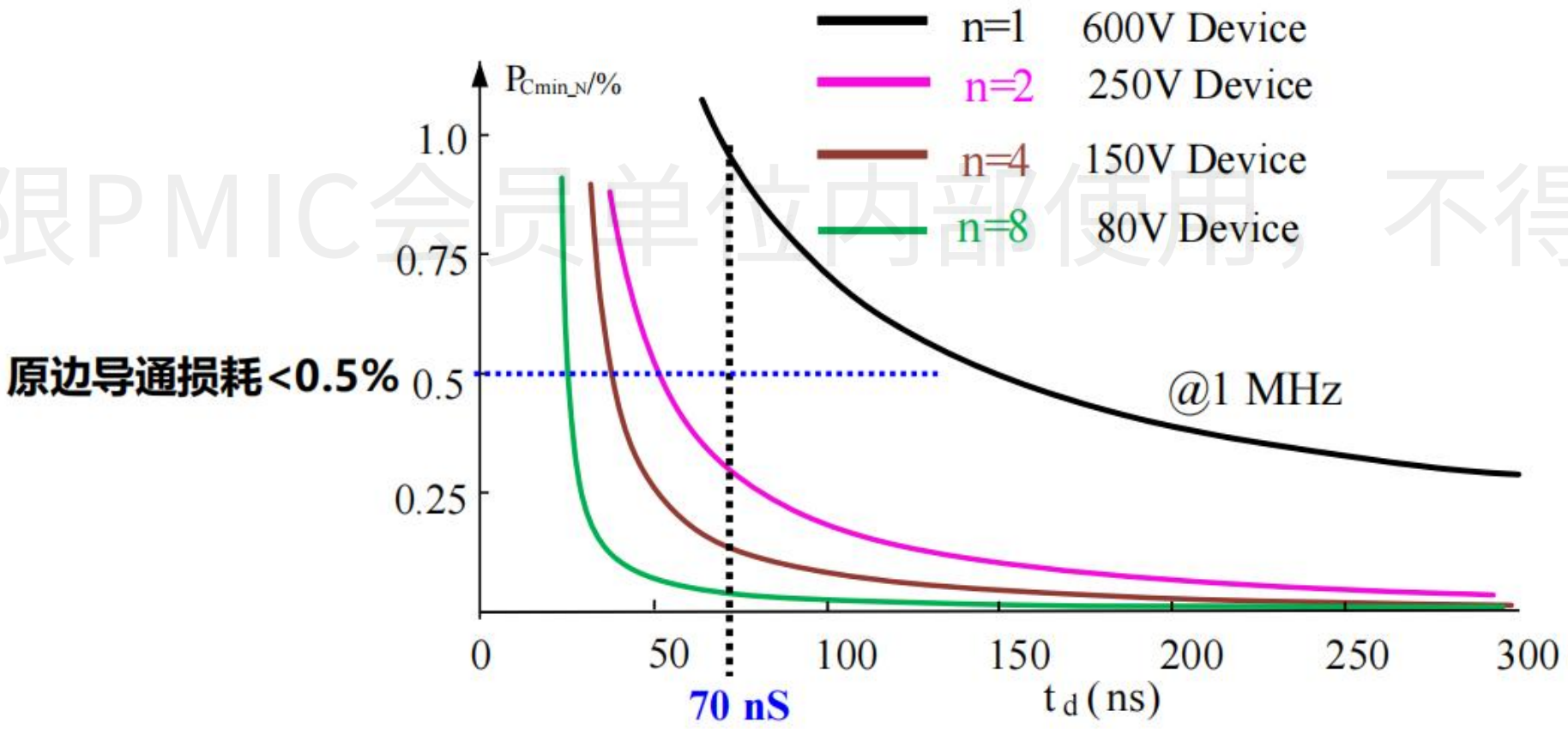
Series-connected low $V_{(BR)DSS}$ devices



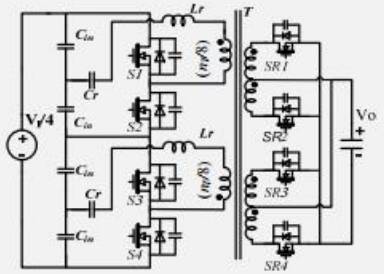
$$NFoM = (\cancel{n}R_{dson}) \cdot \frac{Co_{tr}}{\cancel{n}}$$

不同NFoM 器件对应最小导通损耗

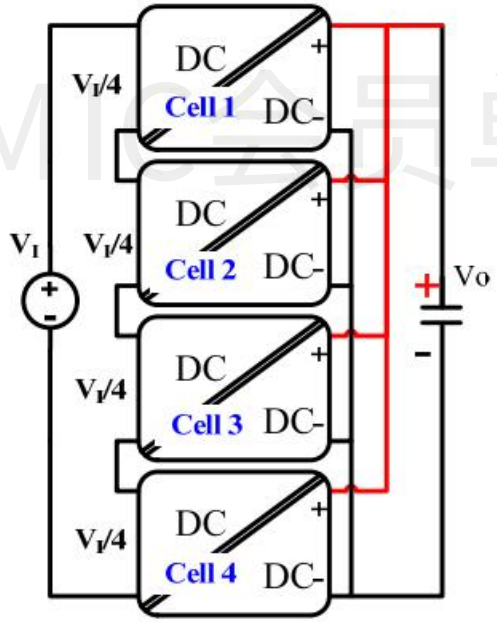
$$P_{Cmin\_N} = \frac{P_{Cmin}}{Po} = \frac{2\pi * \eta * NFoM}{t_d}$$



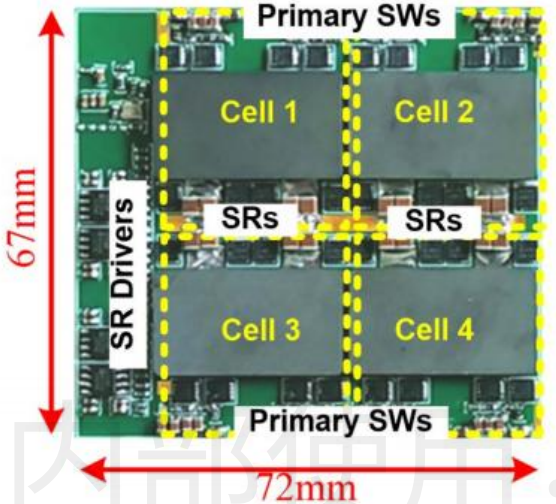
低压元胞电路的高压串联/低压并联



元胞电路

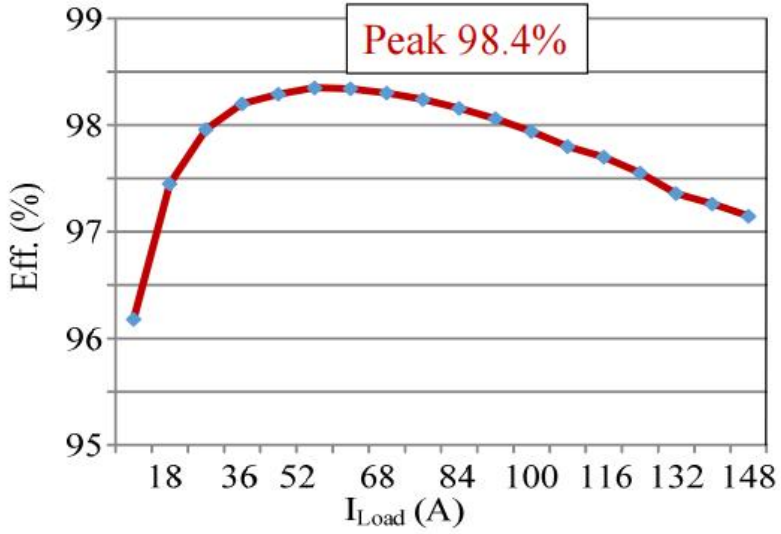


4组元胞电路，原边串，副边并

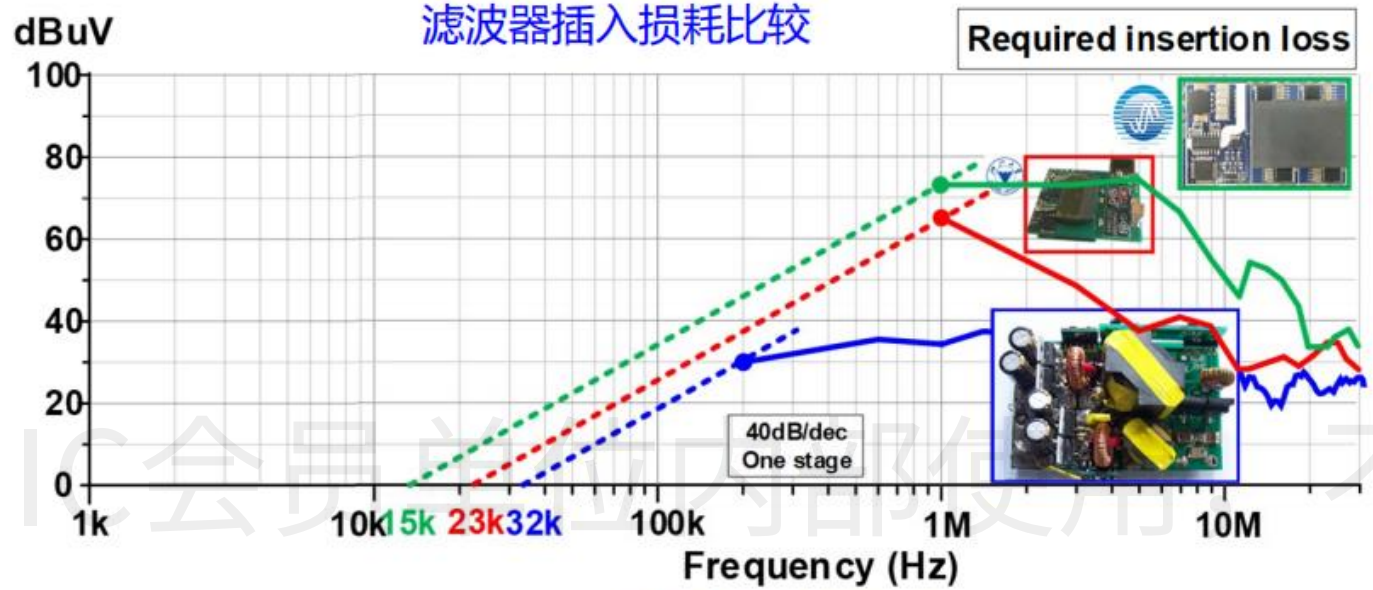


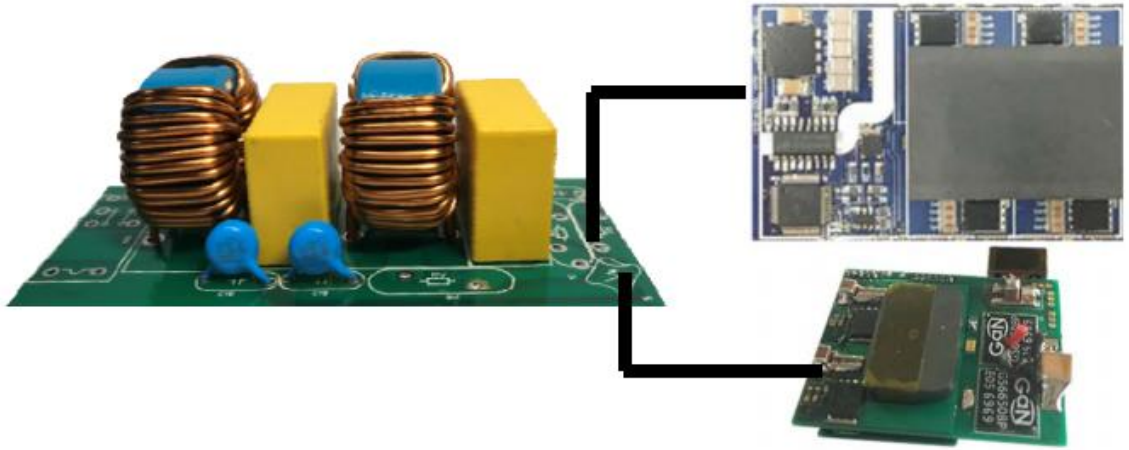
输入: 380V
输出: 12V/150A
功率: 1.8kW

Density:
~900W/in^3
fs:1MHz
6Lays PCB



MHz高频导致更大滤波器体积

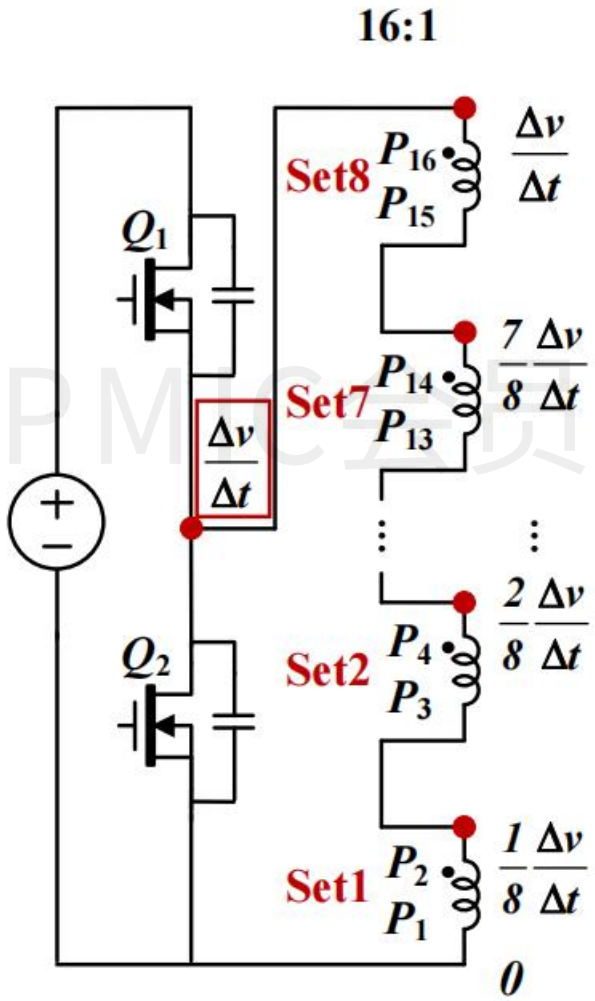




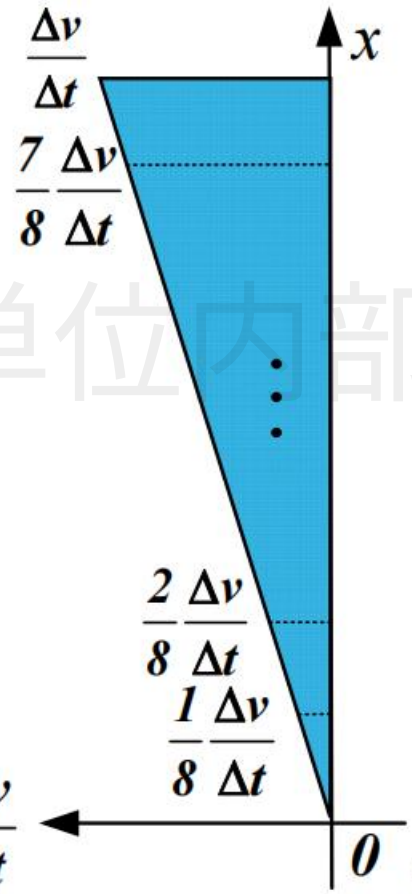
滤波器体积远大于DC/DC变换模块

高压器件构成的传统MHz方案

高压器件构成的传统方案



传统方案的总共模电流

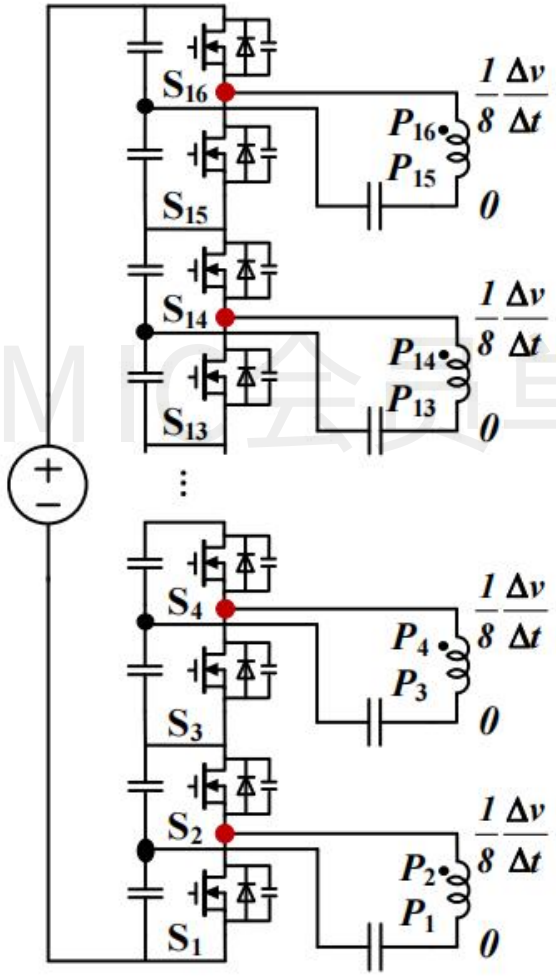


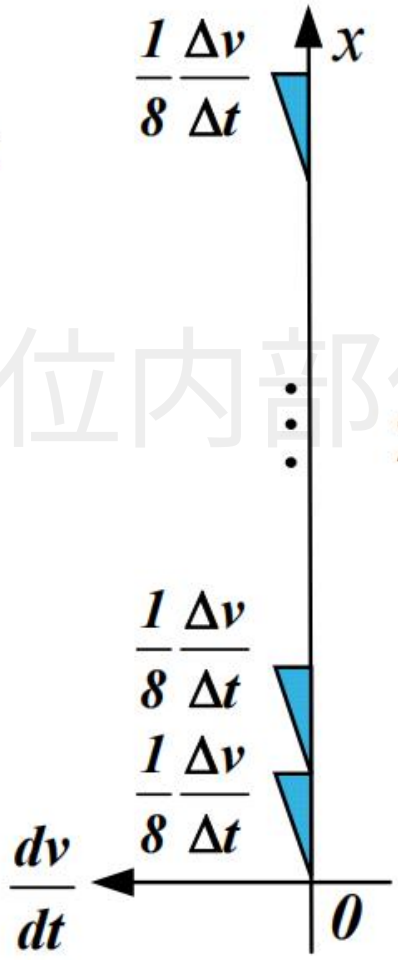
$$i_{CM} = 16C \cdot \frac{\Delta v}{\Delta t}$$

C：一匝原副边绕组的层间物理电容
Δv：LLC谐振变换器的输入电压
Δt：用来实现软开关的死区时间

低压器件构成的多胞电路串并联(ISOP)方案

低压器件构成的ISOP方案(输入串联输出并联)





ISOP方案的总共模电流

$$i_{CM(ISOP)} = 2C \cdot \frac{\Delta v}{\Delta t}$$

$$20\log\left(\frac{i_{CM(ISOP)}}{i_{CM}}\right) = -18dB$$

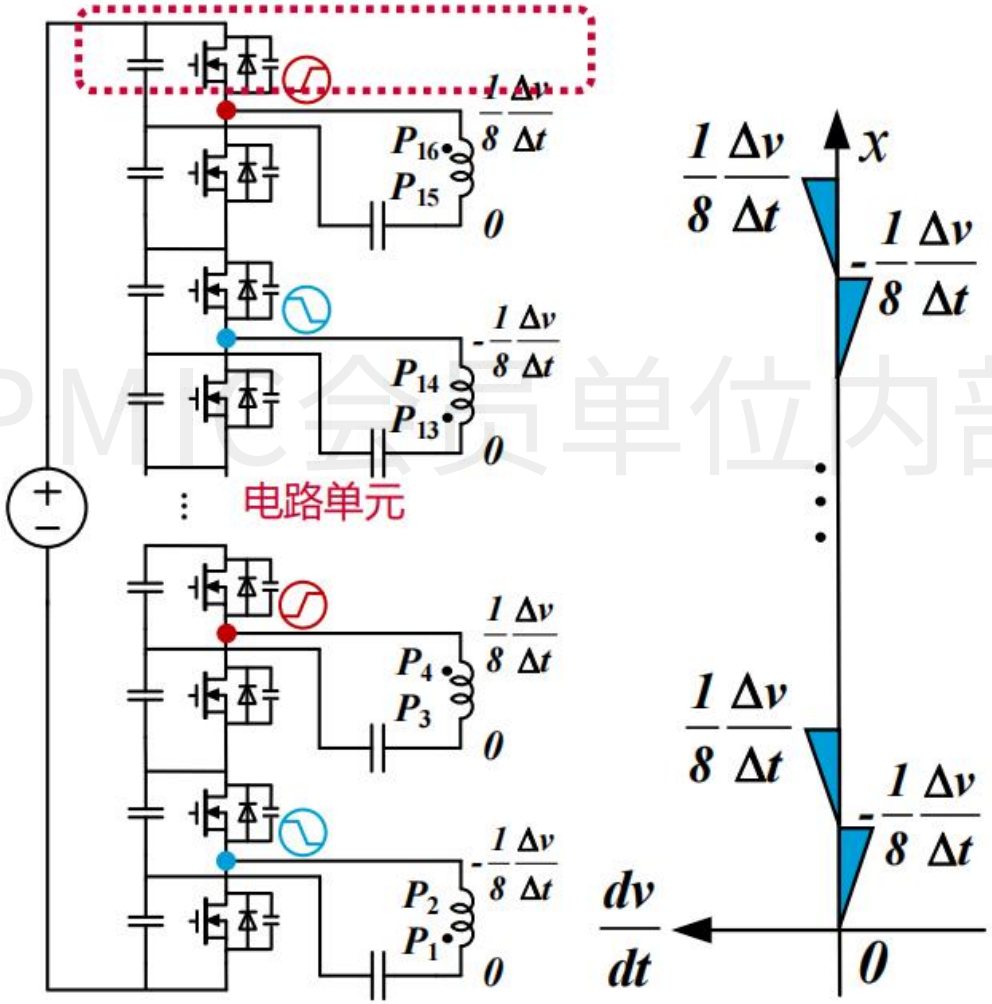
共模电流减小到原来的八分之一

C：一匝原副边绕组的层间物理电容
Δv：LLC谐振变换器的输入电压
Δt：用来实现软开关的死区时间

X. Wu and H. Shi, “High Efficiency High Density 1 MHz 380–12 V DCX With Low FoM Devices,” IEEE Trans. Ind. Electron, Feb. 2020.

元胞电路的交错互补驱动策略

电路单元内交错互补驱动



电路单元内交错之后的总共模电流

$$i_{CM''} = 0$$

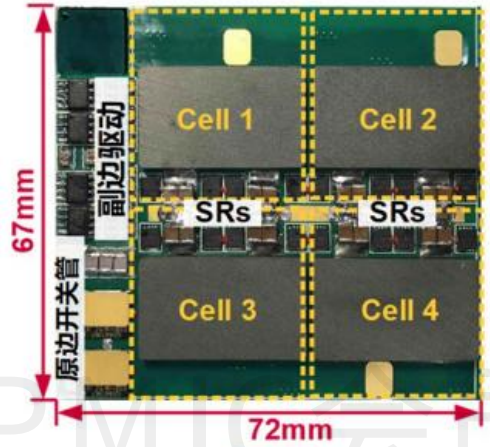
➢ 电路单元内共模噪声抵消

基于多胞电路复合交错控制策略对比

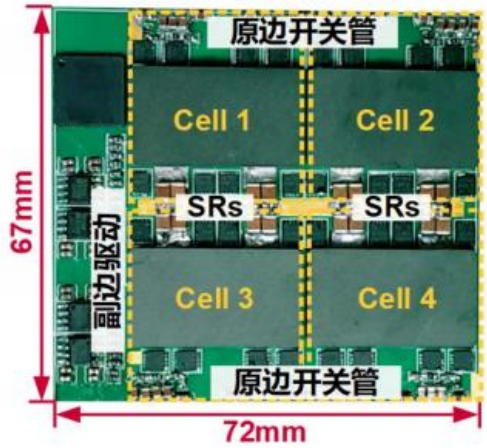
Power Management Innovation Consortium

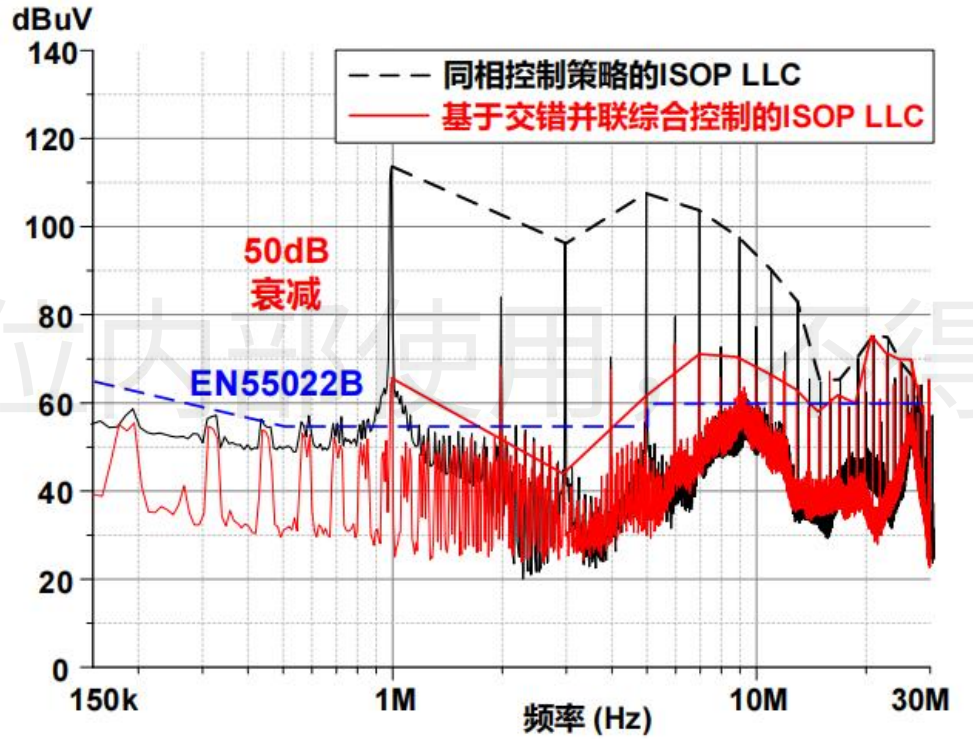
电路单元内交错并联 +电路单元间交错并联

高压器件构成的传统方案



低压器件构成的输入串联方案



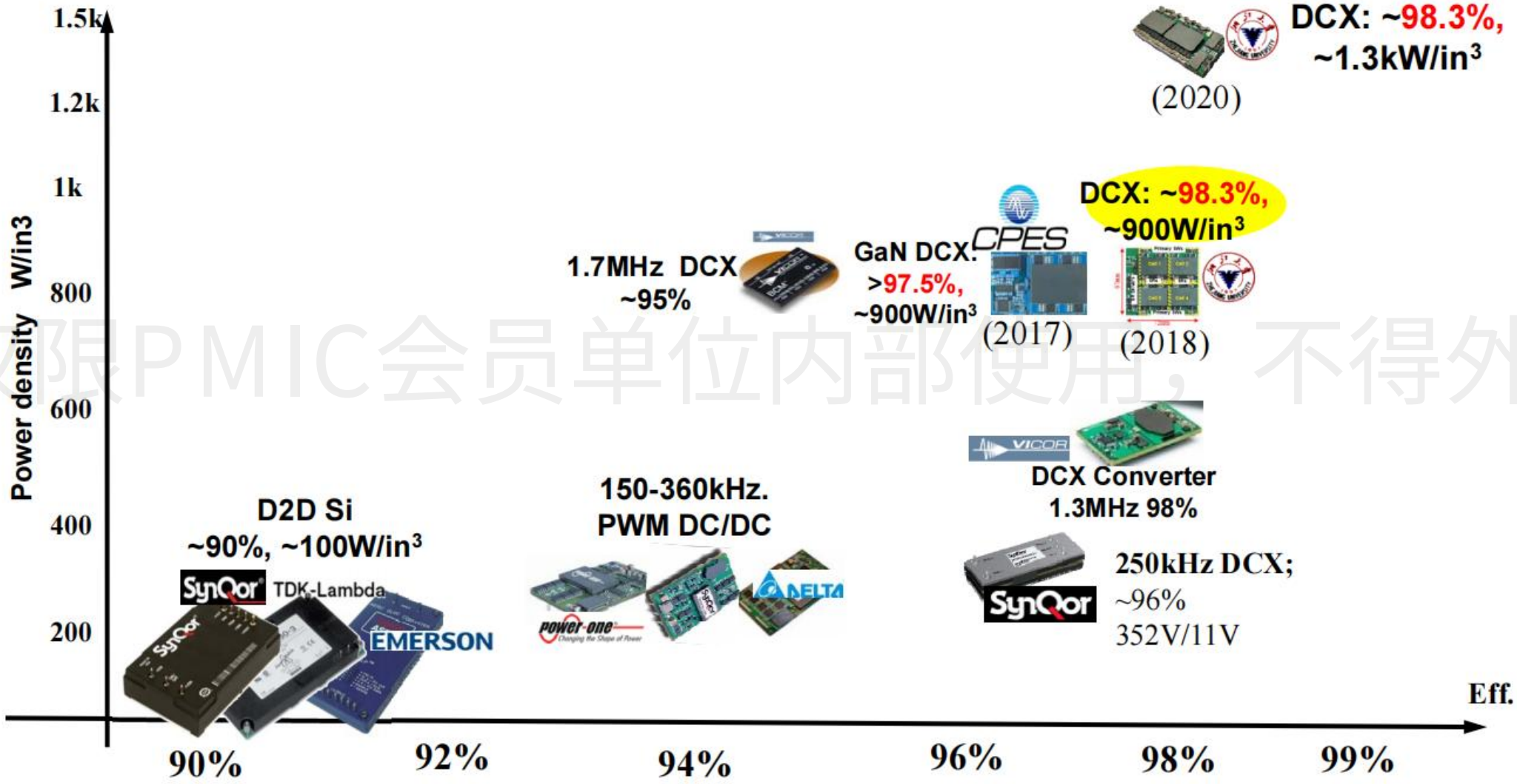


- 测试范围内共模噪声减小50dB
- 基本接近EMI测试标准，滤波器体积大大减小

浙江大学 杭州国际科创中心
ZJU-Hangzhou Global Scientific and Technological Innovation Center

高压DC-DC模块

Power Management Innovation Consortium



总结

- **多电平技术可以大幅降低PFC磁元件体积**

  减小电感的秒参数，还可以减小伏参数，更有效的减小电感体积，提高效率。

- **揭示了低NFoM器件可以提高MHz变换器效率的电路本质**

  在PFC和DC/DC中，低压器件具有比高压(GaN)器件更低的NFoM，可以降低损耗，获得更高的效率

- **低压元胞电路串联降低高压导通损耗，提高功率密度**

  1）元胞低压电路串联的拓扑可以降低导通损耗，提高效率

  2）多元胞低压串联可以降低共模EMI噪声，提高系统功率密度。

  3）通过优化元胞电路间控制逻辑，可以进一步降低/消除共模EMI滤波器