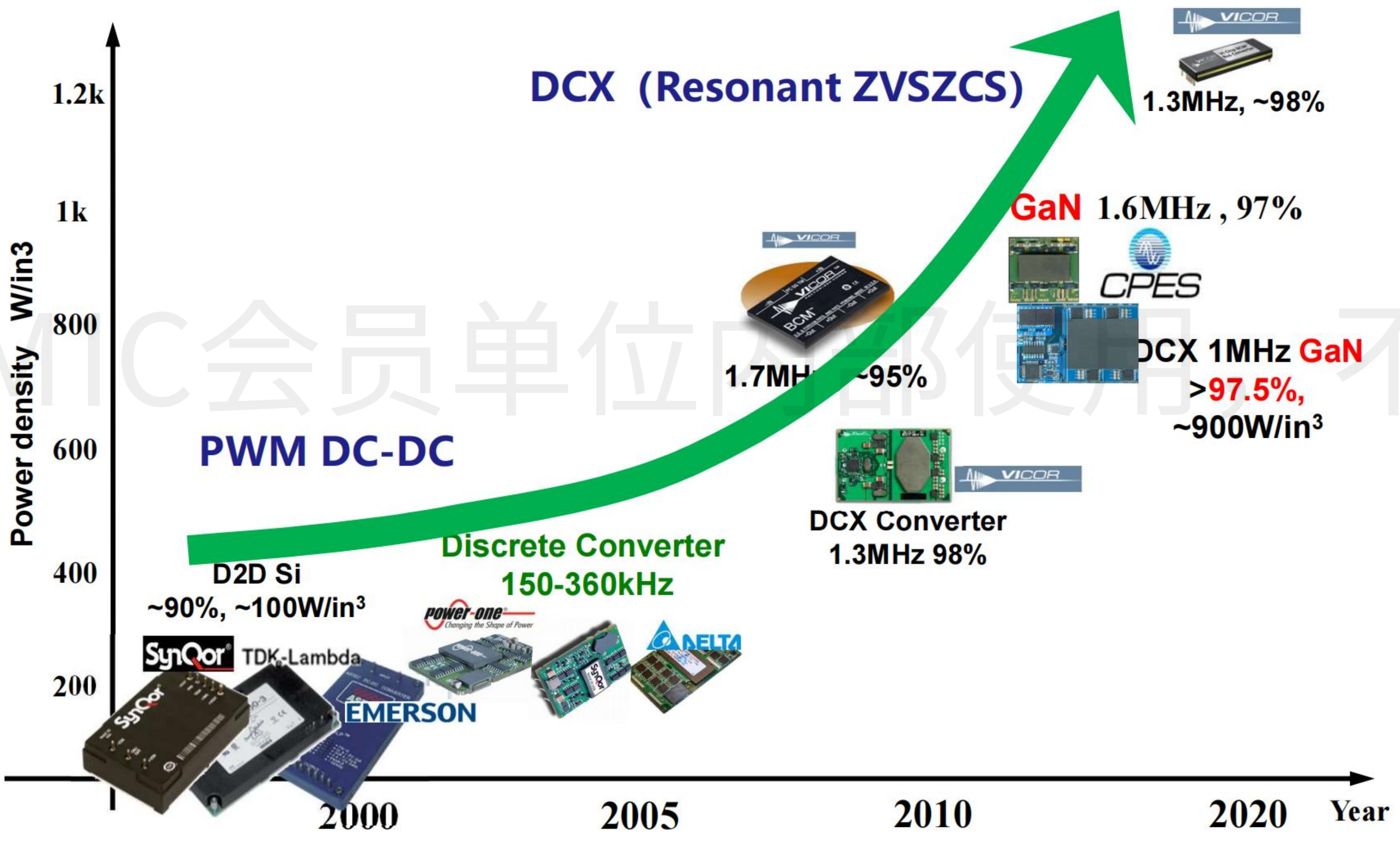
High Efficiency High Power Density Cellular 380V-12V DCX Using Low NFoM Devices

Xinke Wu Ph. D

Trends for Isolated DC/DC Converters



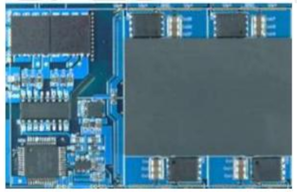
Popular Topology for MHz DCX

VICOR

1.3MHz, ~98%

CPES

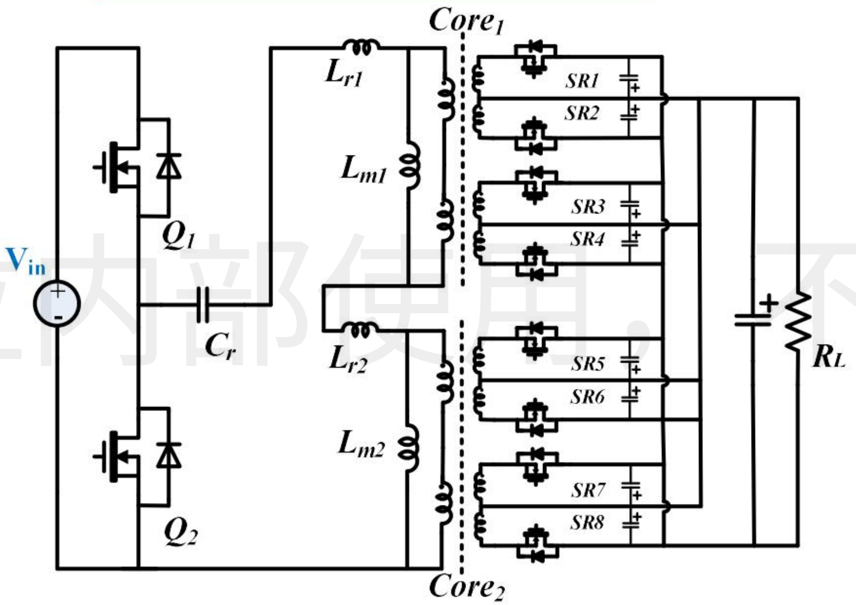
GaN



DCX 1MHz GaN
4 Layer PCB
97.5%,900W/in^3
(2016)

48V-12V
1MHz , >98%
(2019)

- LC Resonant
- Matrix Transformer



☺ ZVS on
☺ ZCS off
☺ Without reverse recovery

Does fully soft witching achieve high efficiency easily at MHz?

Density Comparison among DCXs

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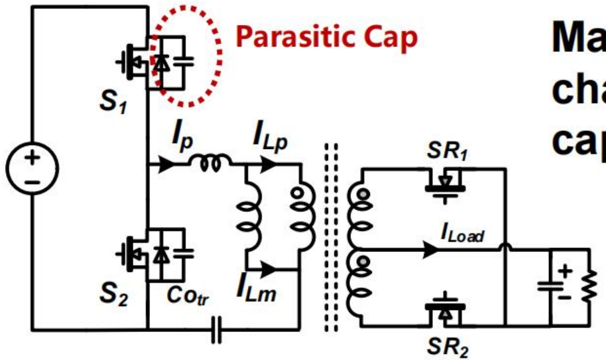
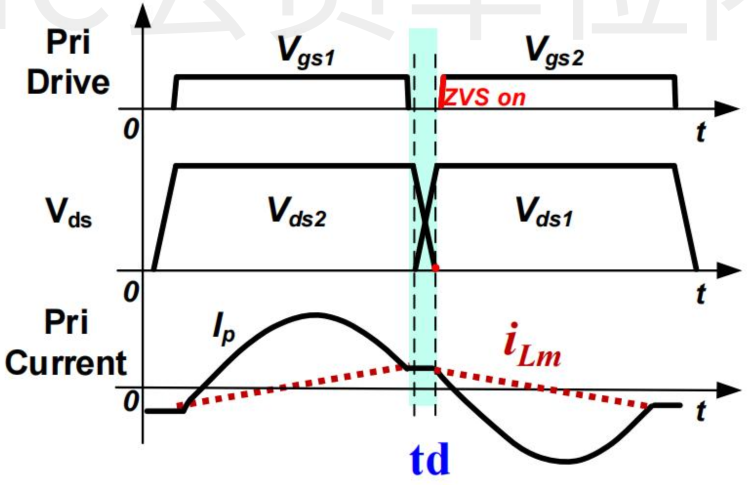
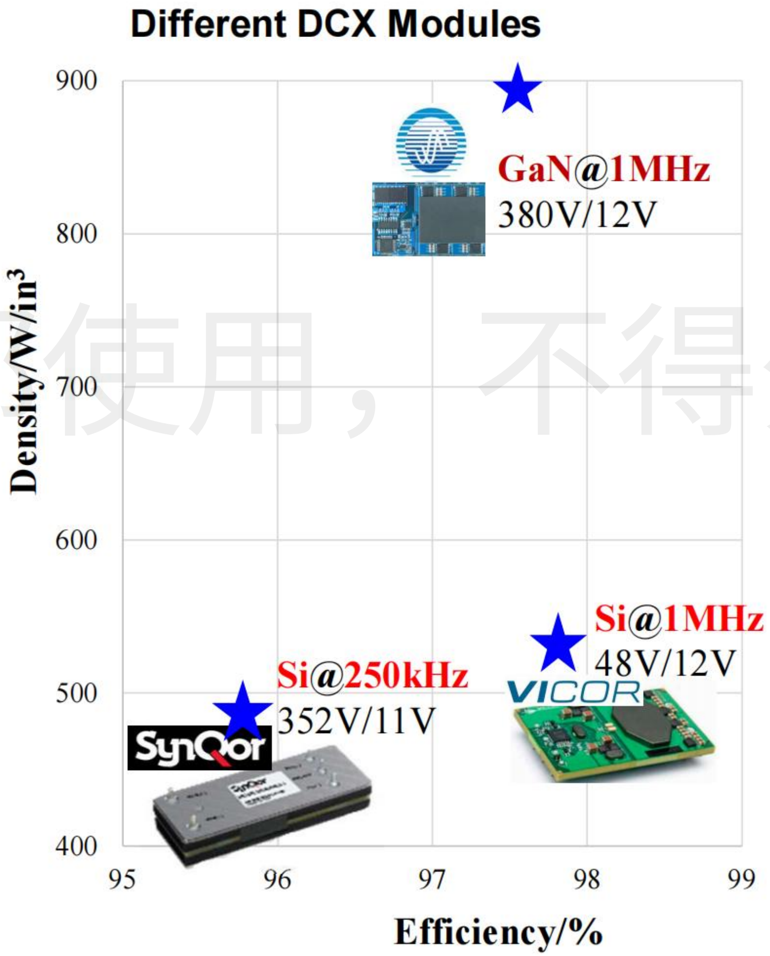


Magnetizing current charging parasitic capacitance

fs≈fr





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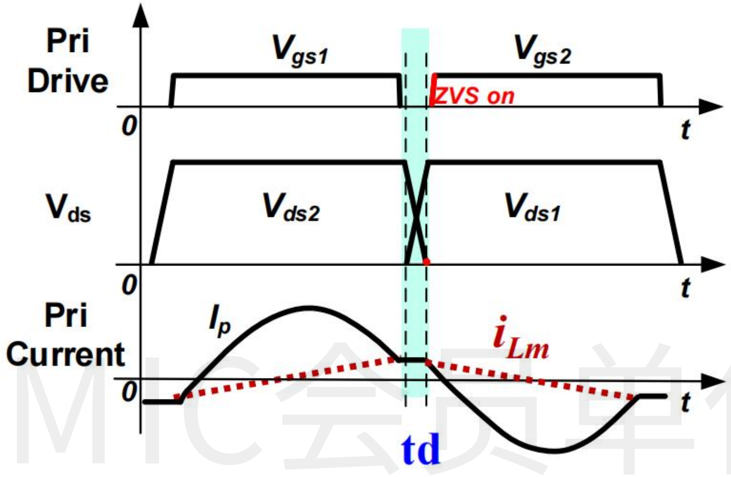
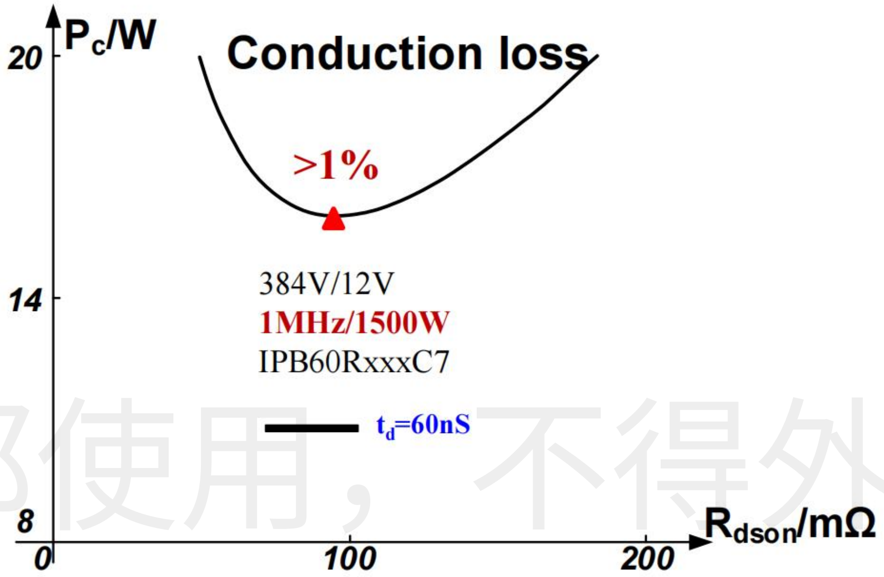
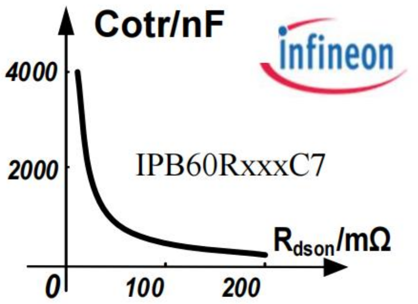
Primary Conduction Loss Model of DCXs





$$P_c(R_{dson}) = A * \frac{1}{R_{dson}} + B * R_{dson}$$

A and B: **Const.** $A = \frac{8n_T^2 V_o^2 T_r * NFoM^2}{t_d^2 T_s}$ $B = \frac{\pi^2 I_o^2 T_s}{8n_T^2 T_r}$



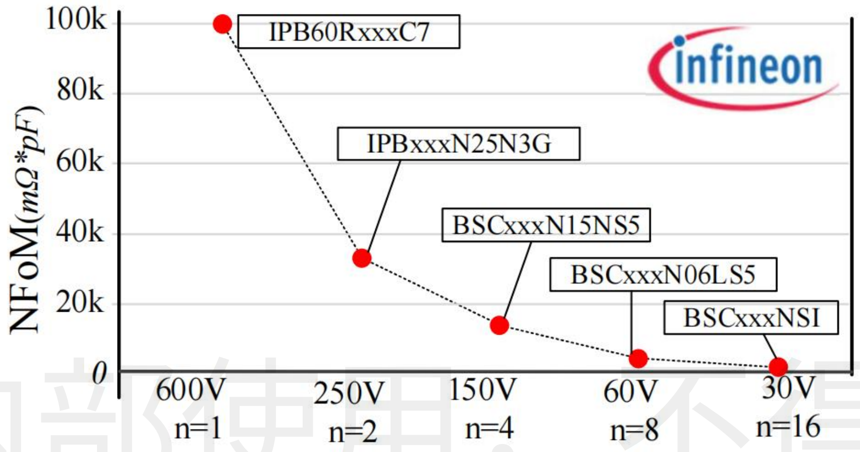
Min. Loss： $P_c(R_{dson}) \geq 2\sqrt{AB} = P_{Cmin} = \frac{2\pi V_o I_o * NFoM}{t_d}$

$$NFoM = R_{dson} * C_{otr}$$

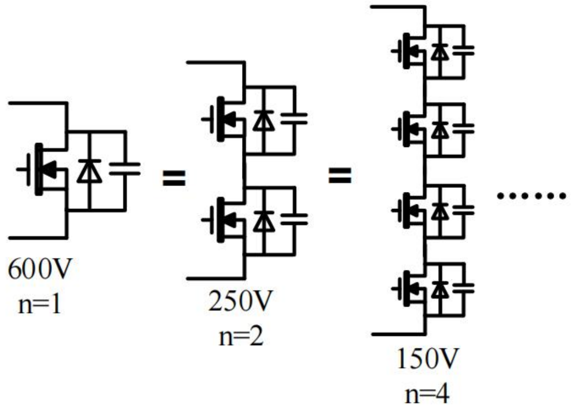
Series-connected low NFoM devices

Low $V_{(BR)DSS}$ =Low NFoM

$$P_{Cmin} = \frac{2\pi * Po * NFoM}{t_d}$$



Series-connected low $V_{(BR)DSS}$ devices



$$NFoM = (\cancel{n}R_{dson}) \cdot \frac{Co_{tr}}{\cancel{n}}$$

Conduction loss depends to single low voltage device

Xinke Wu. Hongbo Shi. “High Efficiency High Density 1 MHz 380–12 V DCX With Low FoM Devices” IEEE TIE 2020. pp1648-1656

Interwinding Capacitance Sinking Magnetizing Current in PCB Transformer

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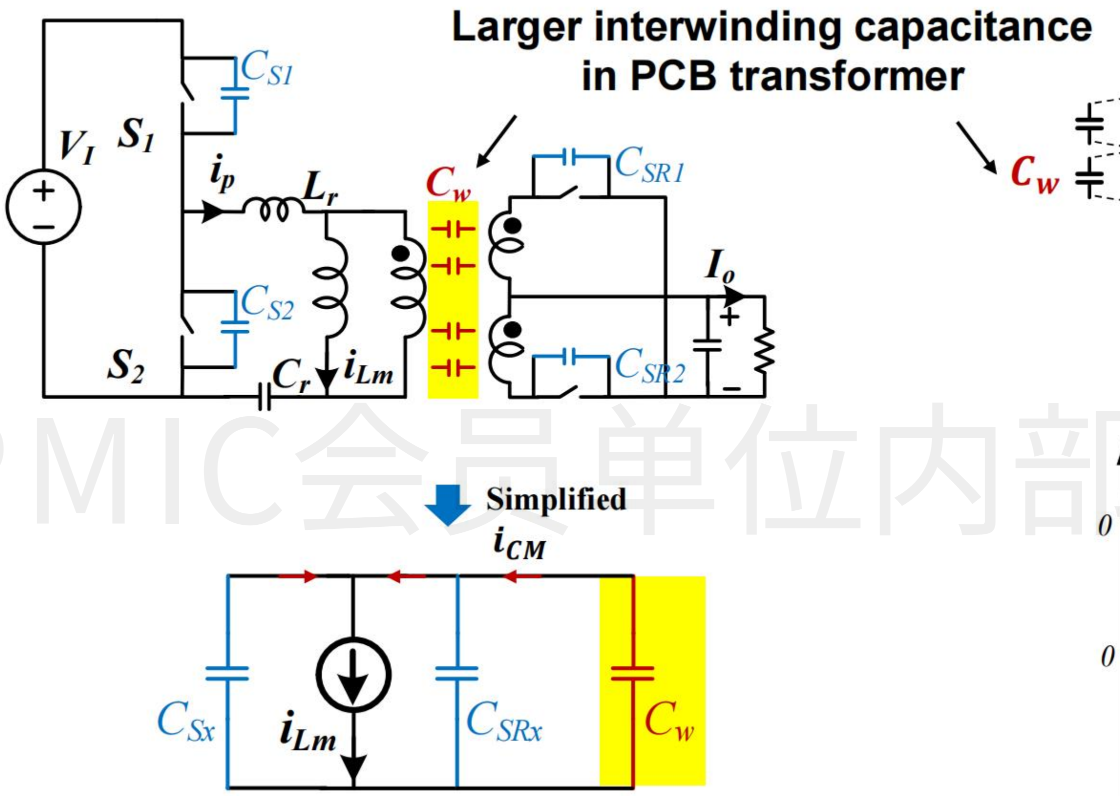
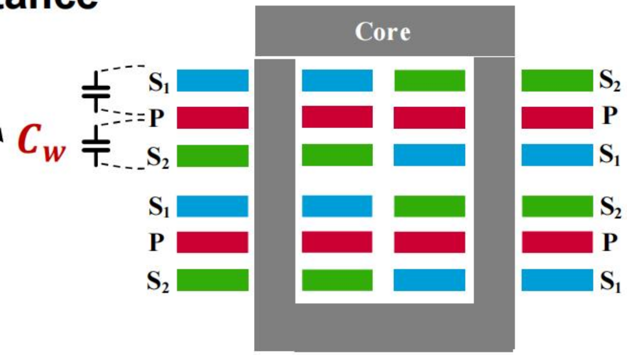
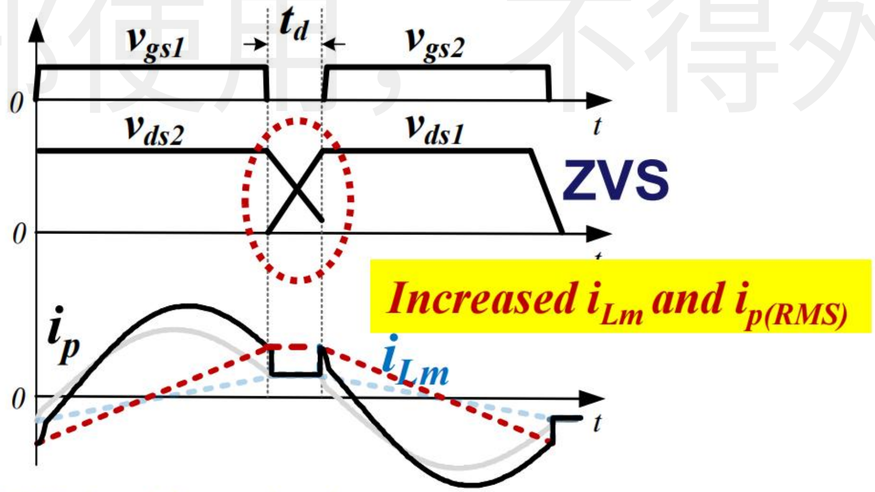




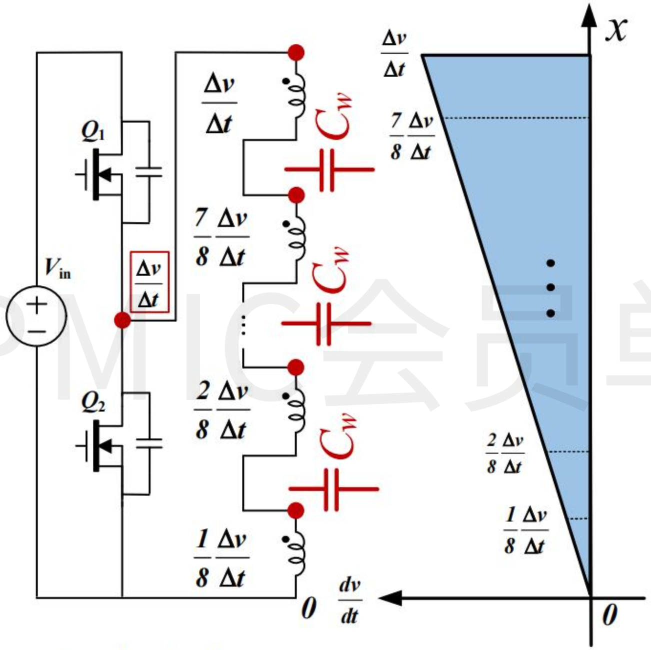


Larger magnetizing current for ZVS is Needed

D. Fu, S. Wang, P. Kong, etc., "Novel Techniques to Suppress the Common-Mode EMI Noise Caused by Transformer Parasitic Capacitances in DC–DC Converters," in IEEE TPEL, Nov. 2013,

Larger Magnetizing Current Leads to Higher Eddy Current Loss in Windings

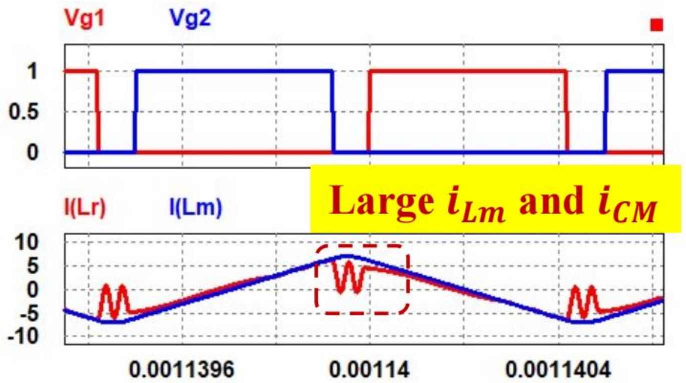
- **Conventional SRC**



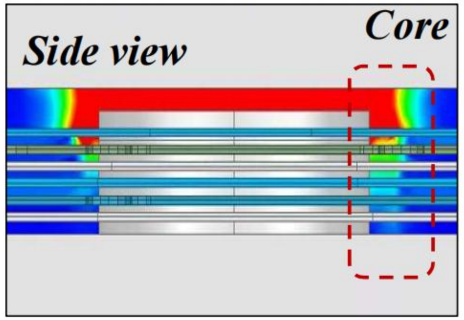
Δv : Input voltage
Δt : Dead time

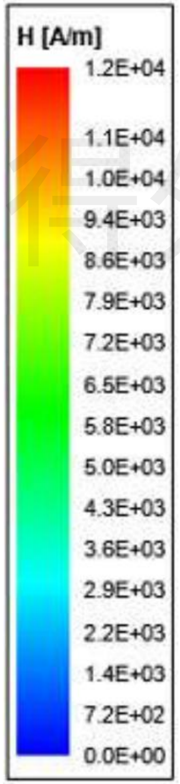
$$i_{CW} = 16C \cdot \frac{\Delta v}{\Delta t}$$

higher magnetizing current



H field distribution 380V/12V DCX



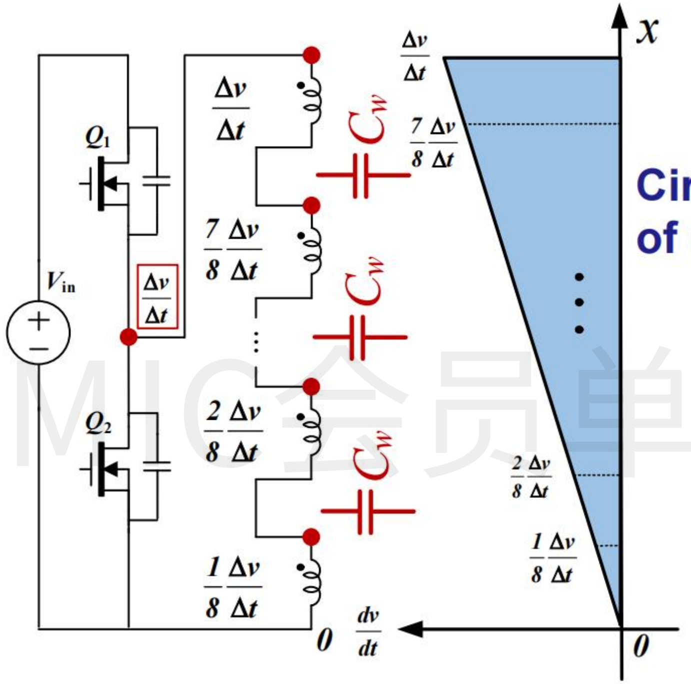


Total Winding loss ≈ 5.4W

@ Io=0.5A light load

Interwinding Cap Sinking Current is Reduced Significantly by Cellular Topology

■ Conventional SRC

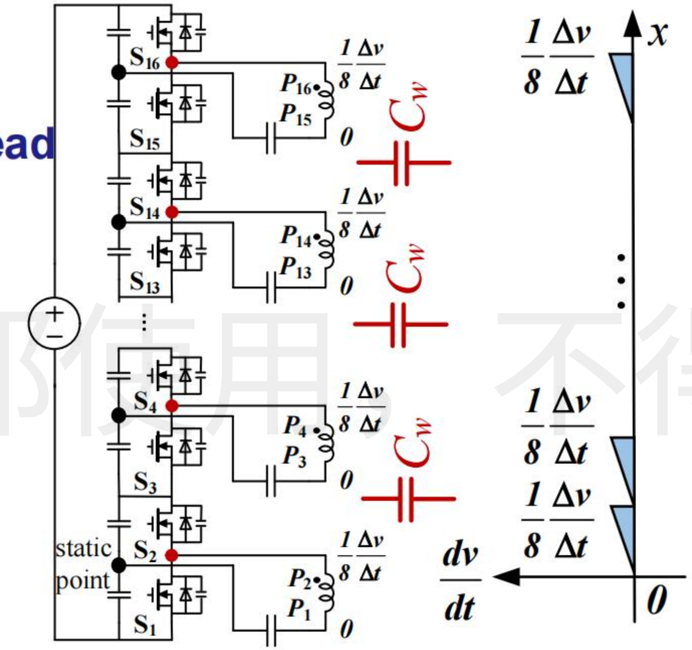


Δv : Input voltage
Δt : Dead time

$$i_{CW} = 16C \cdot \frac{\Delta v}{\Delta t}$$

Circuit in series instead of device in series

■ Cellular ISOP SRC

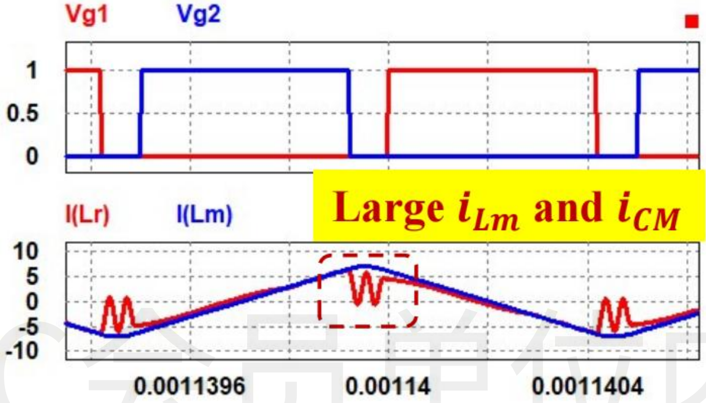


$$i_{CW} = C \cdot \frac{\Delta v}{\Delta t}$$

Smaller magnetizing current sinking by smaller ΔV

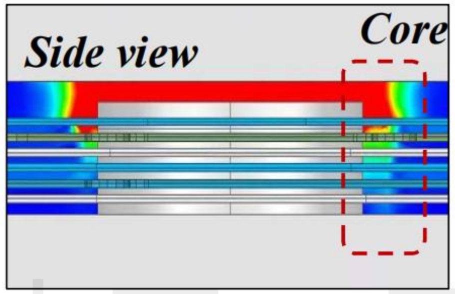
Smaller magnetizing current and smaller eddy current loss in cellular DCX

Conventional HV SRC

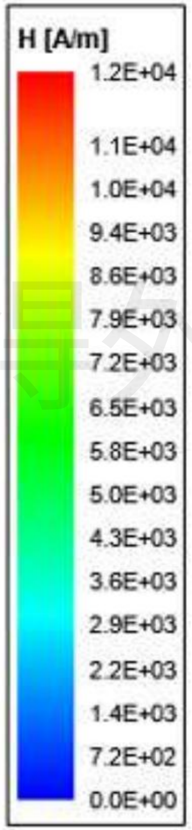


higher magnetizing current

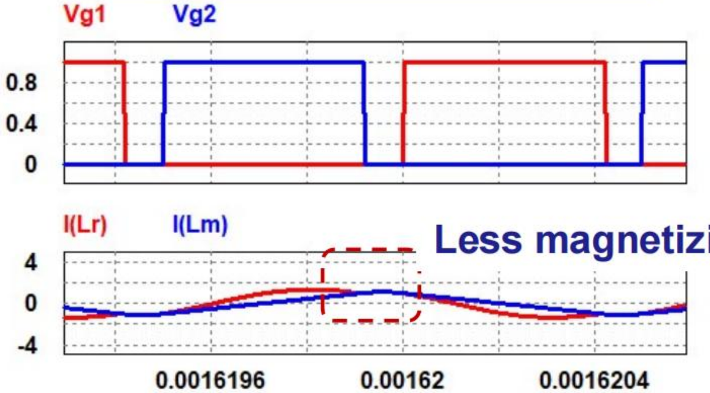
H field distribution 380V/12V DCX @ Io=0.5A



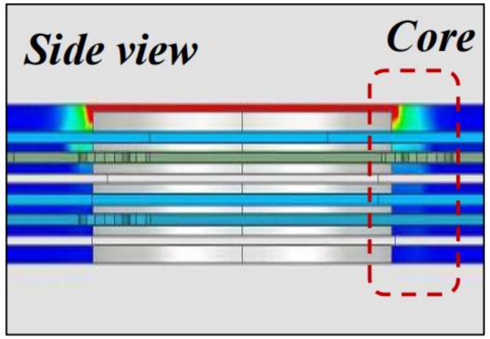
Total Winding loss ≈ 5.4W



Cellular ISOP SRC



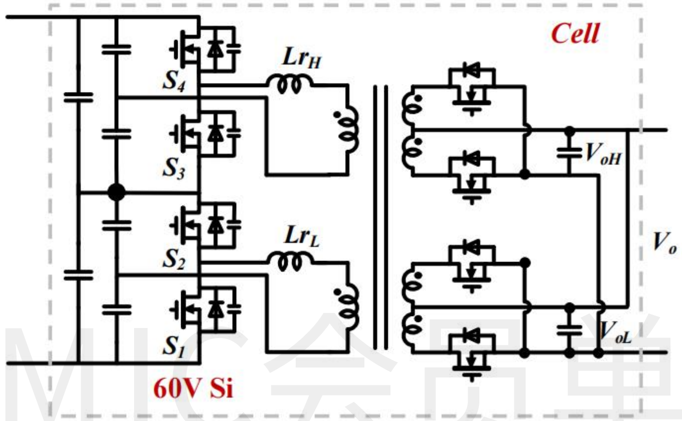
Less magnetizing current



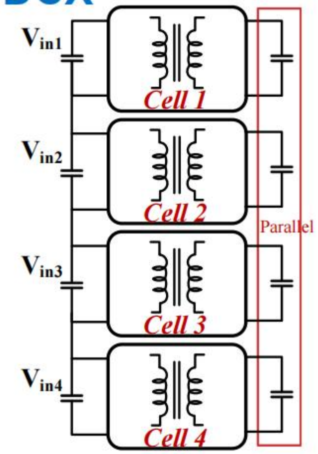
Total Winding loss ≈ 0.3W

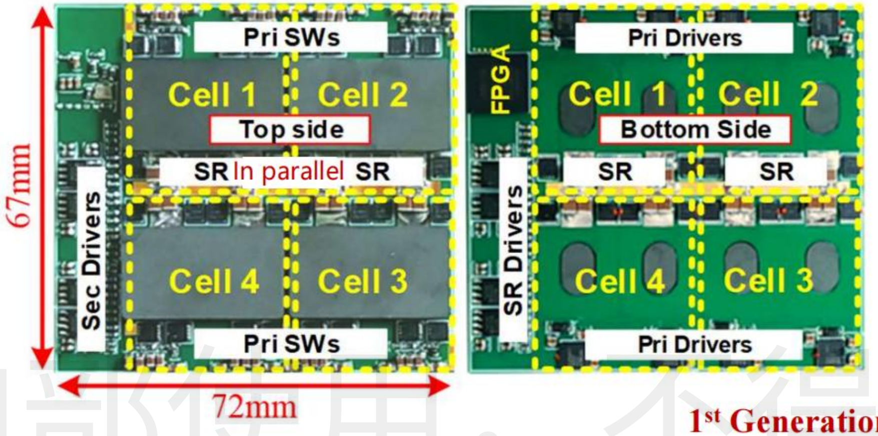
1st Generation 380V/12V Cellular DCX Using Low Voltage Devices

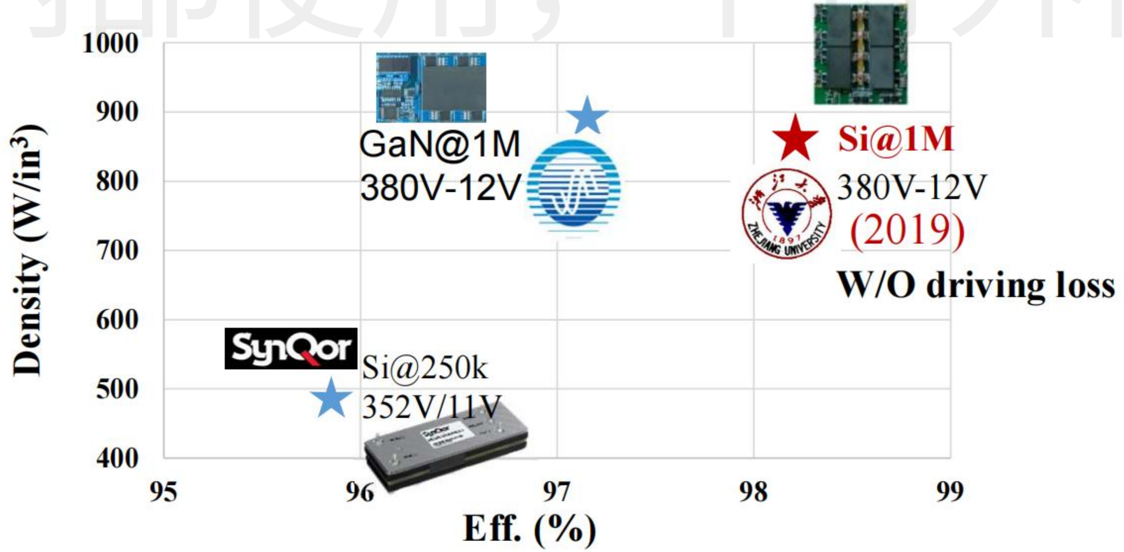
■ Circuit cell: SRC DCX



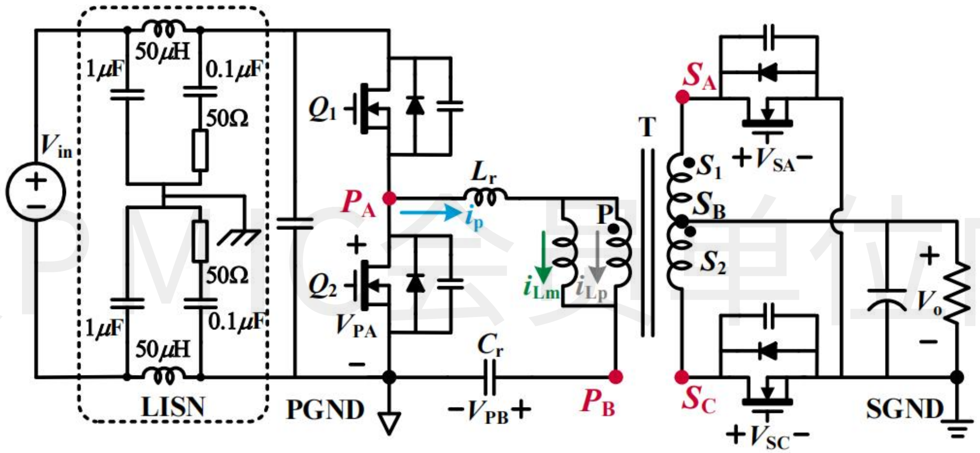
■ ISOP SRC DCX



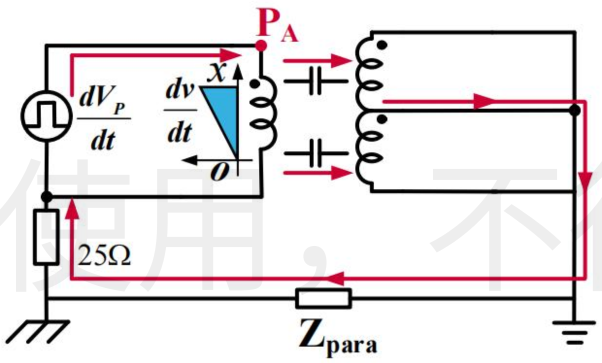




CM Noise Conducting Path of the Half-bridge SRC DCX



Half-bridge SRC DCX topology with LISN

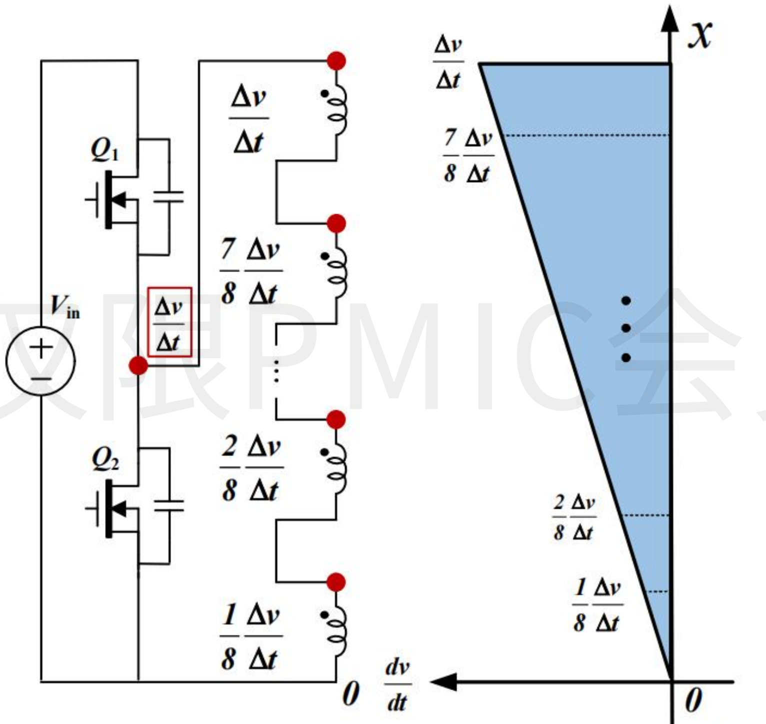


primary common mode noise source and path

[2] Yue Han, Guangcan Li, Hongbo Shi and Xinke Wu, "Analysis and Suppression of Common-Mode EMI Noise in 1 MHz 380 V-12 V DCX Converter With Low NFoM Devices," in IEEE TPEL, vol. 36, no. 7, pp. 7903-7913, July 2021.

Cellular SRC with Static Points for Smaller CM Current and Noise

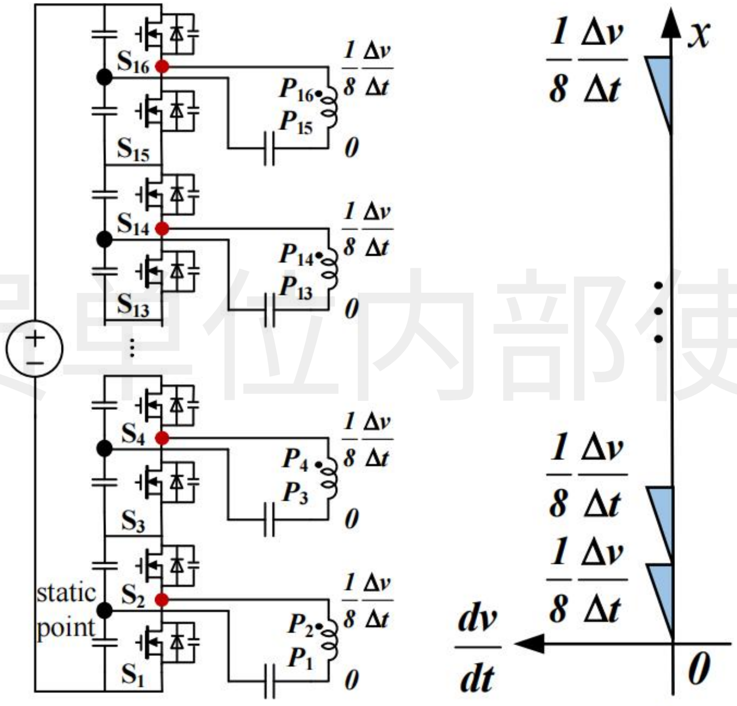
■ **Conventional HV SRC**



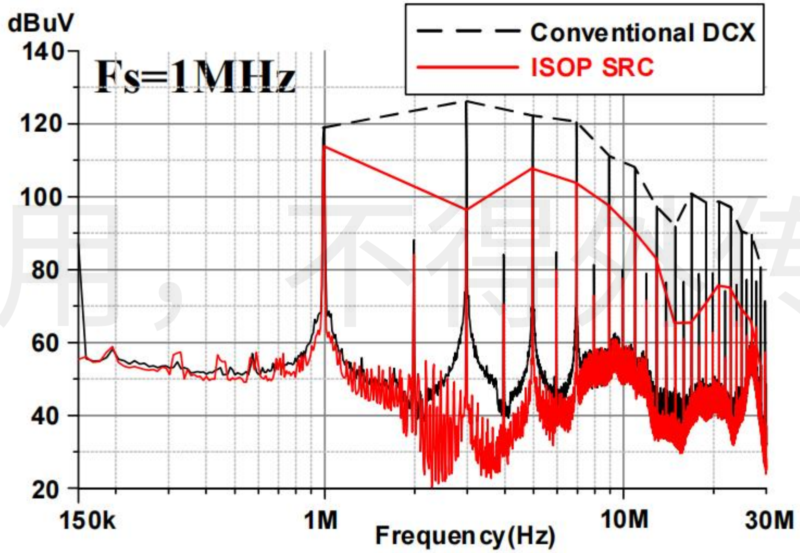
Δv : Input voltage
Δt : Dead time

$$i_{CM} = 16C \cdot \frac{\Delta v}{\Delta t}$$

■ **ISOP Cellular SRC**

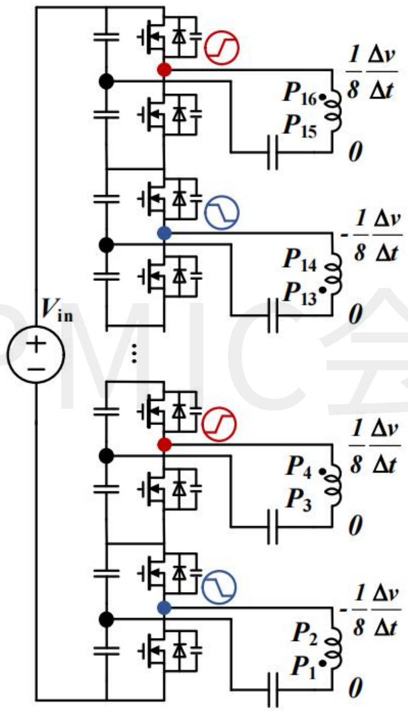


$$i_{CM} = C \cdot \frac{\Delta v}{\Delta t}$$



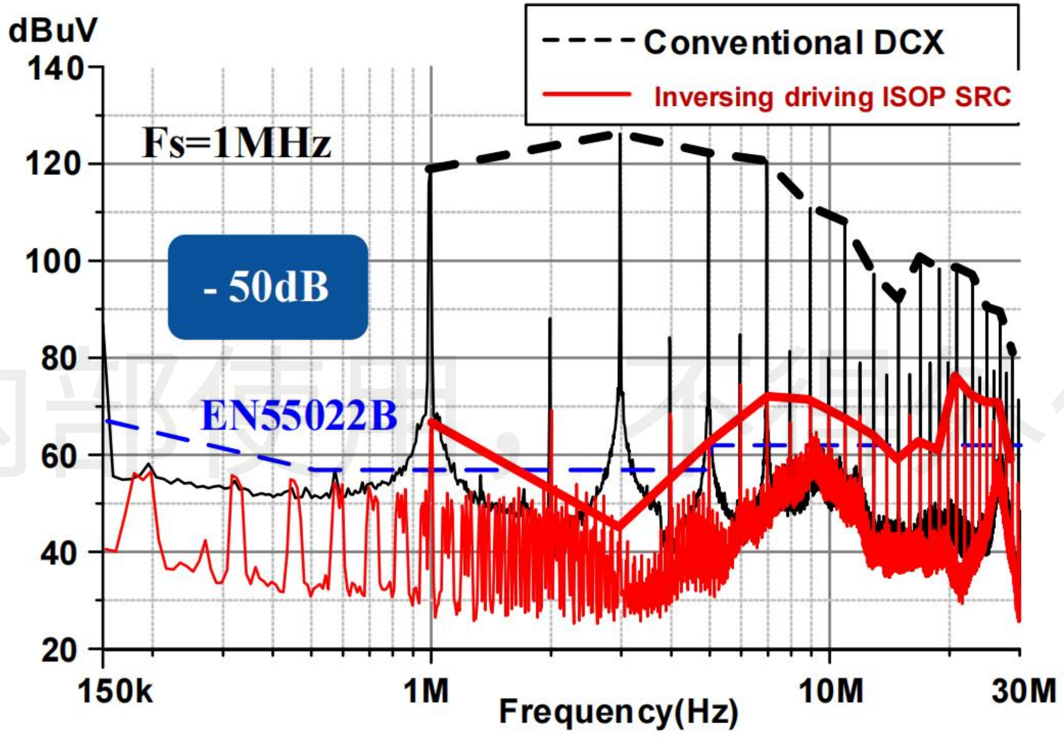
Common-mode Noise Cancellation with Inversing Driving Logic in the Cellular DCX

■ **Inverse driving in ISOP SRC**



Δv : Input voltage
Δt : Dead time

$i_{CM} \approx 0$

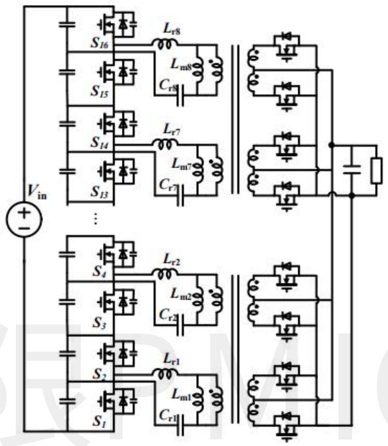


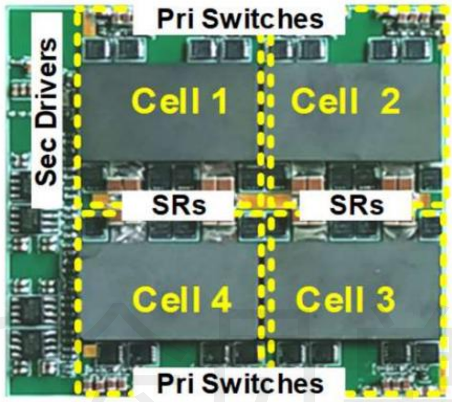
No need for shielding layers

[2] Yue Han, Guangcan Li, Hongbo Shi and Xinke Wu, "Analysis and Suppression of Common-Mode EMI Noise in 1 MHz 380 V-12 V DCX Converter With Low NFoM Devices," in IEEE TPEL, vol. 36, no. 7, pp. 7903-7913, July 2021.

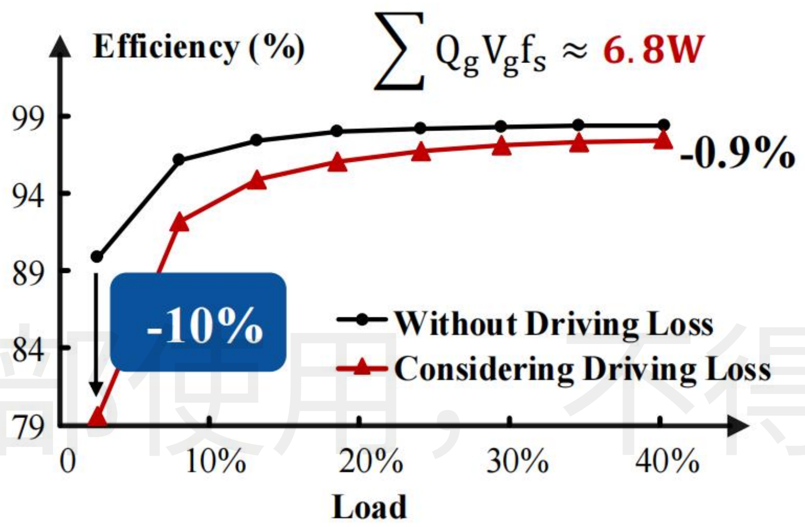
Large Driving Loss when Using Drive ICs

☐ 1MHz 380V-12V-150A DCX





	Primary MOSFET	Synchronous Rectifier
Type	 BSZ040N06LS5	 BSZ0501NSI
Quantity	**16**	**32**
Q_g (nC@7V)	25.7	17.5

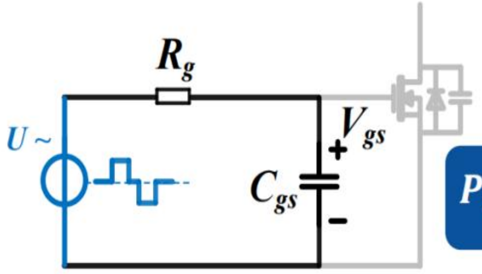


Light load
3% of full load

Light load efficiency reduced significantly

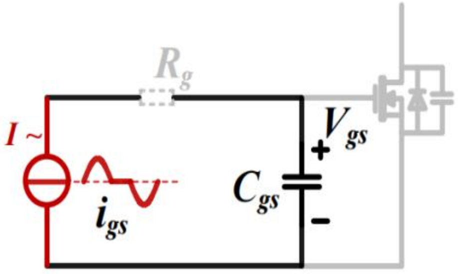
Lower Driving Speed Results in Less Driving Loss in Resonant Driver

- Voltage source driver (VSD)



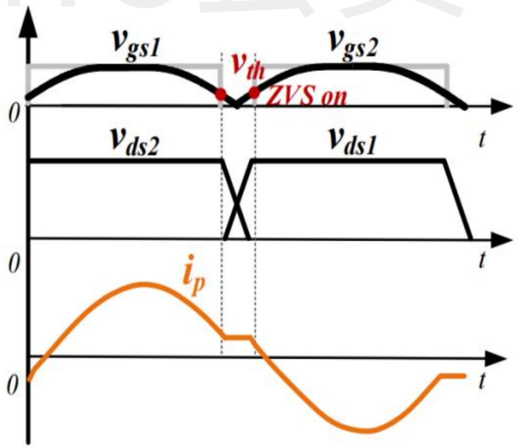
$$P_{dri} = C_{gs} V_{gs}^2 f_s$$

- Resonant driver



Ideal

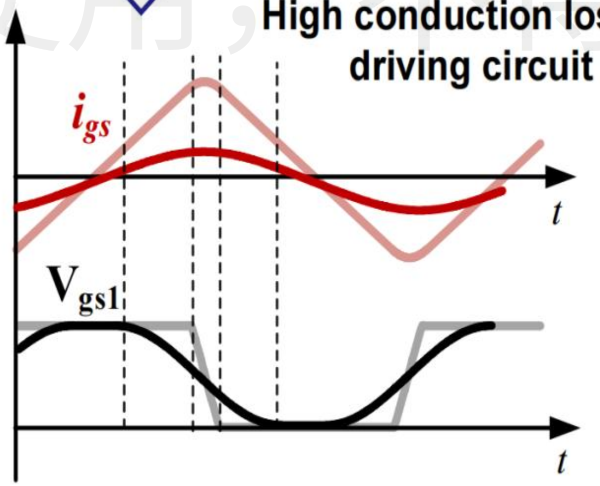
$$P'_{dri} = i_{gs}^2 R_g \rightarrow 0$$



Primary ds voltage and current in SRC converter

Lower driving speed is acceptable owing to sinusoidal switch current

High conduction loss in driving circuit



Less driving current is needed

Driving Loss Reduced Significantly By the Resonant Drive Transformer

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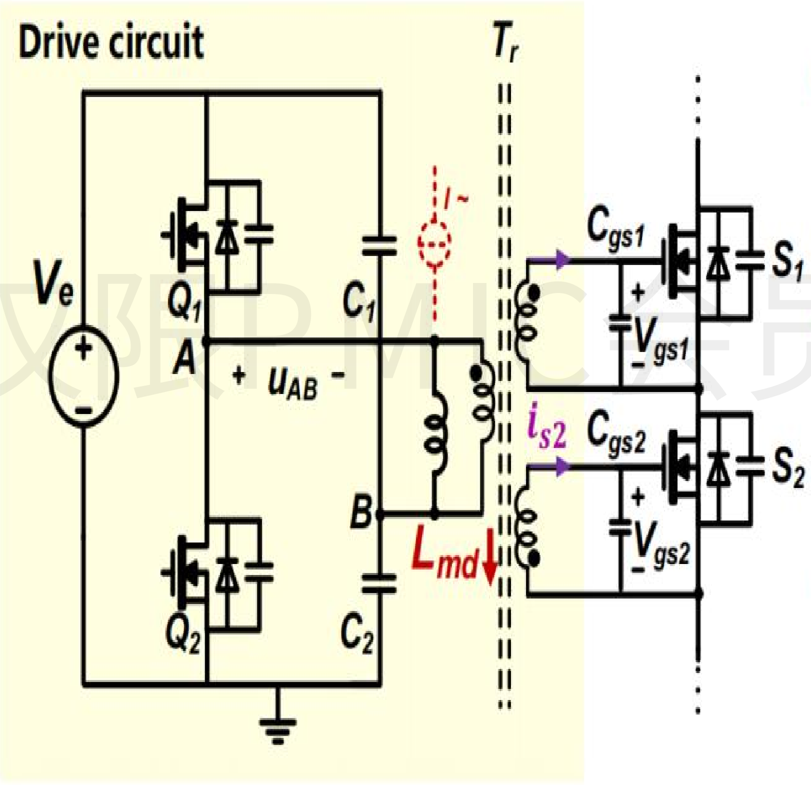
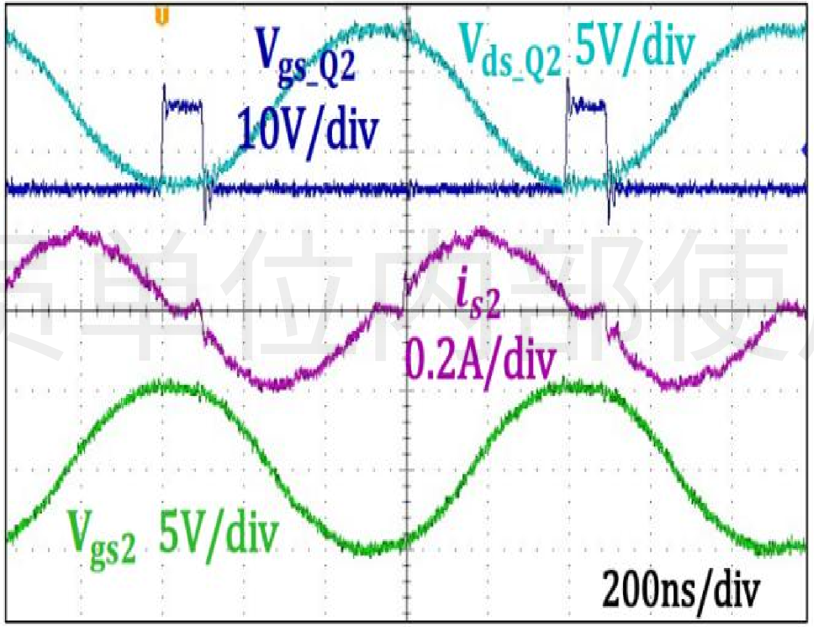
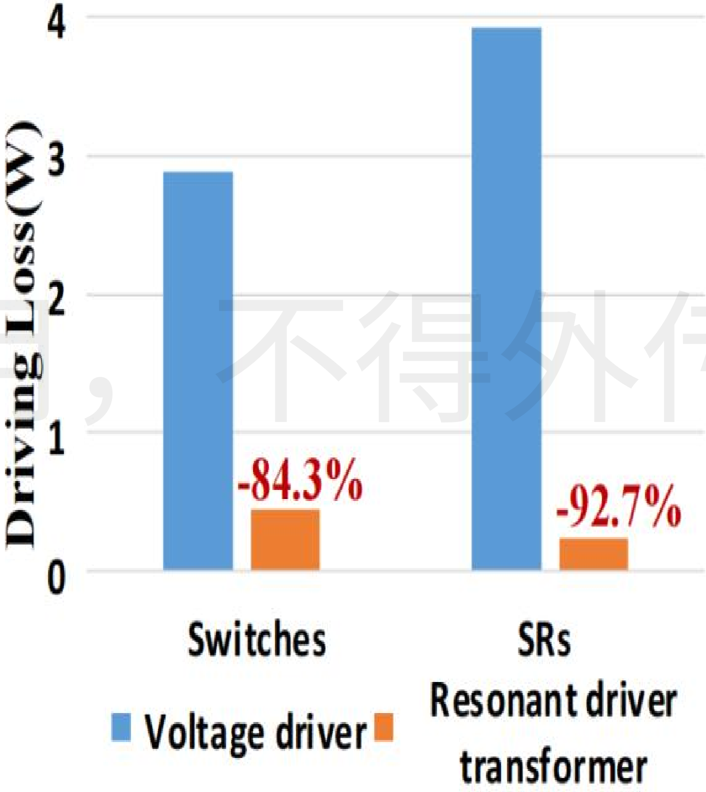


Resonant Drive Transformer

ZVS for driving circuit

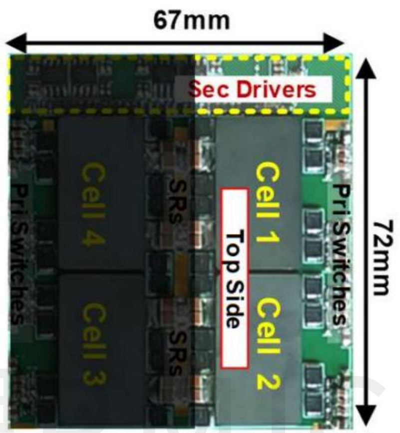




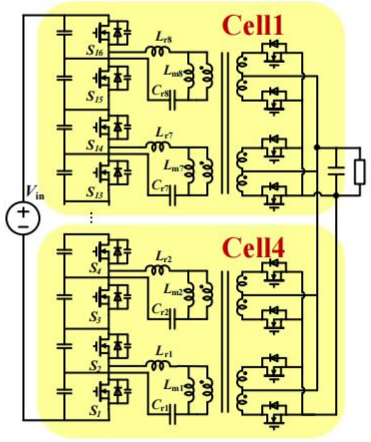
- ✓ Save driving losses
- ✓ Shrink the footprint of drive circuit

Integrating More PCB Layers for Power Density Optimization

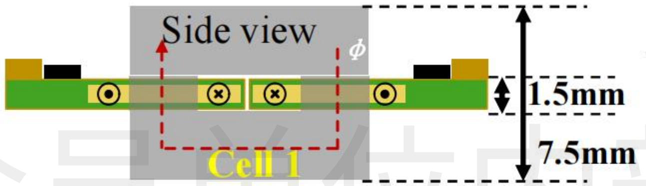
- 1st Generation



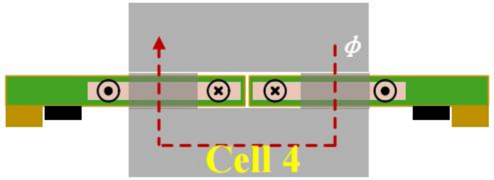
Six lays PCB



- Transformer =4



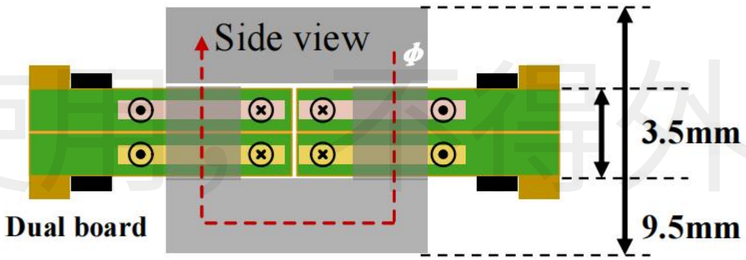
≈ 500W



≈ 500W

- Transformer =2

12 lays PCB



≈ 1kW

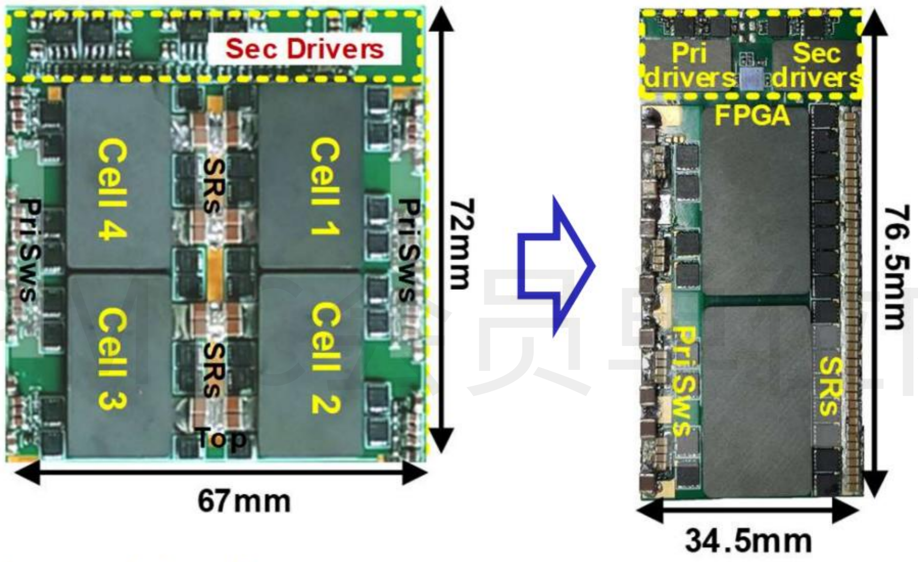
Footprint Reduced

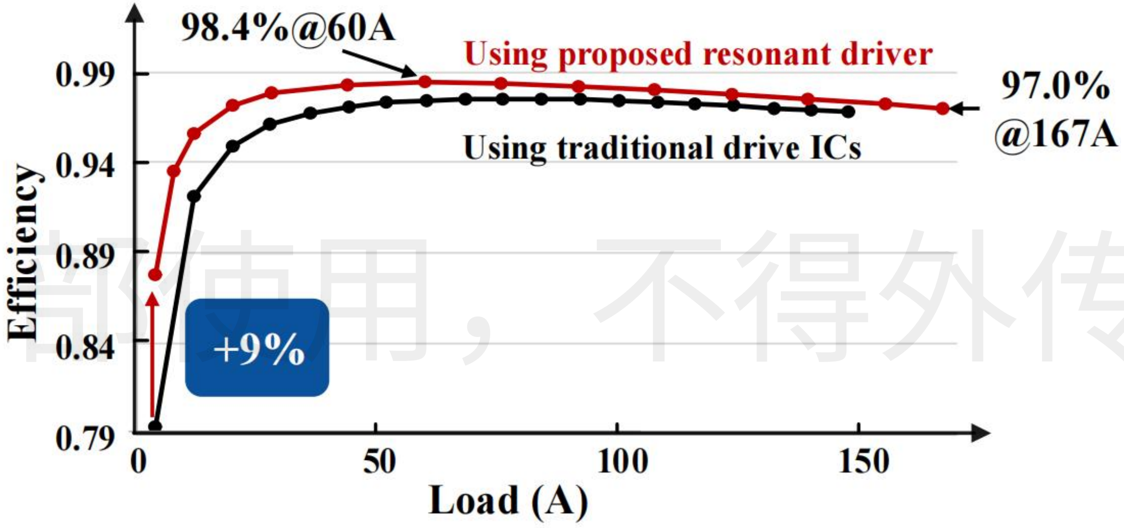
Cellular topology makes higher integrated transformer easier

2nd Generation 380V/12V DCX Using Resonant Drive Transformer and Integrated Power Transformer

■ Comparison of the prototypes

1st Generation　　　　2nd Generation





Considering the driving losses

■ Power Density:

~0.9kW/in³　　　　~1.3kW/in³

[3] Guangcan Li and Xinke Wu, "A 98.4% Efficiency 380V-12V DCX With 1.3kW/in3 Power Density Using Low NFoM Devices and Resonant Drive Transformer," in IEEE TPEL, vol. 37, no. 10, pp. 12346-12356, Oct. 2022.

Less Power Density Improvement when Further Reducing the Thickness of Plate Core

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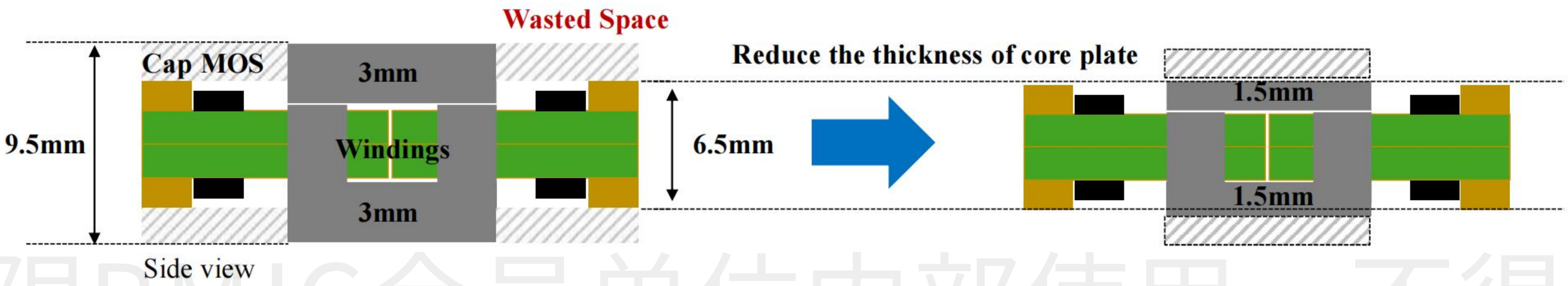
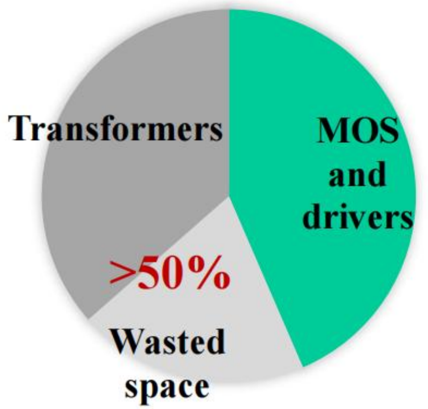
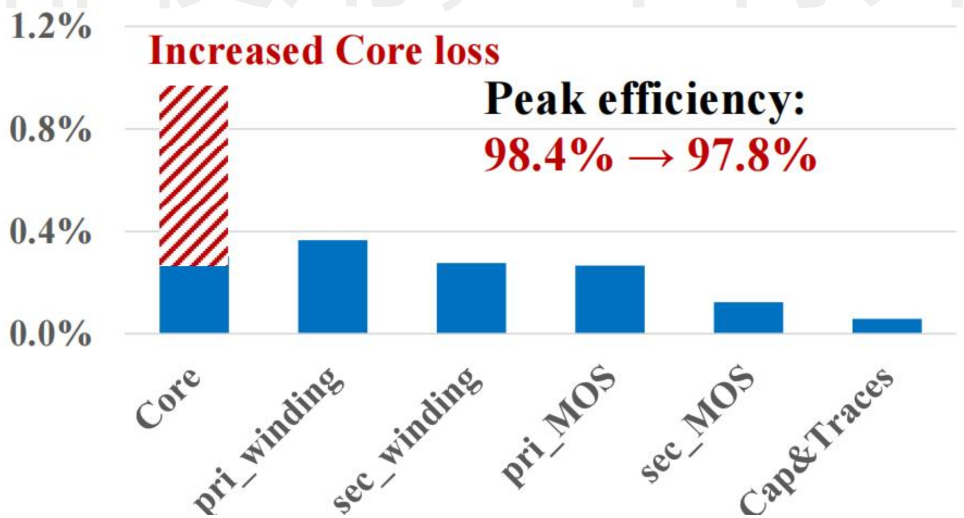
Core plate is thicker than chips





■ Volume Breakdown

■ Loss Breakdown @ peak efficiency



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Multi-window EI Core for Shrinking Plate Thickness

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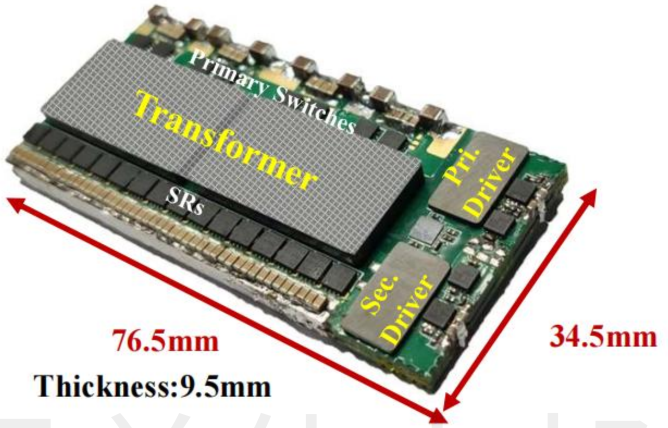

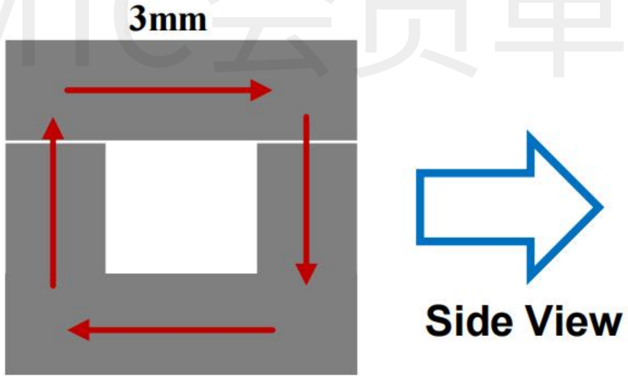

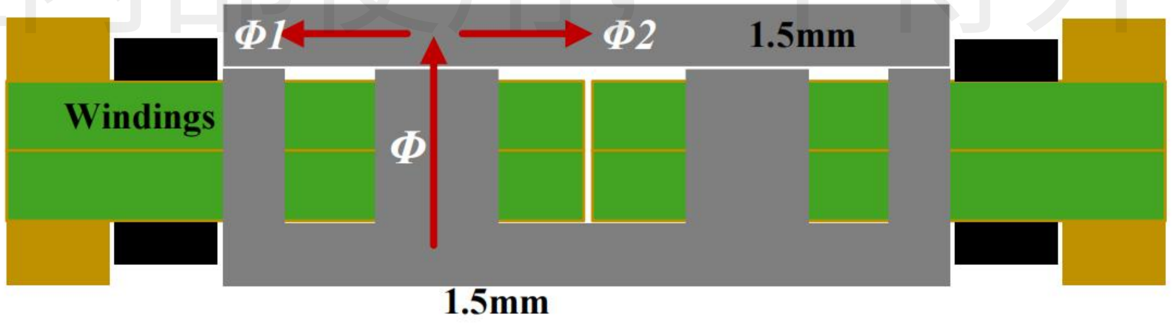

- Large thickness resulted by single-side flux flow in U Core

How to guarantee Φ1=Φ2 ?

The Requirement for Even Flux Distribution in Multi-_x0002_ Window EI Core

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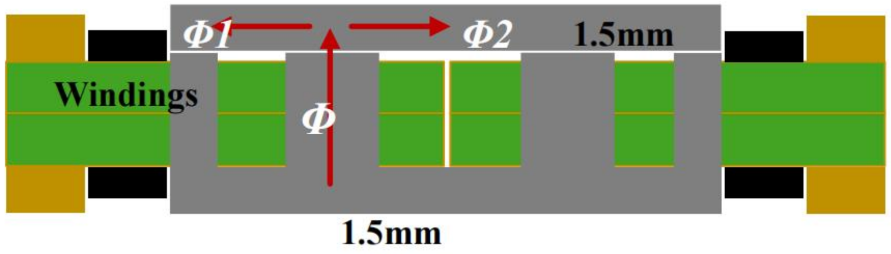
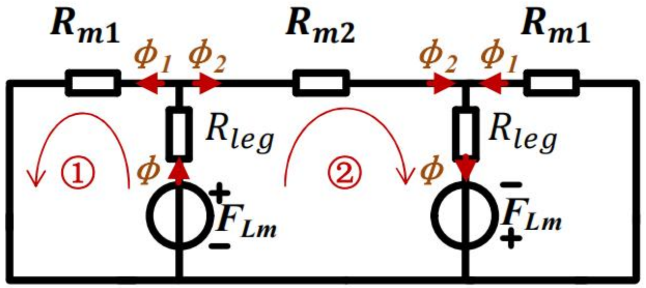
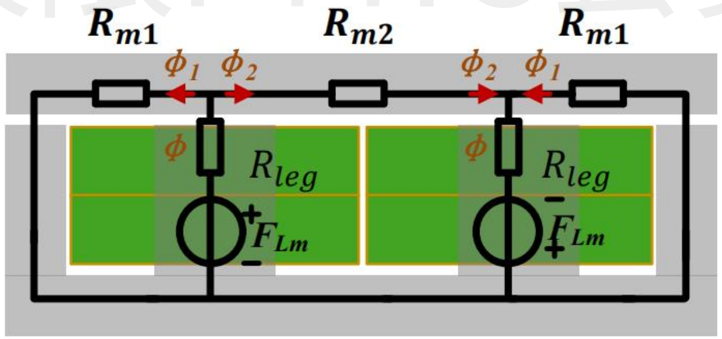




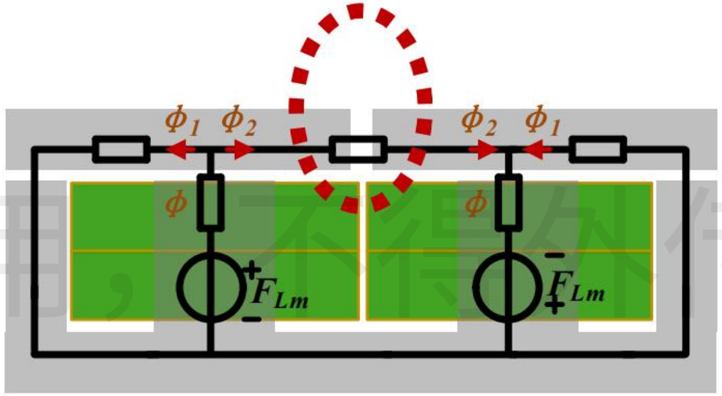
Magnetic resistance model



① $F_{Lm} - \emptyset R_{leg} = \emptyset_1 R_{m1}$

② $2\cancel{F_{Lm}} - 2\emptyset \cancel{R_{leg}} = \emptyset_2 R_{m2}$

①x2 $2\cancel{F_{Lm}} - 2\emptyset \cancel{R_{leg}} = 2\emptyset_1 R_{m1}$

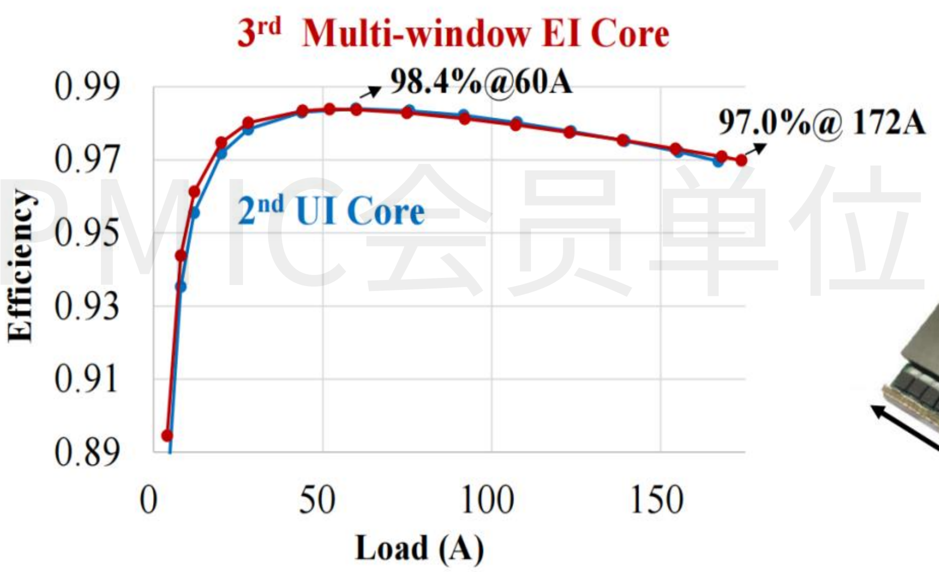


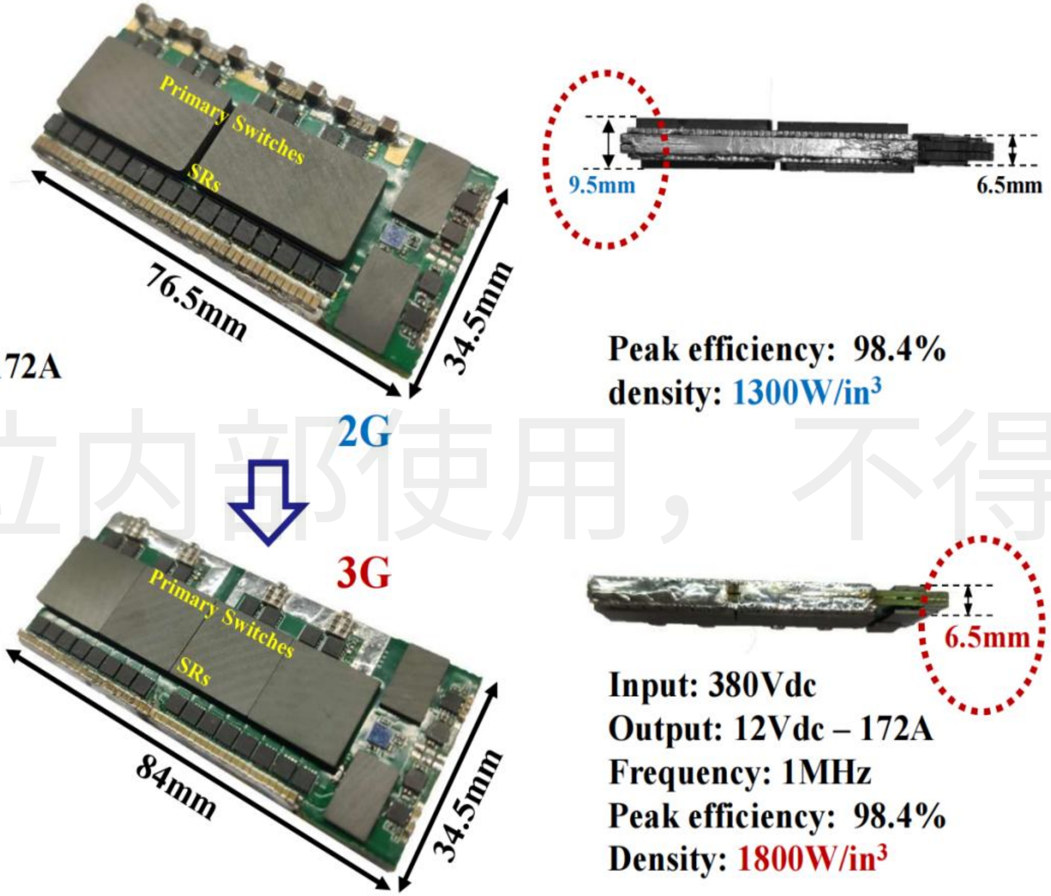
$$\frac{\emptyset_1}{\emptyset_2} = \frac{R_{m2}}{2R_{m1}}$$

$R_{m2} = 2R_{m1}$ to make $\Phi_1 = \Phi_2$

Comparison Between the Prototype Using U Cores (2G) and Multi-window EI Core (3G)

➤ **Efficiency of the Prototype**



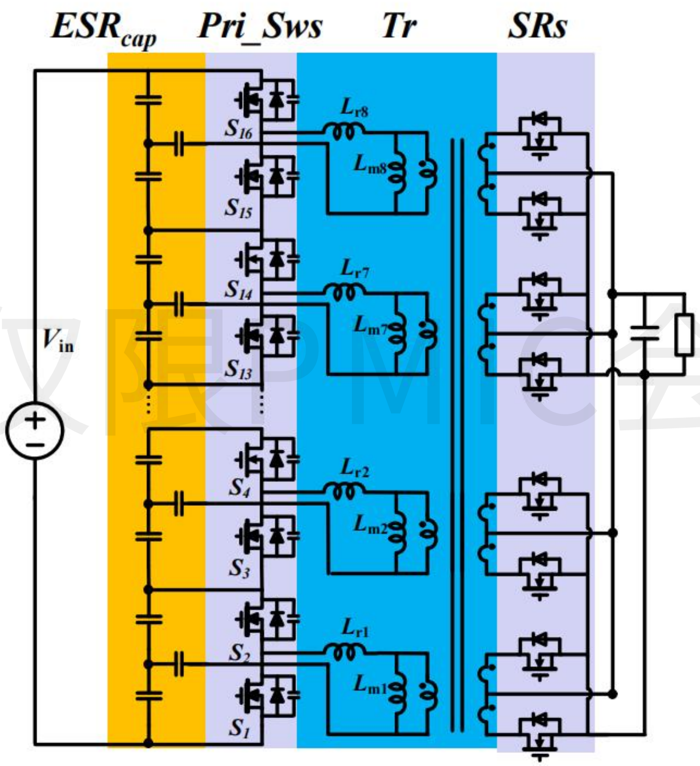


Peak efficiency: 98.4%
density: 1300W/in³

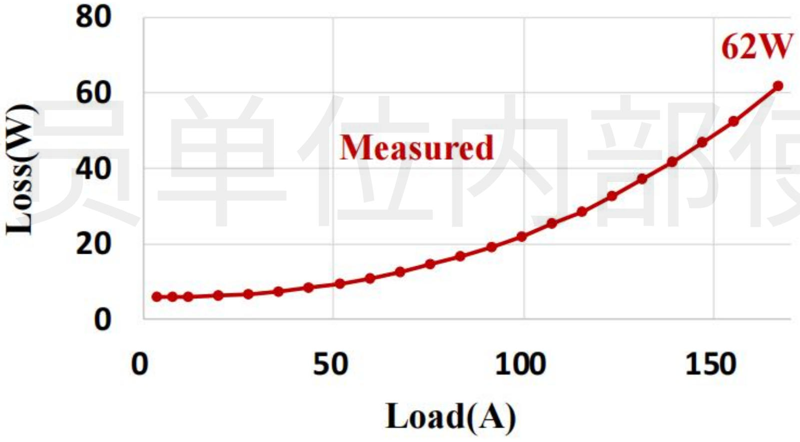
Input: 380Vdc
Output: 12Vdc – 172A
Frequency: 1MHz
Peak efficiency: 98.4%
Density: 1800W/in³

[4] Guangcan Li and Xinke Wu, "A 1.8kW/in³ Power Density Cellular 380V-12V DCX with 98.4% Peak Efficiency Using Low NFoM Devices and Resonant Drive Transformer," in PEAC 2022 (Accepted).

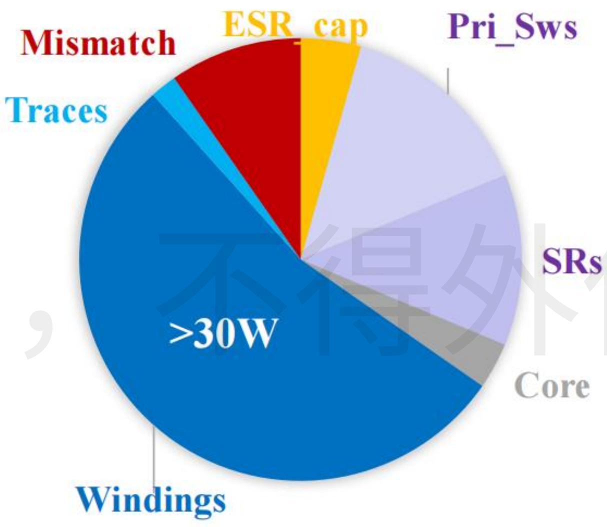
Loss Breakdown of the 3G Prototype



- Loss under different load



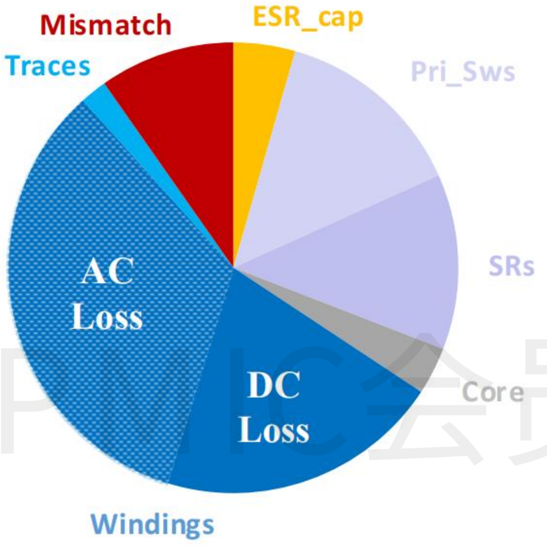
Loss Breakdown @Full Load



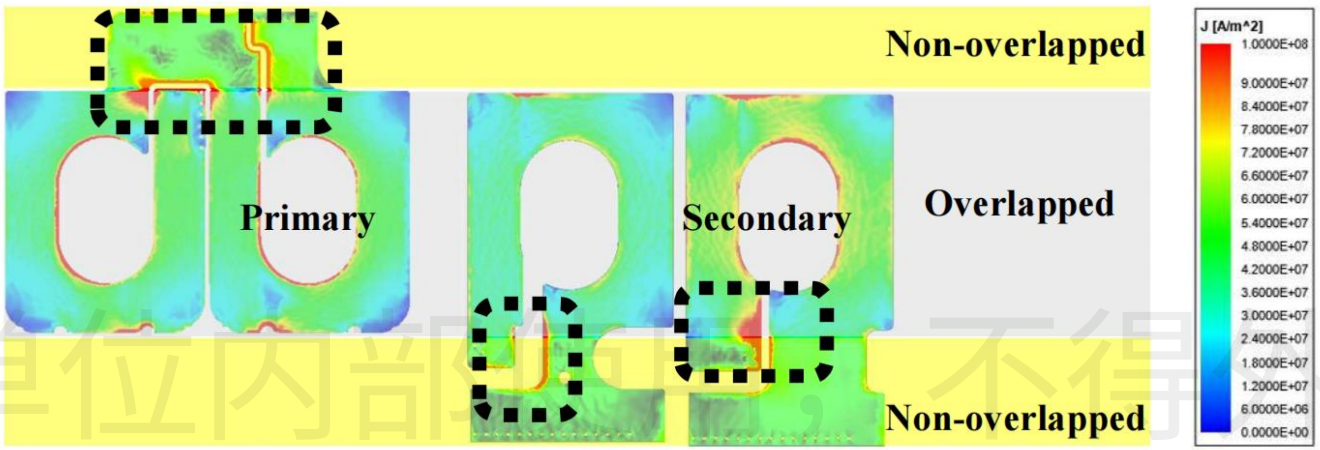
Large winding loss @full load

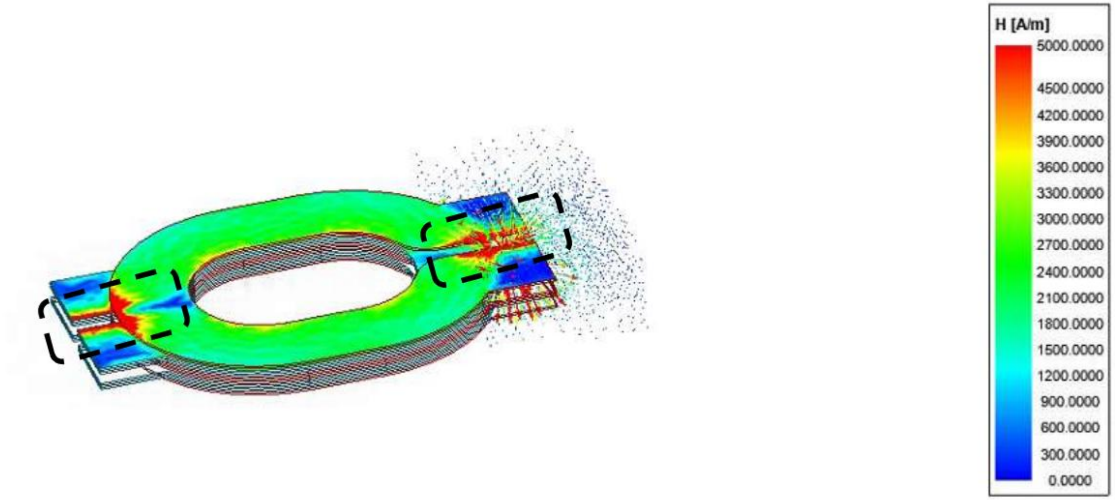
Eddy Current Loss of the Windings

➢ Loss Breakdown @ Full load



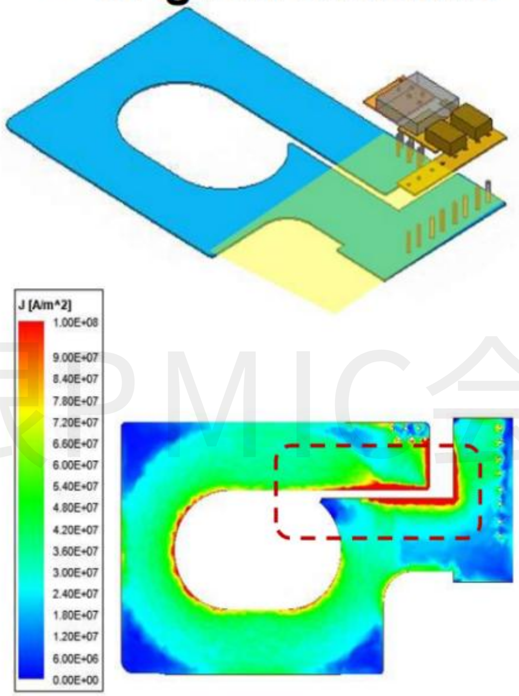
■ Large termination loss on windings @ 1MHz



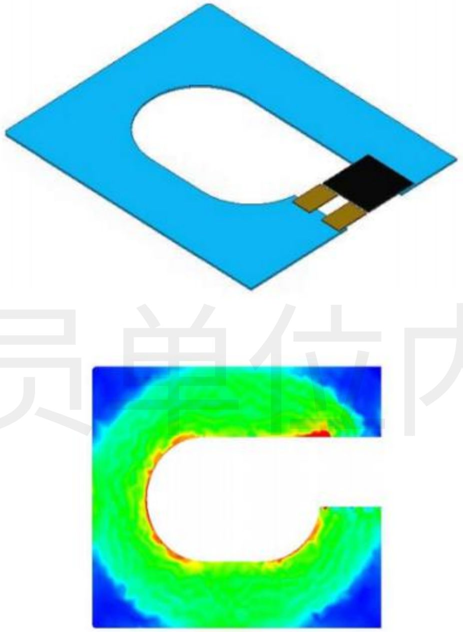


Typical Termination Loss Reduction Methods and 4th Generation Prototype

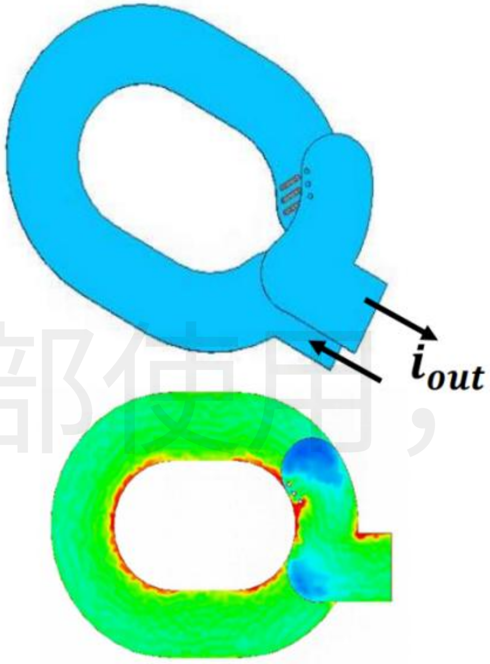
■ Original structure



■ Method 1



■ Method 2



Non-overlapped Termination results in large eddy current

Integrate SRs on windings

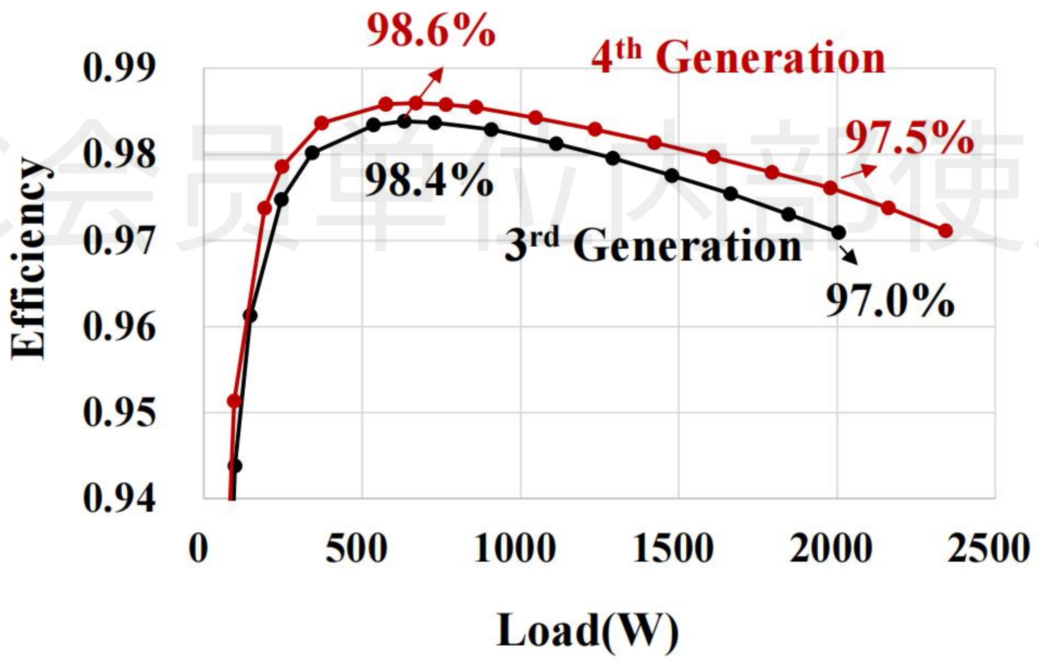
Interleave the termination

Efficiency Improvement with Termination Optimization

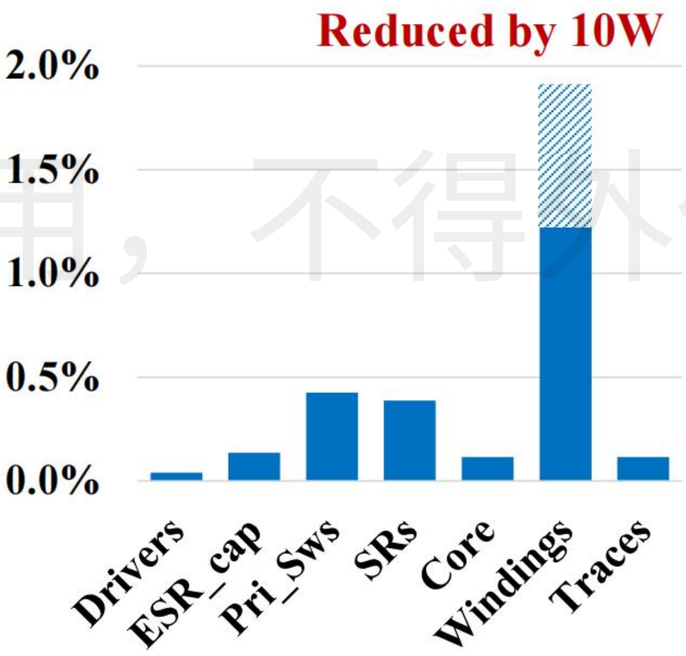
- After termination optimization

Input: 380Vdc
Output: 12Vdc

4th Generation



■ Loss Breakdown @ Po=2kW



Evolution of 1MHz 380V/12V 2kW Prototypes

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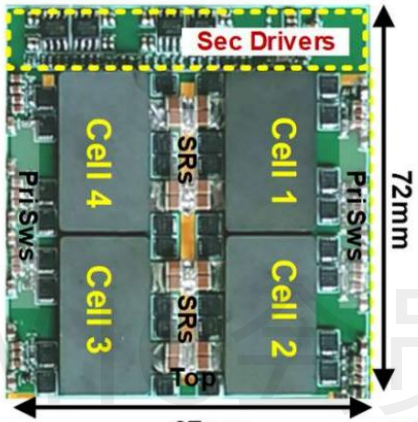
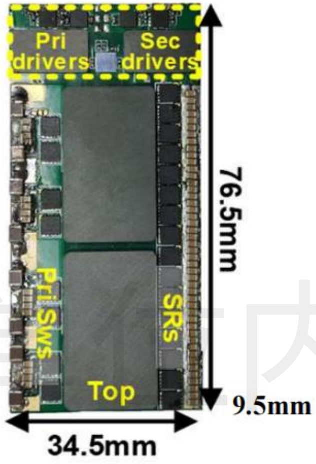
	1st G	2nd G	3rd G	4th G
Peak Efficiency	97.3%	98.4%	98.4%	98.6%
Power Density	0.8kW/in³	1.3kW/in³	1.8kW/in³	2.1kW/in³

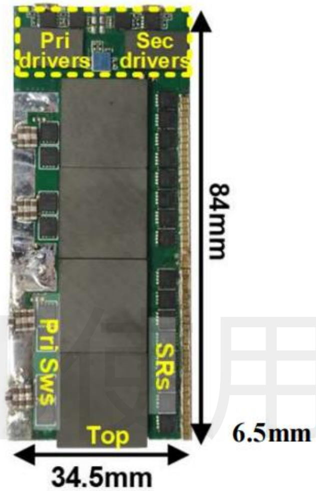


(2018)



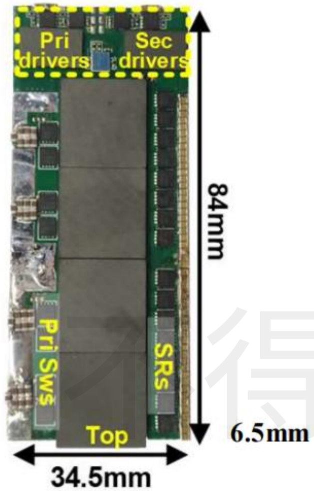
(2020)

Resonant Drive Tr.



(2022. May)

Multi-window EI Tr.

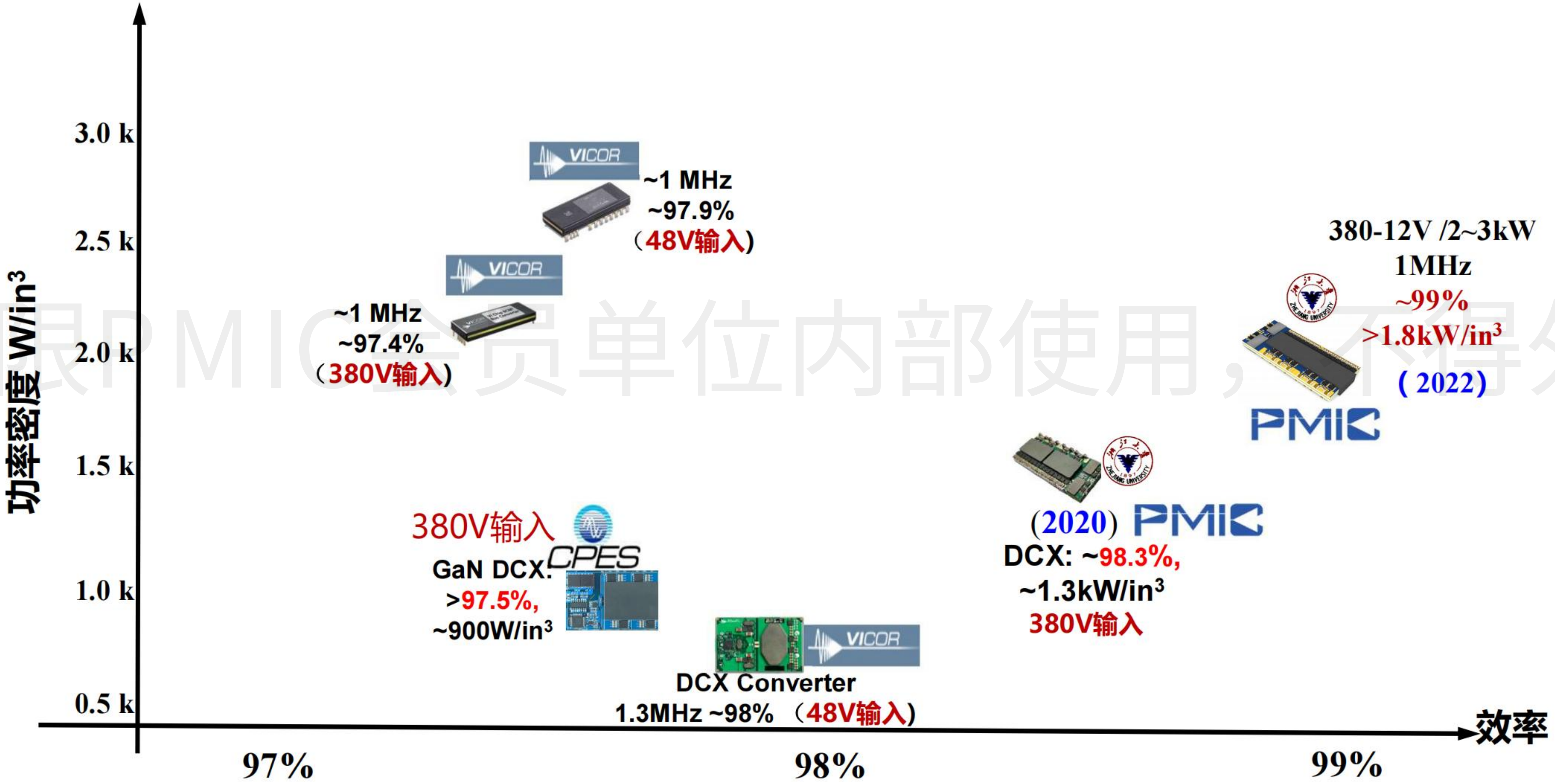


(2022. Nov.)

Termination optimizing

1st G → 2nd G → 3rd G → 4th G

380V-12V DC/DC模块技术发展



感谢电源管理技术创新联盟(PMIC)资助！

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英飞源技术 INFY POWER
OPPO
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SILERGY
KIWI INSTRUMENTS
AOHAI 奥海科技
vivo
杰瑞
派恩杰
JOULWATT
INOVANCE
FOX ESS 麦田能源
Anker Innovations
DMEGC
纳微 Navitas
Great Wall 长城电源
ZTE中兴
EVTECH 富特科技
INVENTRONICS 英飞特电子
Innoscience 英诺赛科
BPS 晶丰明源
Signify
BOCO 铂科电子
CukTech
SINOMAGS 希磁科技

电源管理技术创新联盟(PMIC)--会员制

Power Management Innovation Consortium

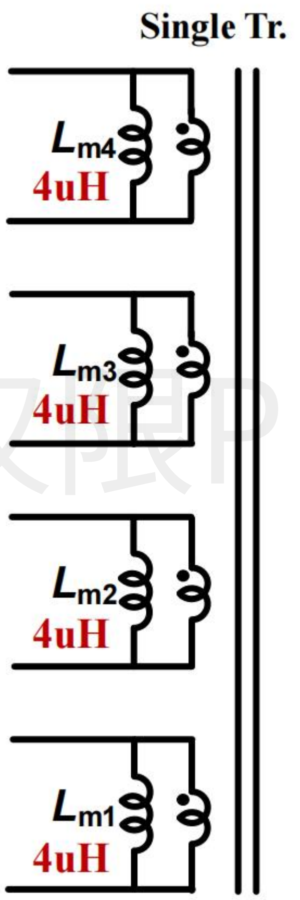
PMIC 高校主导、行业共建的电源管理技术生态链

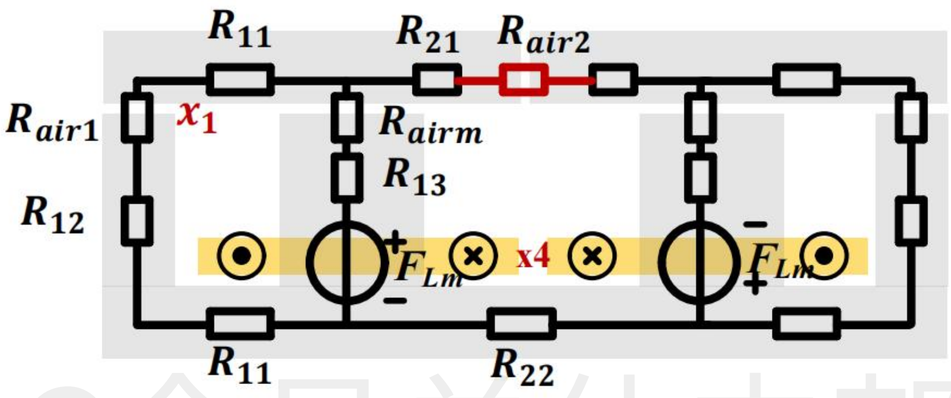
器件	装置	系统
矽力杰半导体	深圳英飞源技术	OPPO技术
杰华特半导体	杰瑞电子(716所)	台达电子
派恩杰电子	长城电源	VIVO技术
纳微半导体	杭州英飞特新能源	汇川技术
英诺赛科	铂科电子	中兴通讯
横店东磁	奥海科技	安克创新
希磁科技	昕诺飞(原飞利浦)	
必易微电子	酷科电子（紫米）	
晶丰明源	杭州富特科技	
	麦田能源	

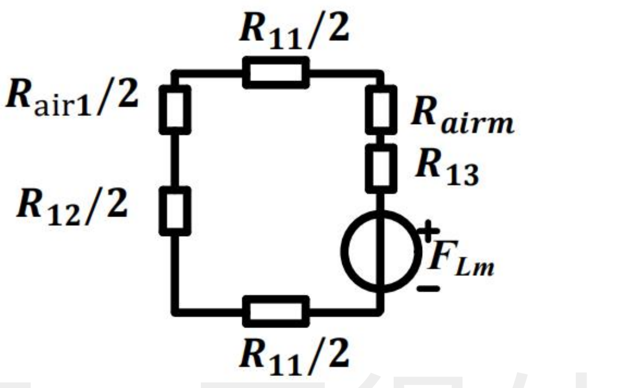
- 国内首个
- 合作生态
- 模式探索
- 未来技术

Thanks for your time

Backup - Appendix A —— Calculation of the Airgap





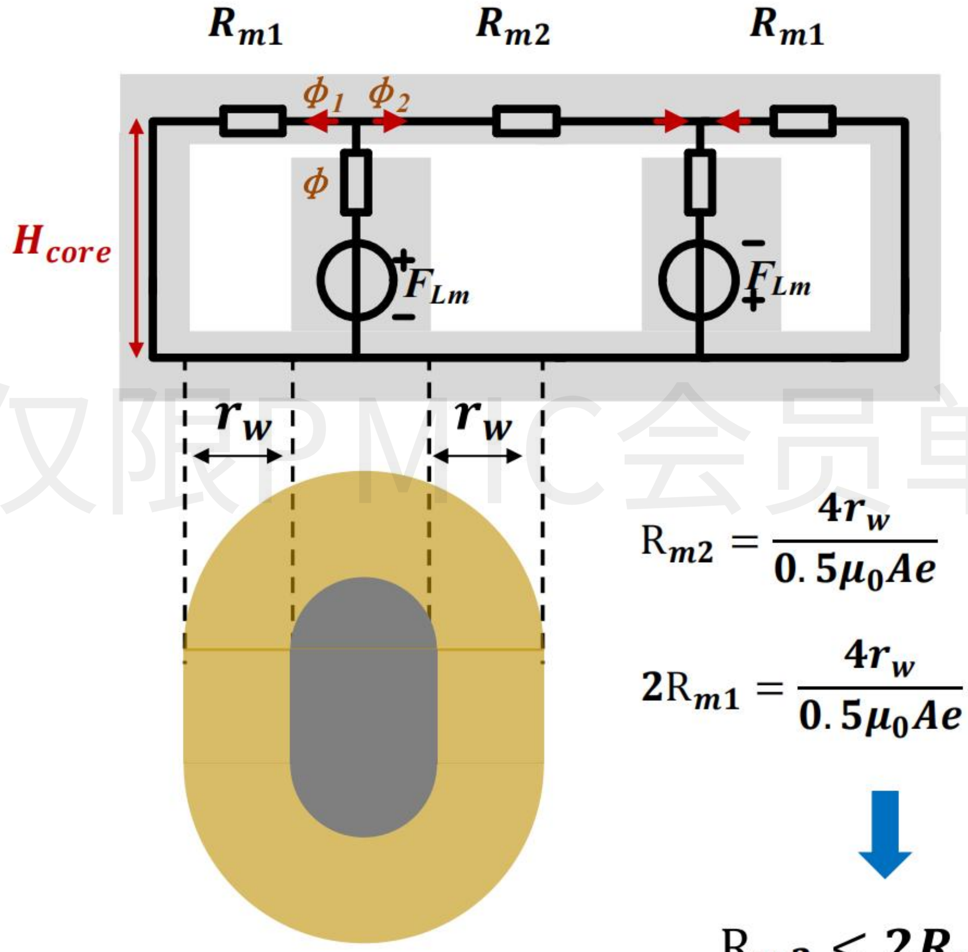


Equivalent Loop for Lm calculation

$$\begin{cases} R_{\mathrm{air1}} = \dfrac{x_1}{0.5\mu_0 Ae} \\ R_{\mathrm{airm}} = \dfrac{x_1}{\mu_0 Ae} \\ 16uH \approx 2 * 4^2 * \dfrac{1}{R_{airm} + R_{air1}/2} \\ \sum R_{2i} + R_{air2} = 2(\sum R_{1i} + R_{air1}) \end{cases}$$

$$x_1 \approx 60um, x_2 \approx 130um$$

Backup - Appendix B —— No Airgap on Side Core Legs

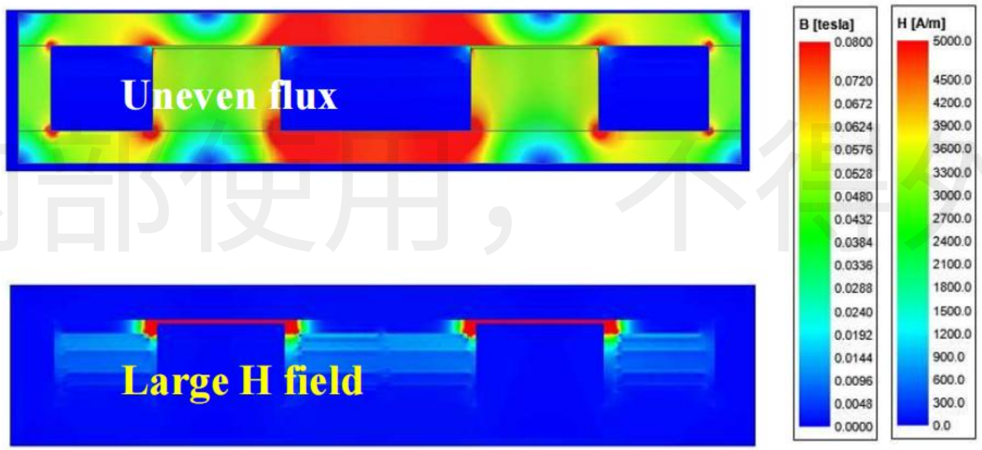


$$R_{m2} = \frac{4r_w}{0.5\mu_0 Ae}$$

$$2R_{m1} = \frac{4r_w}{0.5\mu_0 Ae} + \frac{2H_{core}}{0.5\mu_0 Ae}$$

$$R_{m2} < 2R_{m1}$$

■ **3D Simulation Results**



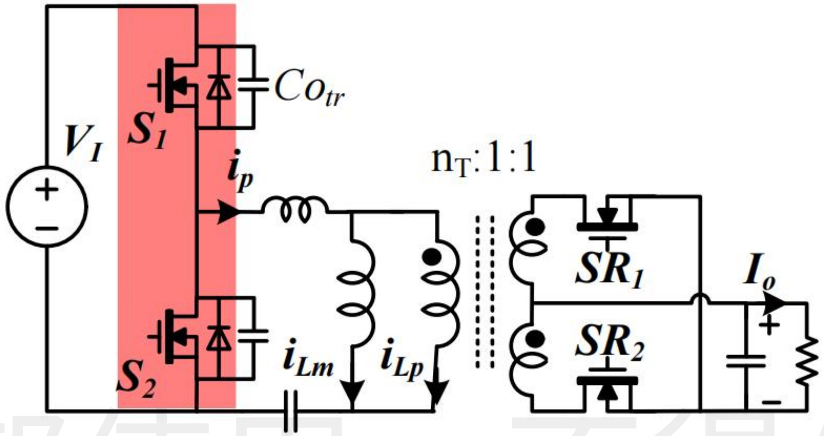
Total winding loss ~0.5W @0.4A Io

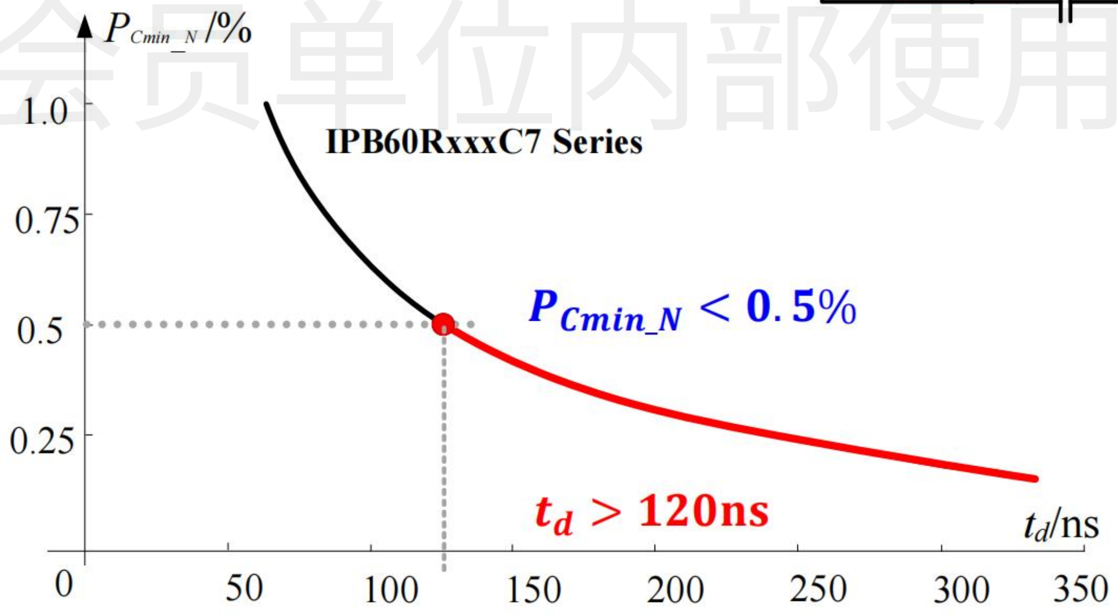
Larger t_d Leads to Less Pri. Conduction Loss

Normalized primary conduction loss:

η: efficiency

$$P_{Cmin\_N} = \frac{P_{Cmin}}{P_o} = \frac{2\pi\eta * NFoM}{t_d}$$





Larger t_d Results in higher RMS Current in Windings

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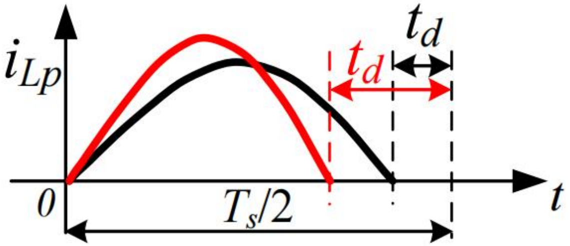
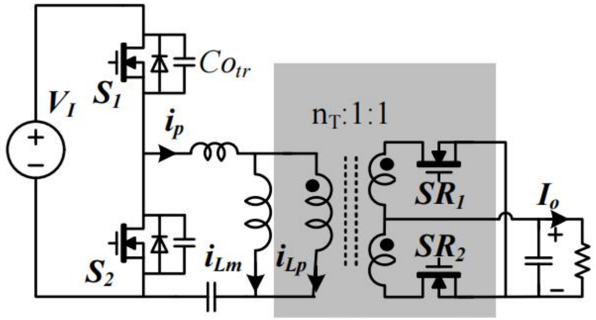
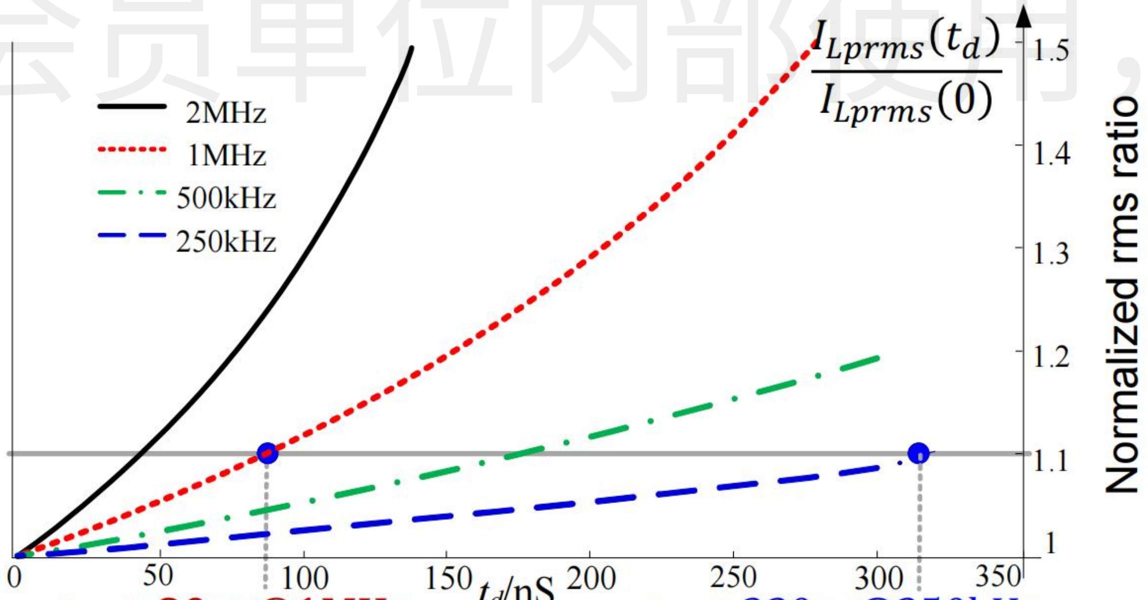
RMS current vs. t_d





t_d ↑→Winding loss & SR conduction loss↑

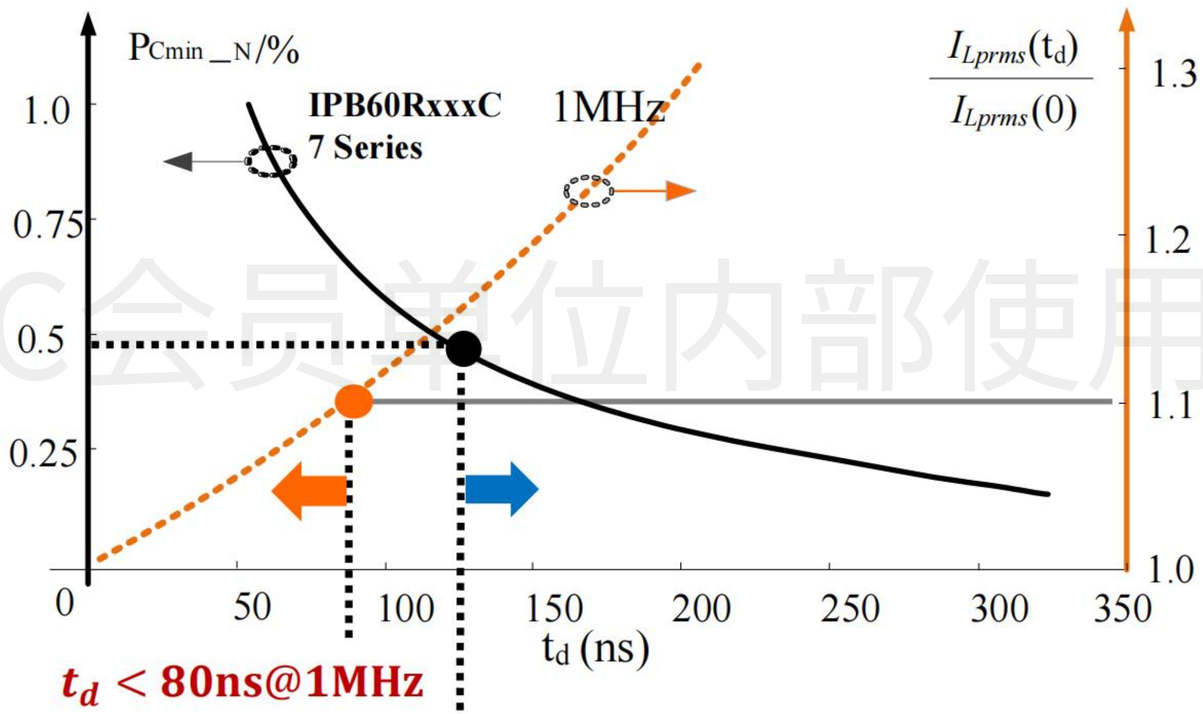


t_d < 80ns@1MHz

t_d < 320ns@250kHz

Great Challenge between Pris. and Winding Loss at MHz Level Achieving High Efficiency

$$P_{Cmin\_Normalized} = \frac{2\pi * \eta * NFoM}{t_d}$$



t_d < 80ns@1MHz

No Overlap @ 1M

Impossible of 98% efficiency with Current High Voltage Si devices.

Achieve High Efficiency at MHz when Using Series Connected Low NFoM Devices

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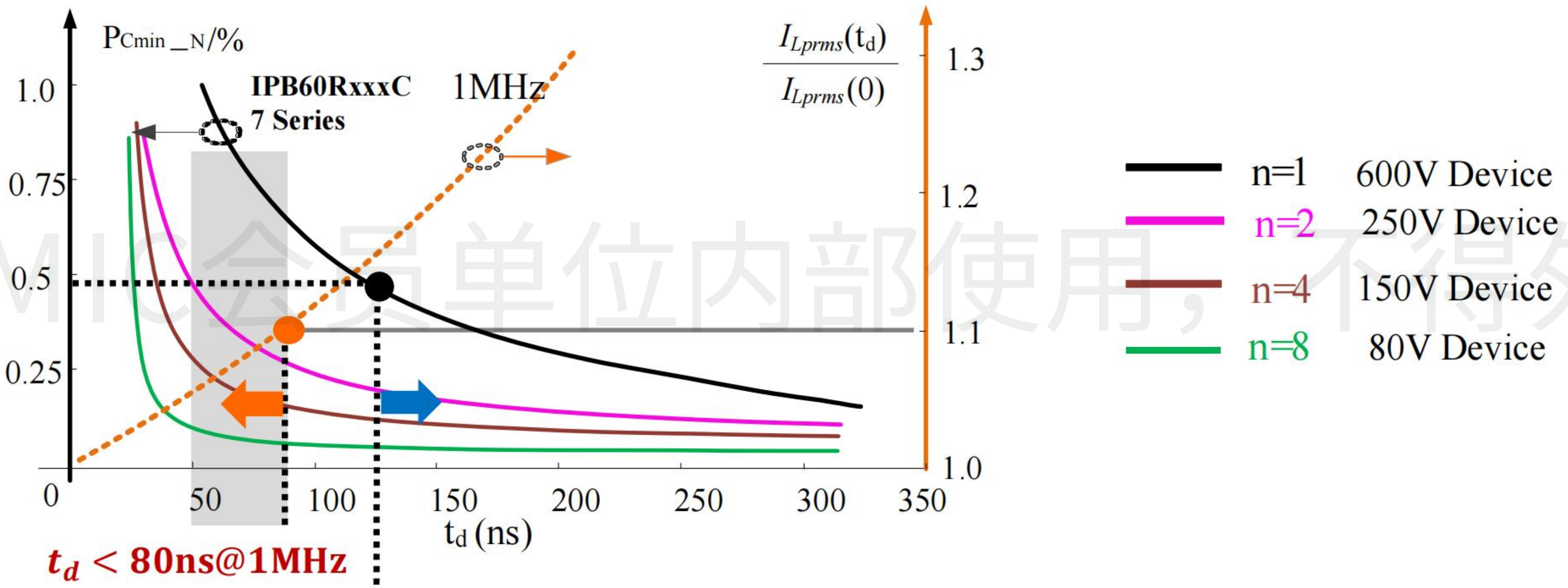
$$P_{Cmin\_N} = \frac{P_{Cmin}}{Po} = \frac{2\pi * \eta * NFoM}{t_d}$$



Overlap appear @ 1M

98% efficiency is available with Low Voltage Si devices at MHz.