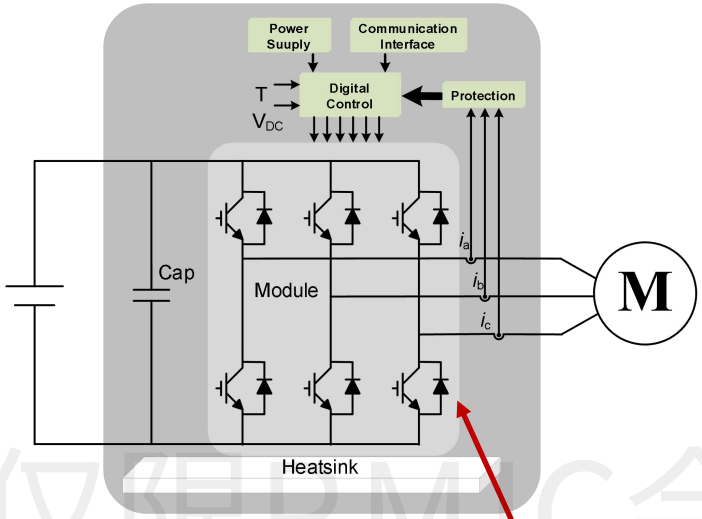
碳化硅双面散热模块的银烧结工艺及模块测试

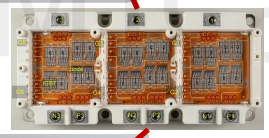
Silver Sintering Technology and Module Test of SiC Double-Side-Cooling (DSC) Module

报告人：董泽政 博士

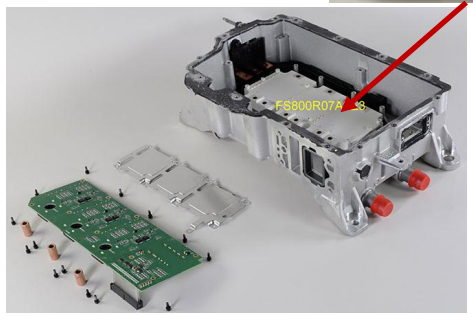
Power Density of Traction Inverter from Various EVs

Power Management Innovation Consortium

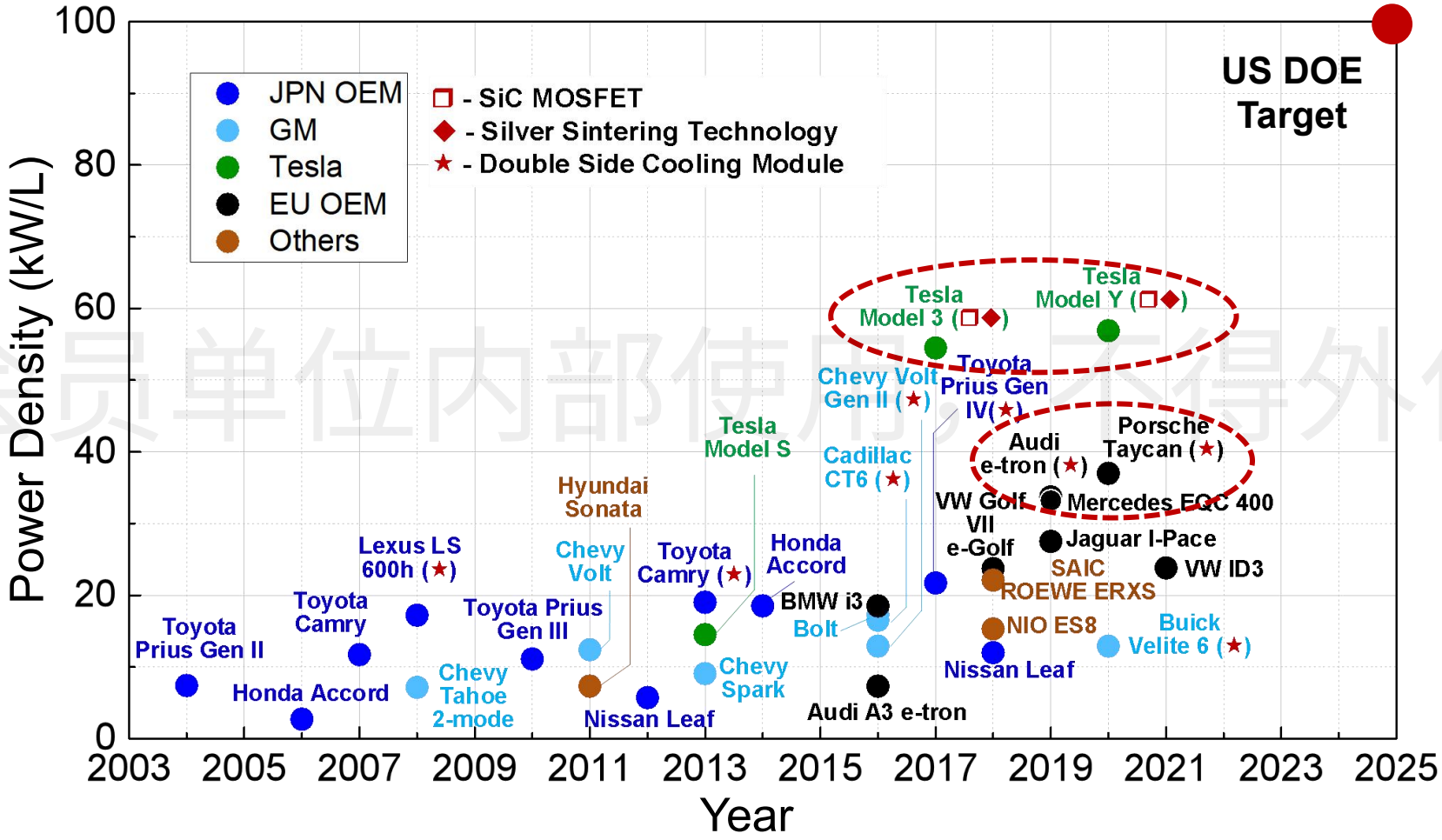




Power Module



Traction Inverter



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Liu M, Coppola A, Alvi M, et al. Comprehensive Review and State of Development of Double-Sided Cooled Package Technology for Automotive Power Modules[J]. IEEE Open Journal of Power Electronics, 2022, 3:271-289.

Double Side Cooling (DSC) Power Module in EV

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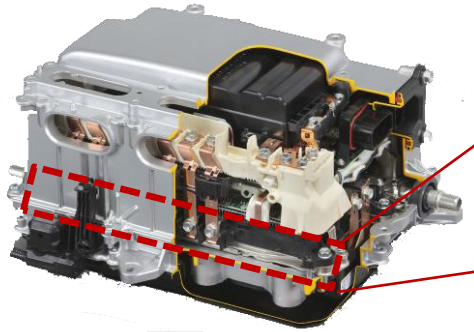
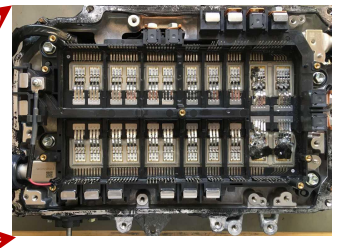
3rd Generation PCU

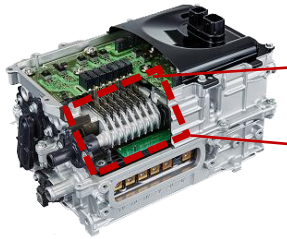


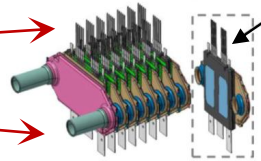


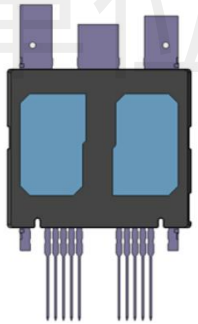
Sing Side Cooling
Power Module

33% Volume Reduction !

4th Generation PCU

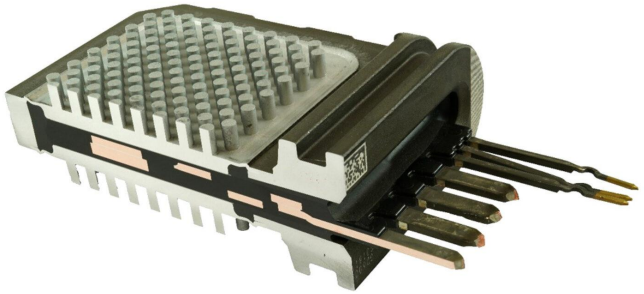




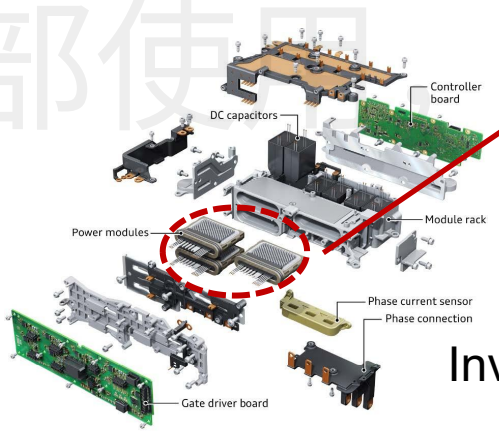


Double Side Cooling
Power Card

Power Control Unit (PCU, Toyota)



Power Module

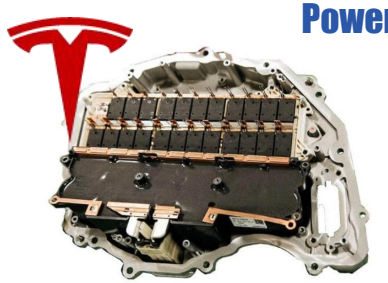


Inverter

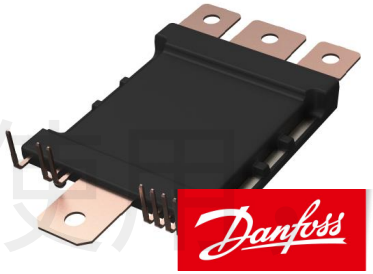
Double Side Cooling Power Module from Hitachi (Audi e-tron)

Advantages of Silver Sintering Technology

PMIC
Power Management Innovation Consortium

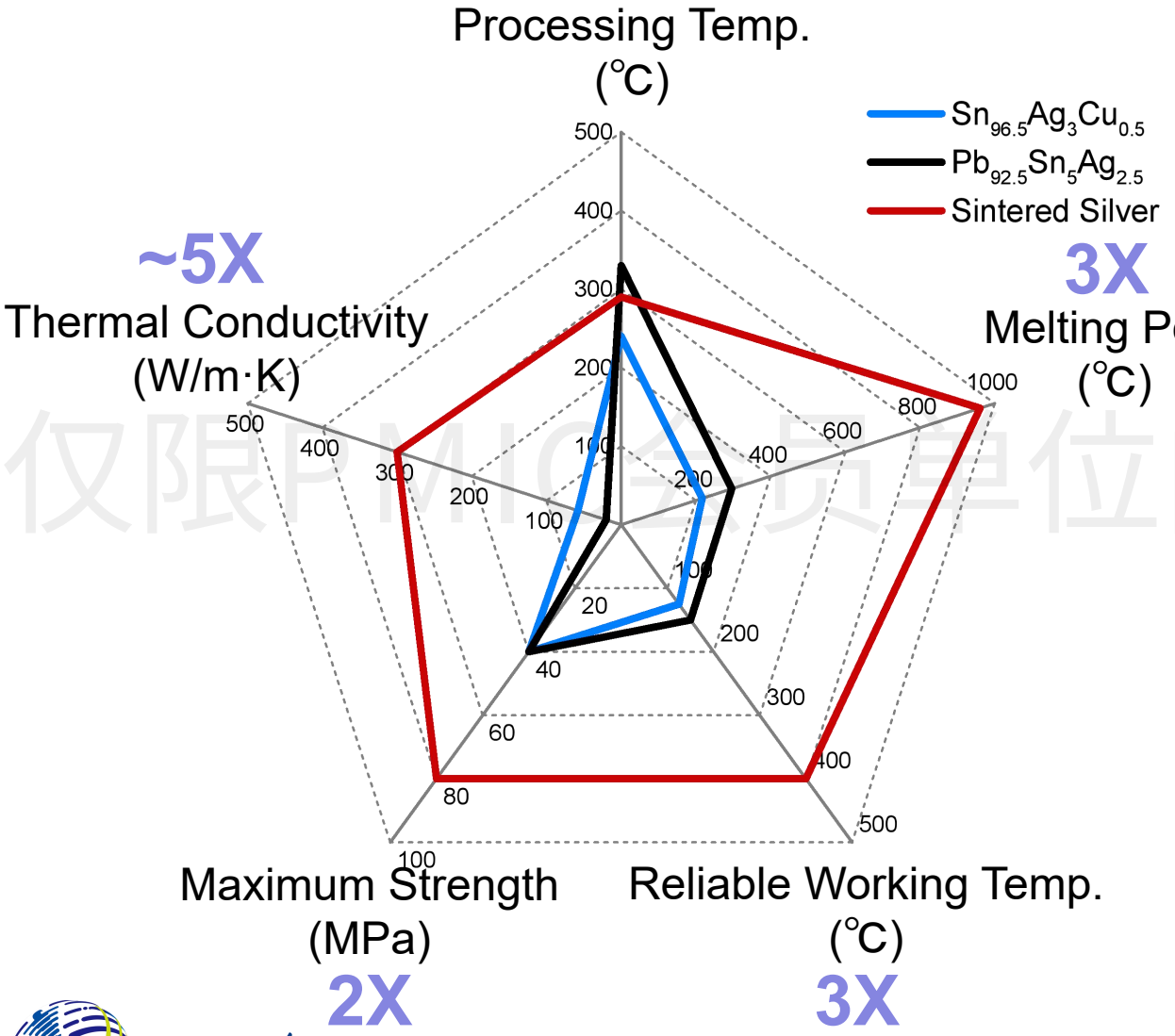


- 24 1-in-1 STPAKs;
- Sintered on a Heatsink;
- 175℃.

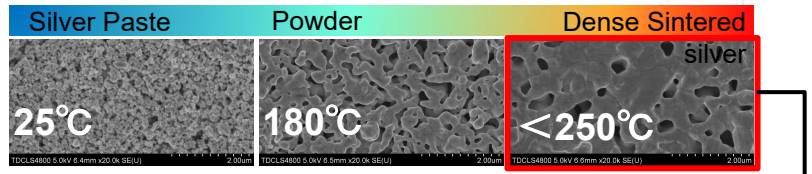


- 1200V/800A SiC ;
- Sintering SiC Top Metal Plate & Backside;
- 175℃.

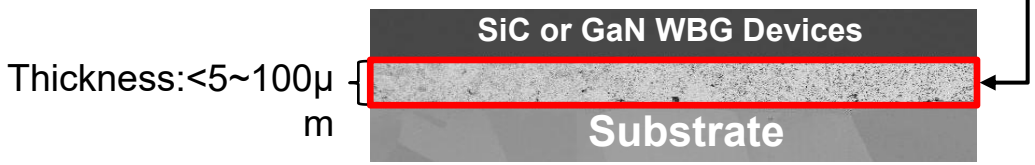
15X lifetime* !



SEM Microstructure after Sintering



Sintered Silver Joint interface



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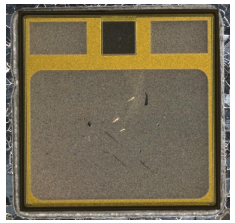
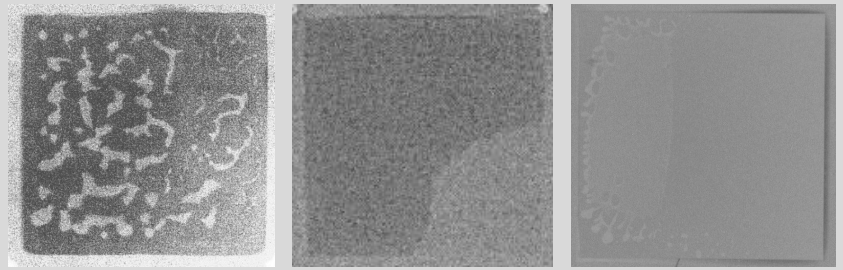
*F. Carastro, et al., "DCM-1000X -Automotive Power Module Technology Platform Optimized for SiC Traction Inverters," in IEEE APEC 2021

Conventional Process Issues of Silver Paste

Printing → Die Attaching → Sintering

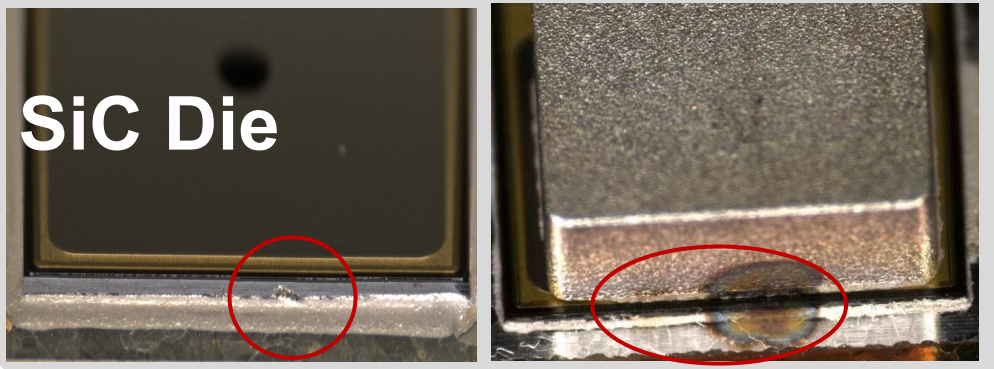




Typical Void and Delamination Defects

Overflow Issue

Creepage Issue



- Overflow & Creepage issue
- Defect Control
- Thickness Consistency

Sintering Thickness：50-80 μm
Thickness Tolerance：>±10 μm

Film Transfer Technique based on Silver Paste

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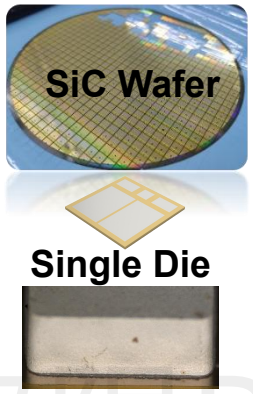
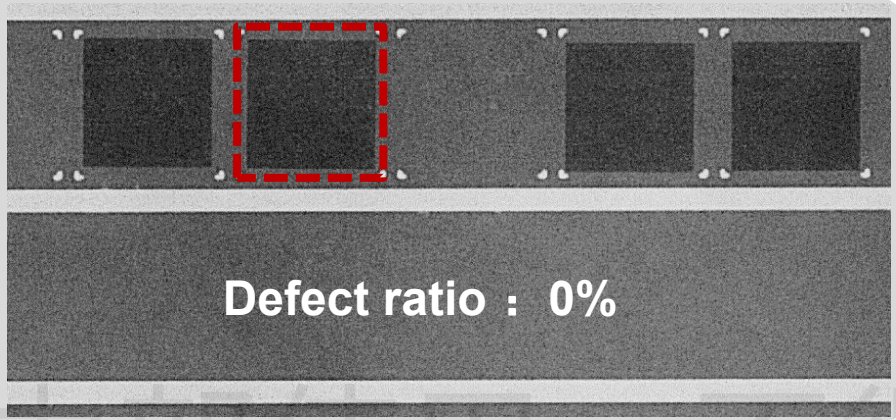
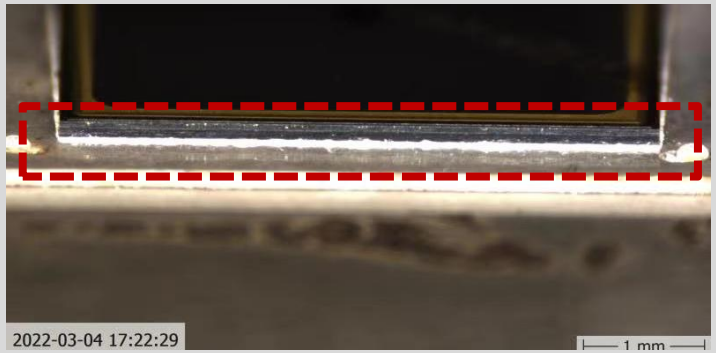
Silver Paste Film Transfer Technique

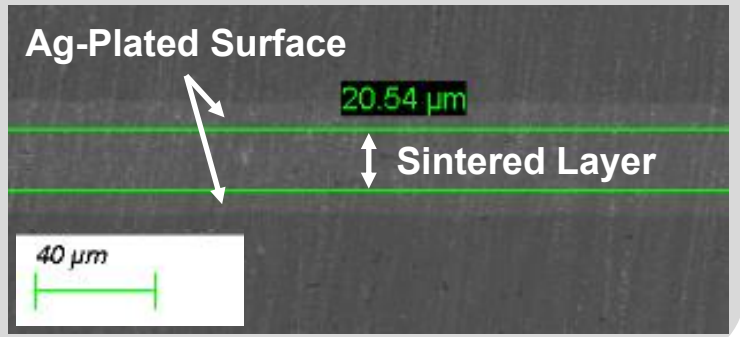




Overflow of sintered silver：＜10-20μm



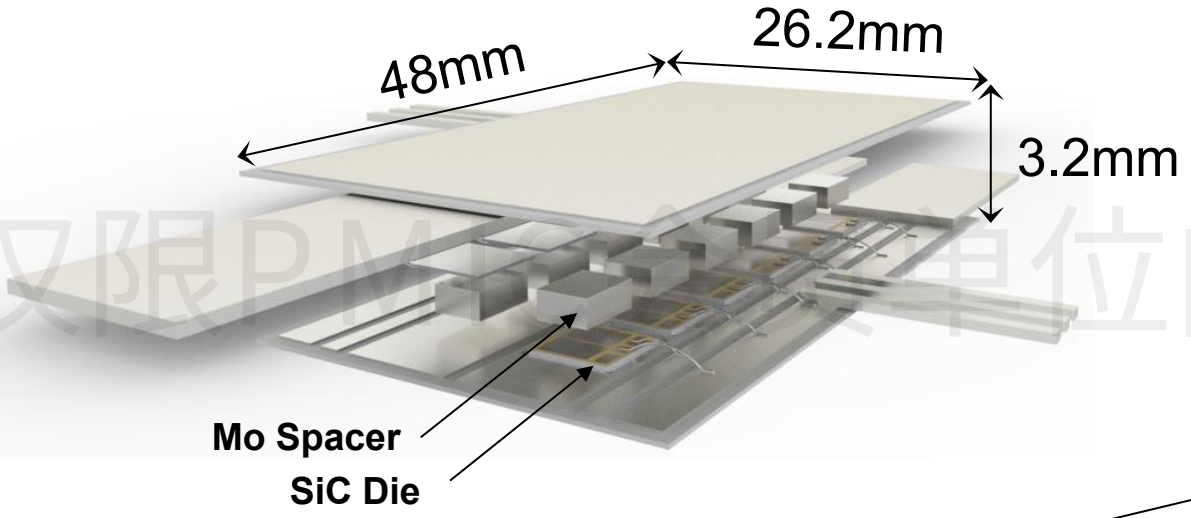
- **Negligible Overflow**
- **No Defects**
- **Consistent Thickness**

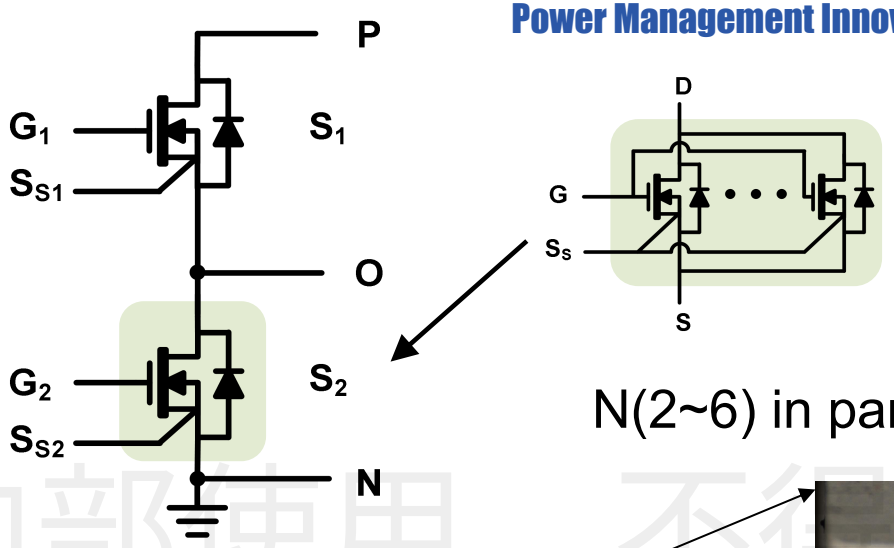


Sintering Thickness：＜20-100 μm
Thickness Tolerance：＜±3 μm

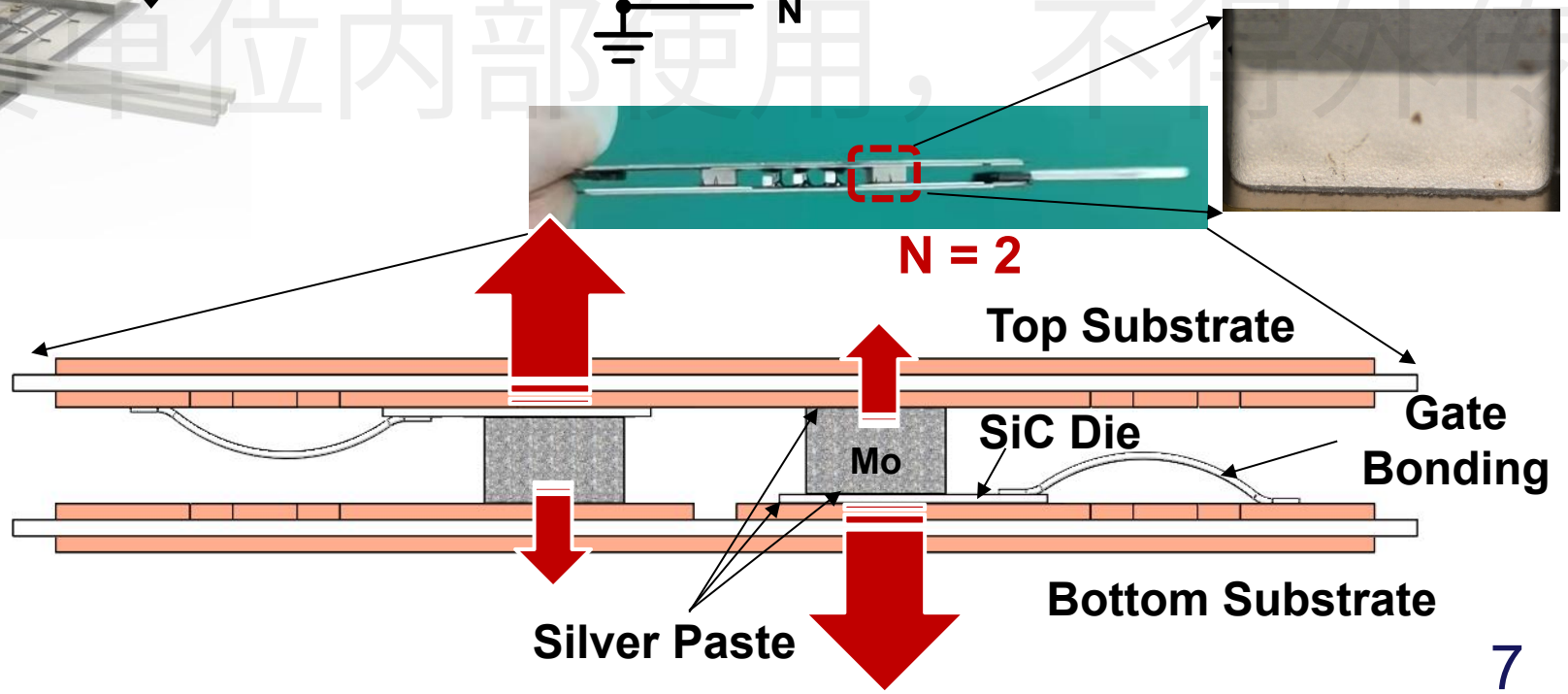
DSC SiC Power Module

N Dies in Parallel (N=2~6)





N(2~6) in parallel



$V_{(BR)DSS}$ Characteristics of DSC SiC Power Module

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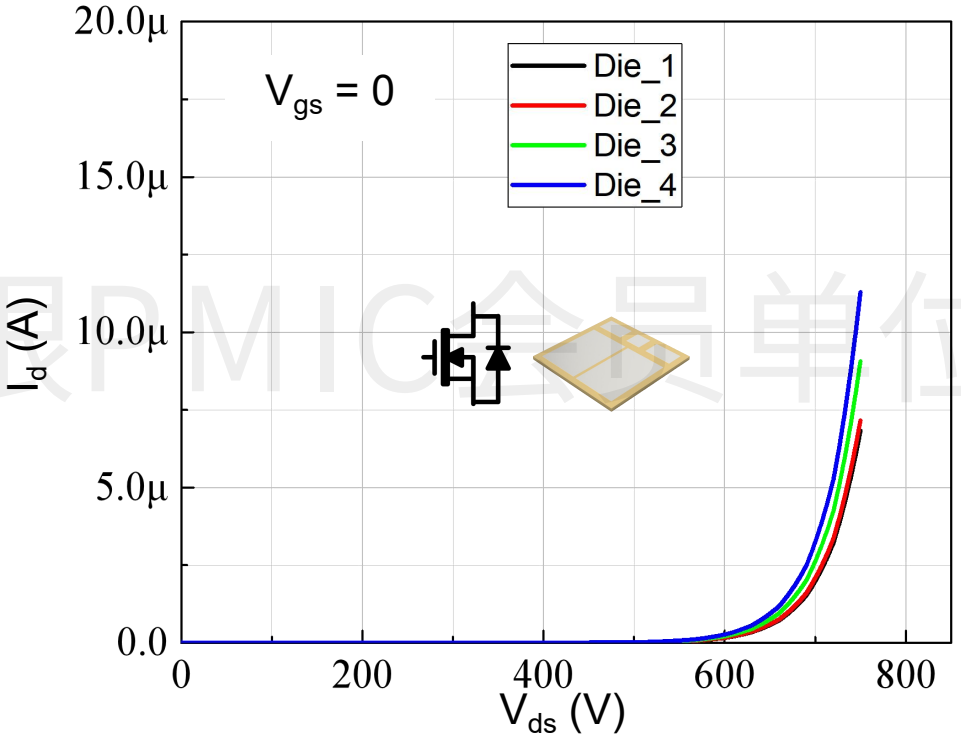
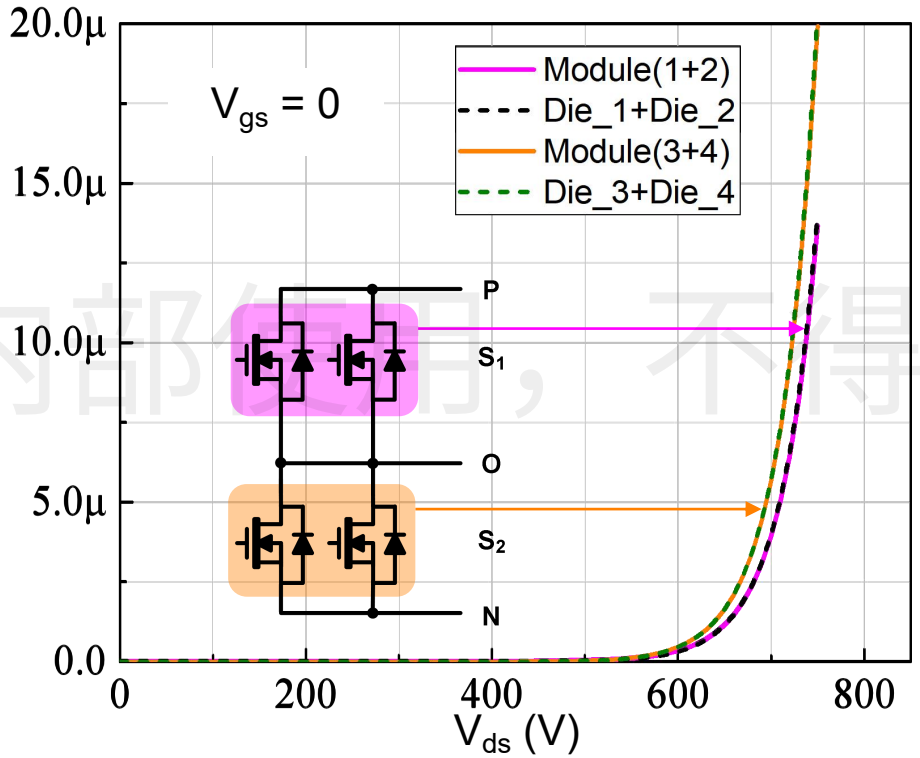
@25 ℃ Die Specification : 750V/8mΩ, 5×5 mm²

Single Die

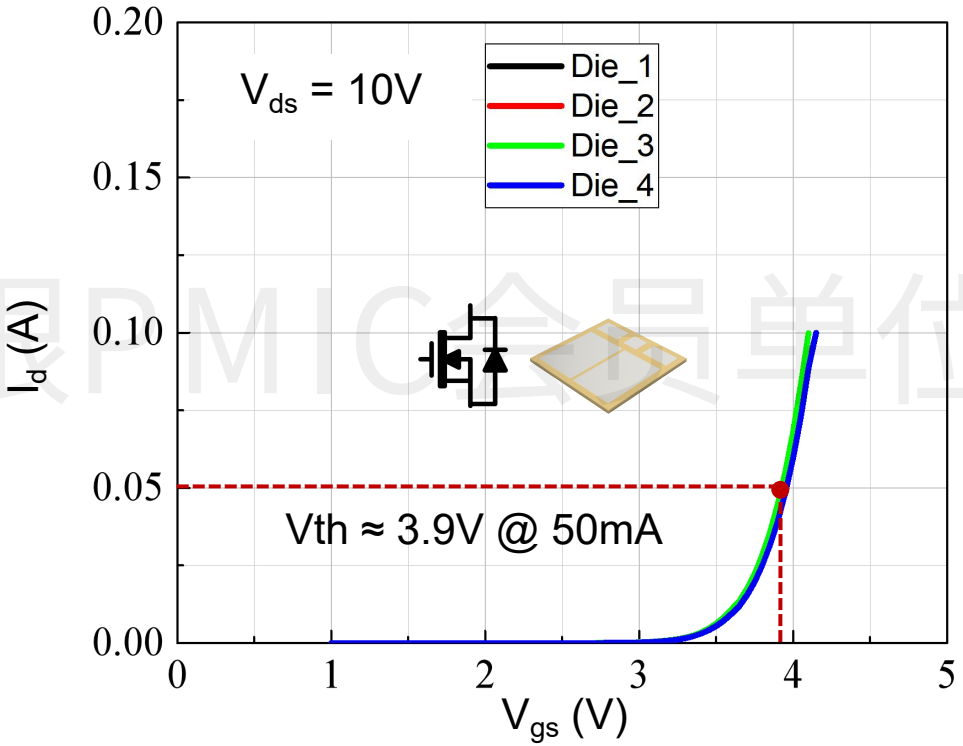


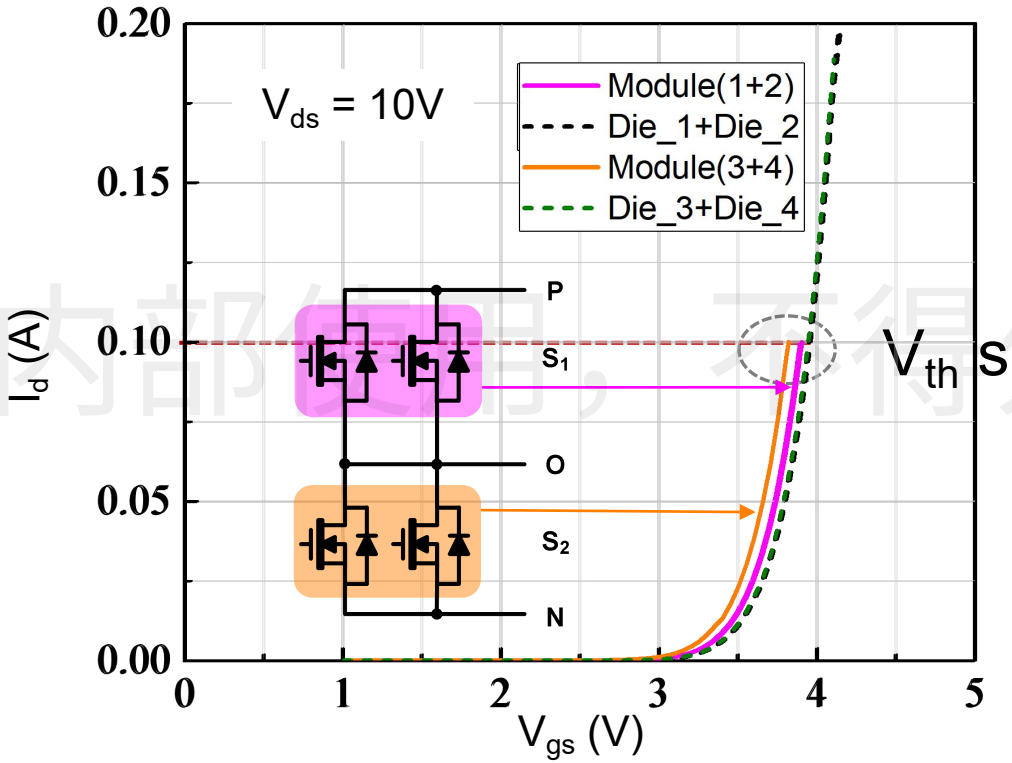


V_{th} of DSC SiC Power Module

Power Management Innovation Consortium

@25 ℃

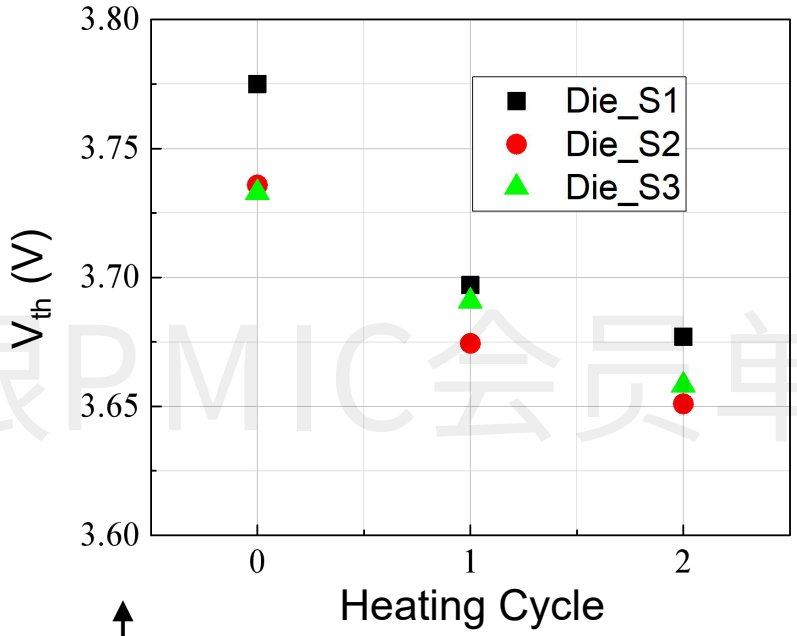


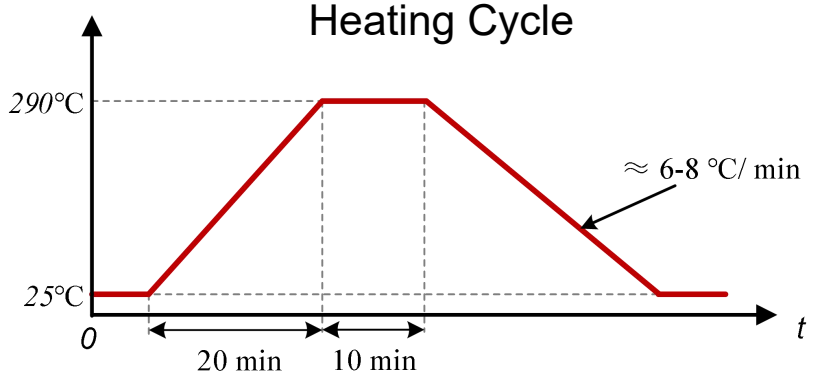


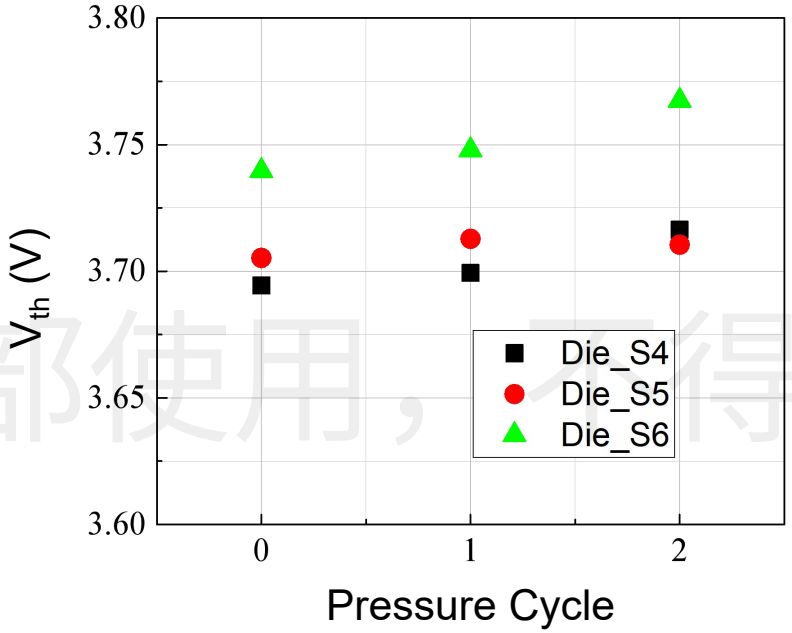
- Temperature ?
- Pressure ?

V_{th} Shift (Temperature or Pressure)

V_{th} @ V_{ds} = 10V, I_d = 50mA







15MPa, 5min

Forward $R_{ds(on)}$ of DSC SiC Power Module

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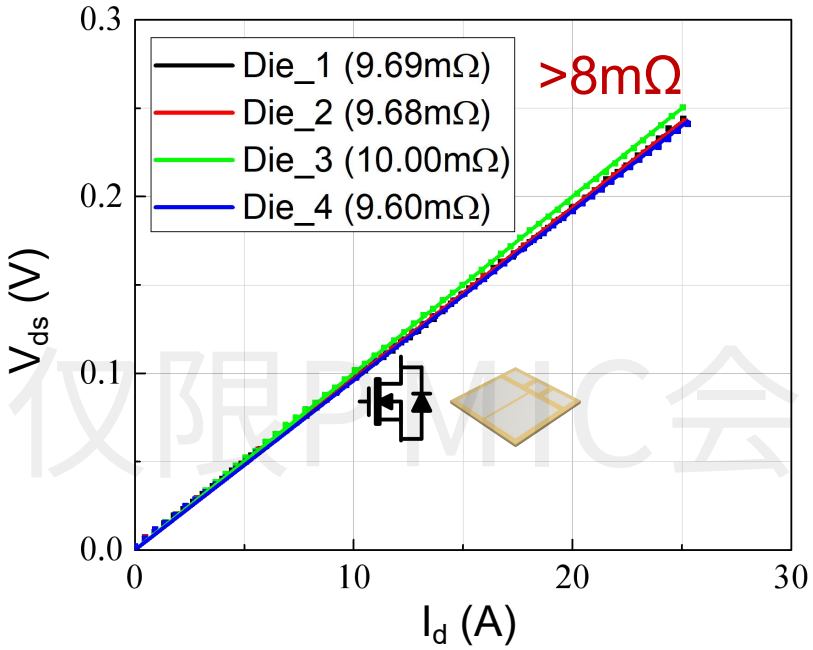
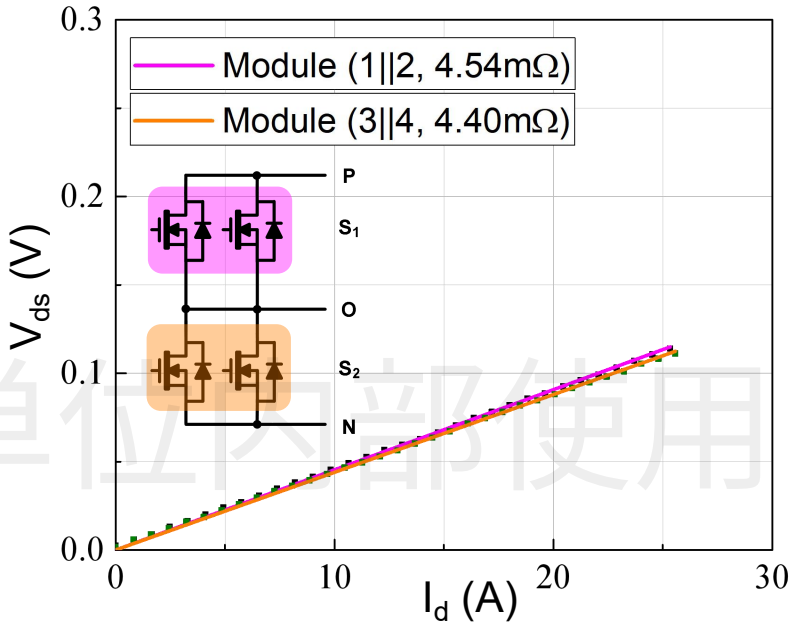
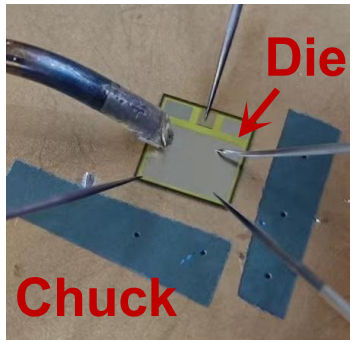
@25 ℃ Die Specification : 750V/8mΩ, 5×5 mm²



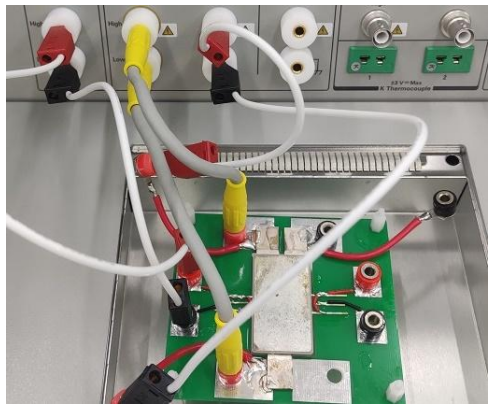


4.54mΩ < **4.84**mΩ (Die_1 + Die_2)

4.40mΩ < **4.90**mΩ (Die_3 + Die_4)



High
Contacting Resistance



No Contacting Resistance
(Sintering & Soldering)

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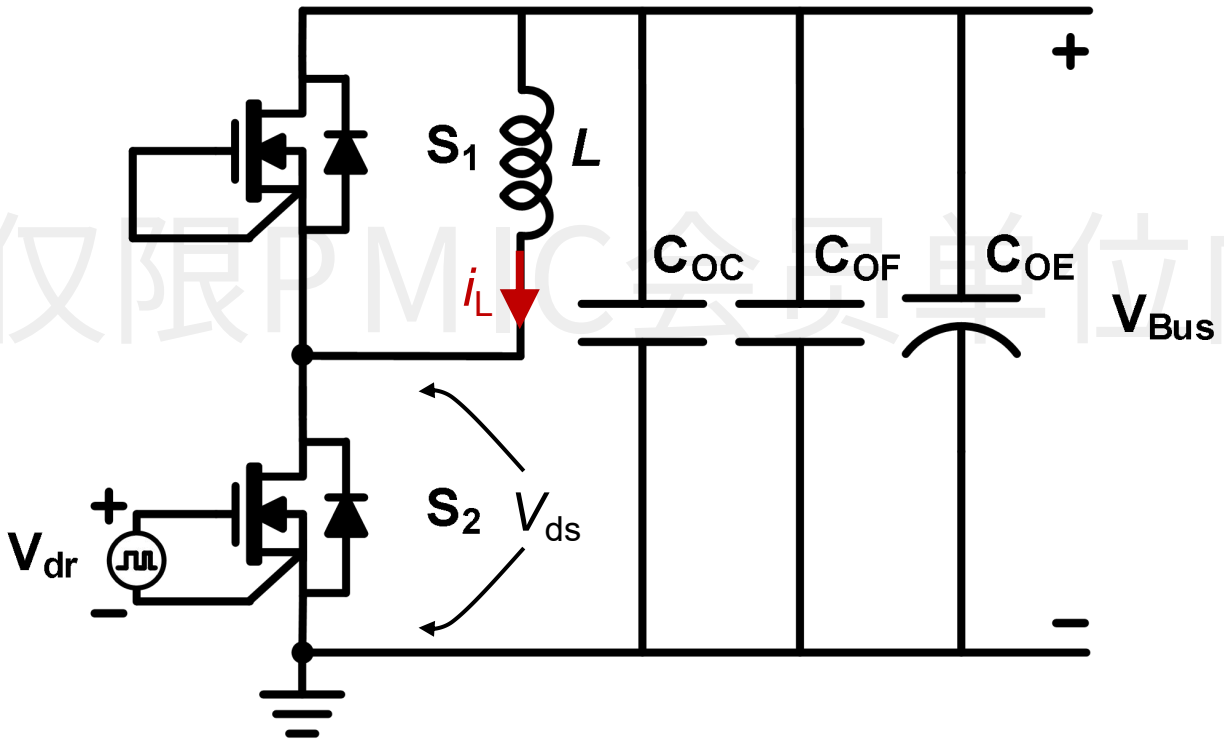
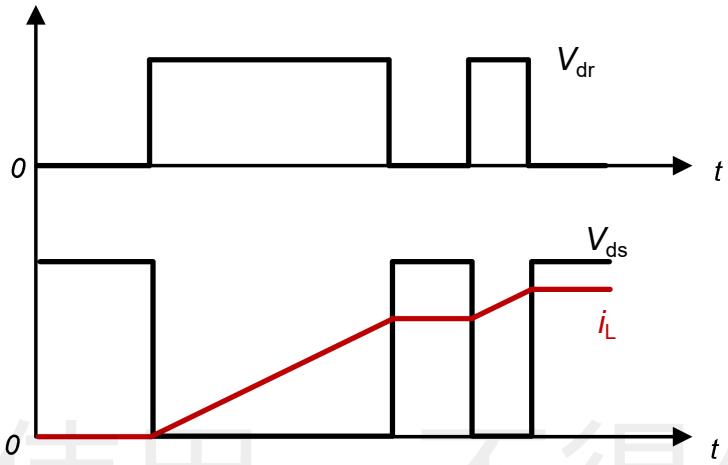
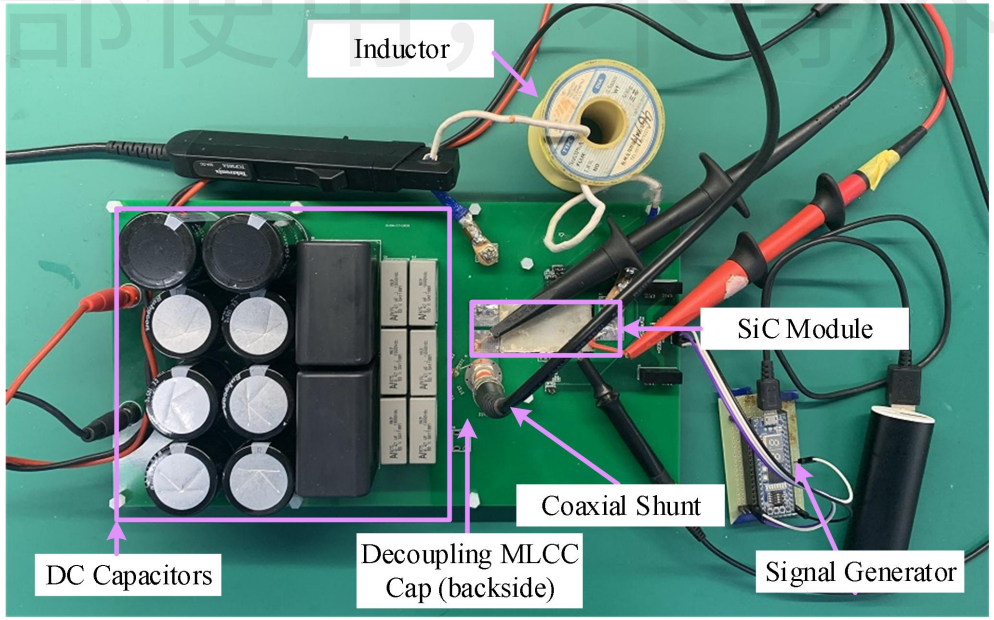
Double Pulse Test (DPT)

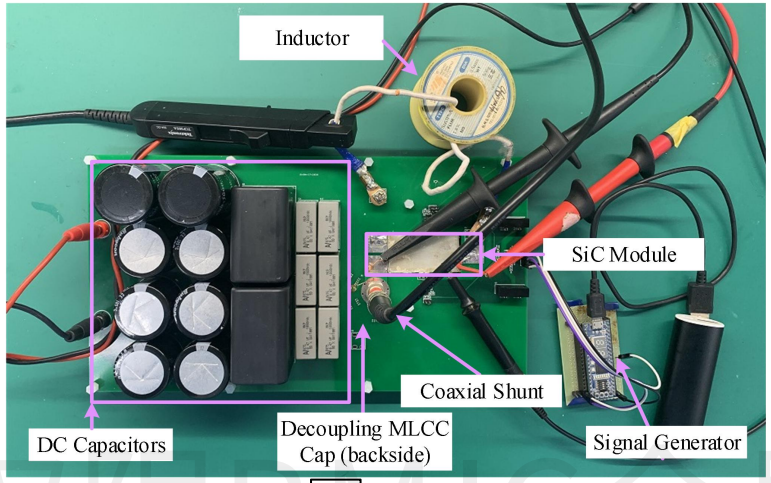
Test Condition: 400V/200A L:46μH V_{dr}:0~15V $R_{g(on)}$=$R_{g(off)}$:5.1Ω



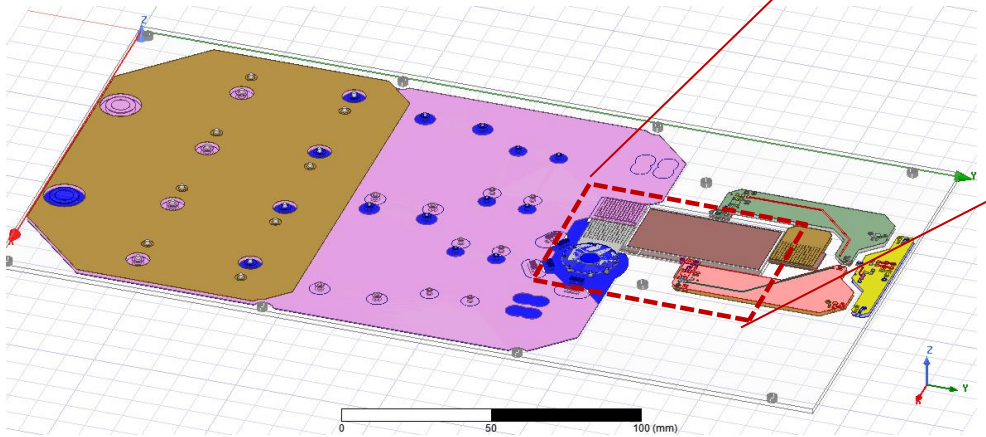


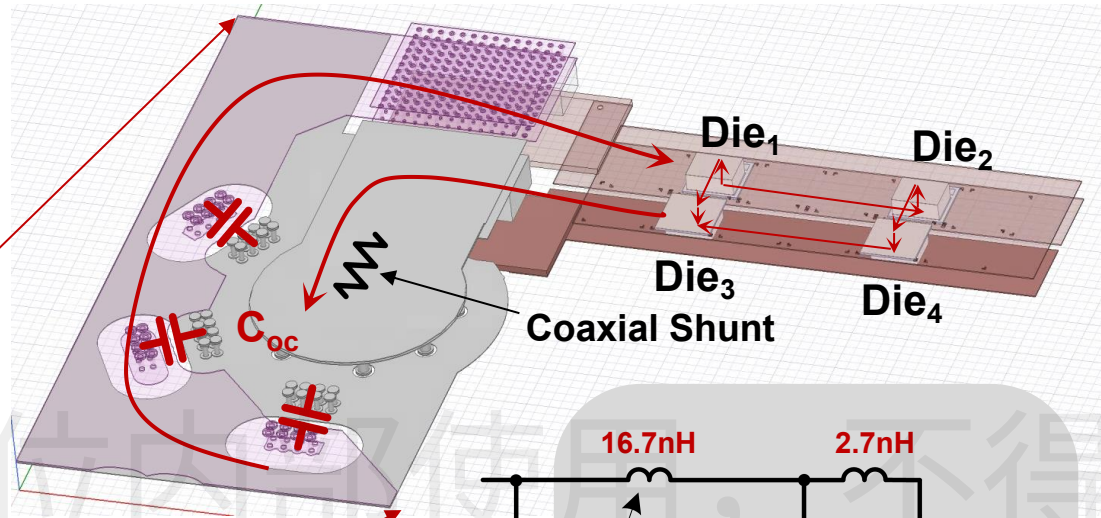


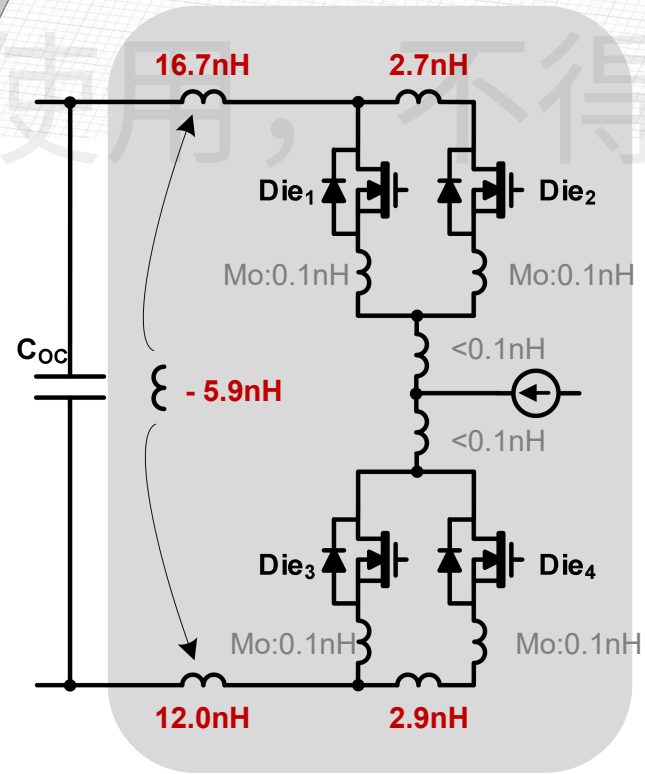
Parasitic Inductances Extraction



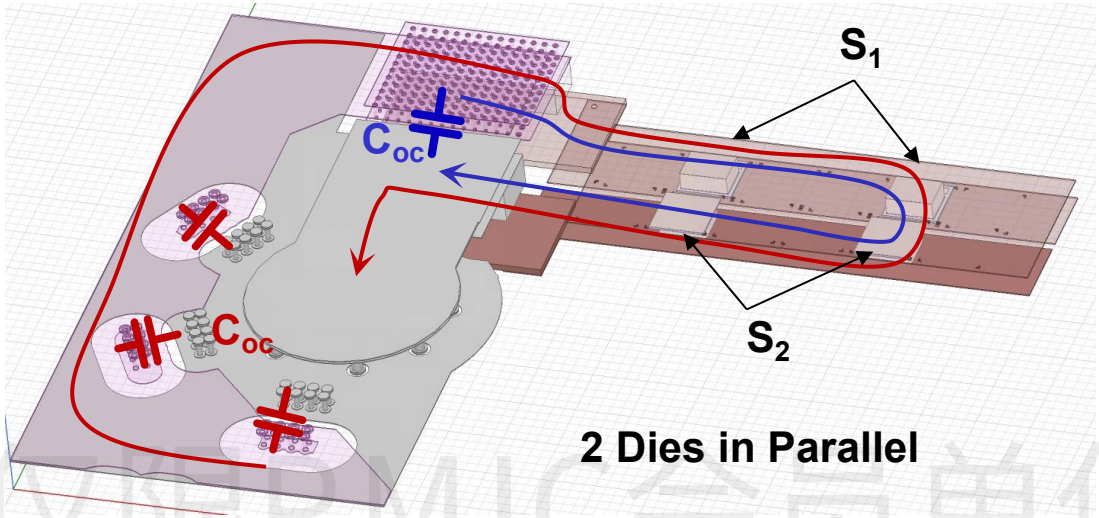
Ansys Q3D







Parasitic Inductances Extraction

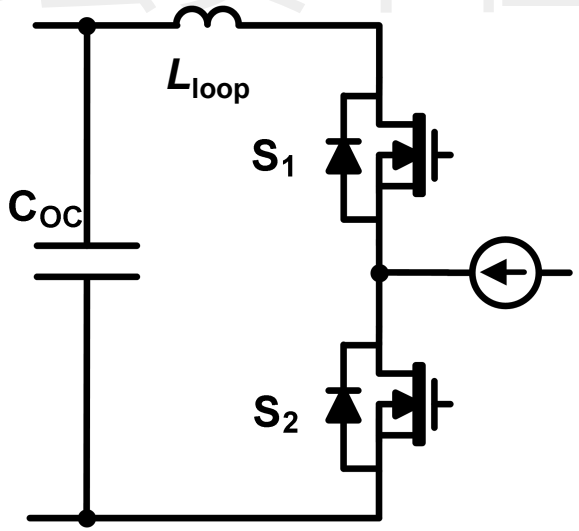


2 Dies in Parallel

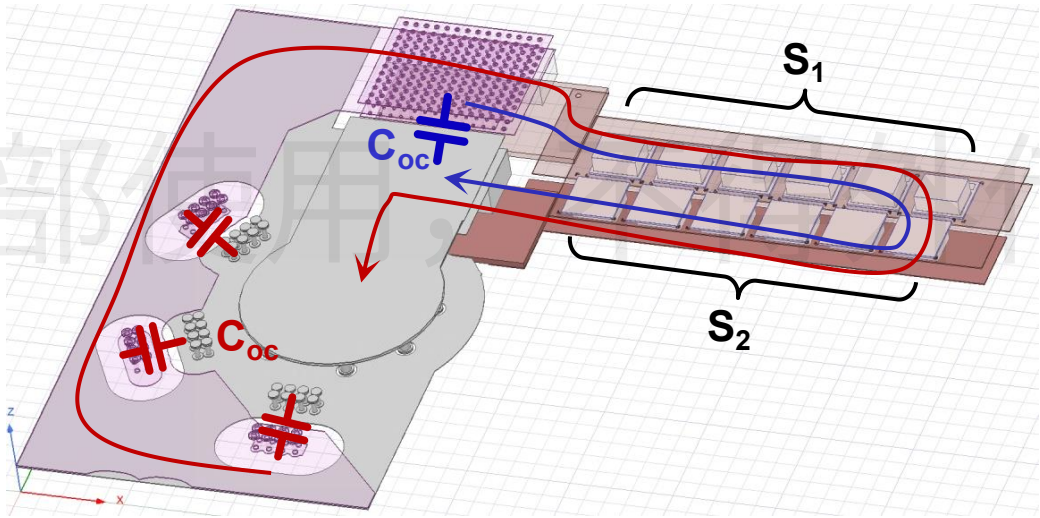
Simplified Model

L_{loop}=18.5nH

L_{loop}= 8.5nH



6 Dies in Parallel



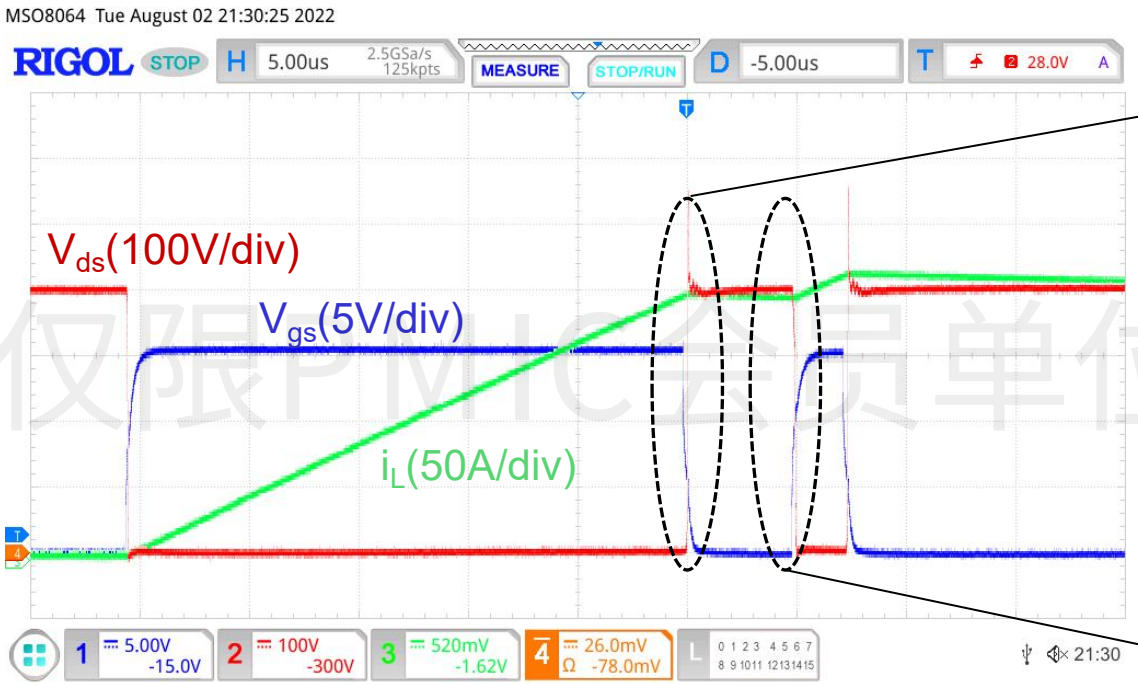
L_{loop}= 16.8nH

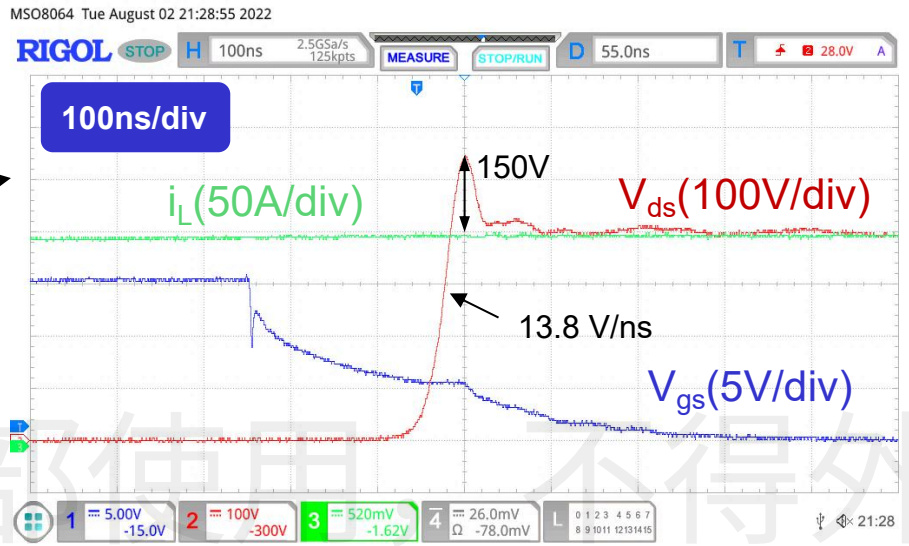
L_{loop}= 6.8nH

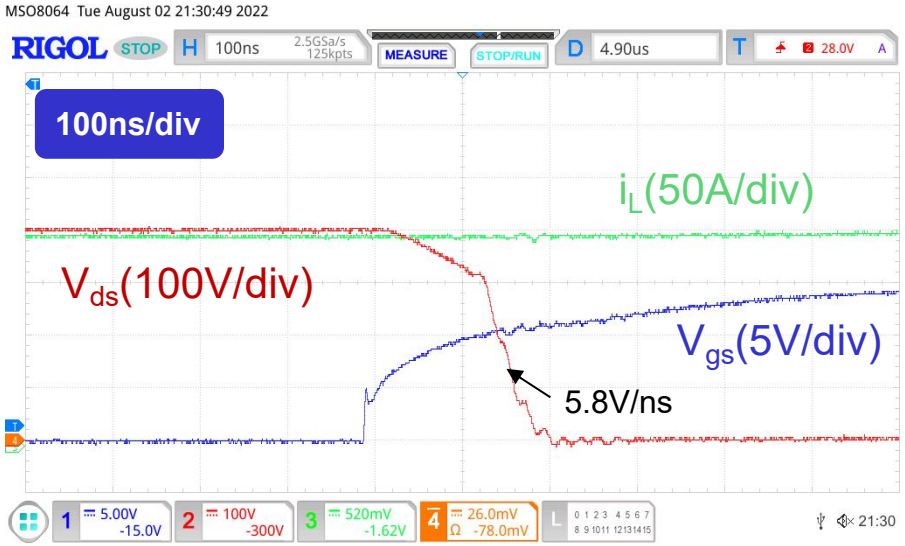
Switching Waveforms (V_{gs} & V_{ds}) of DPT

Power Management Innovation Consortium

Test Condition: 400V/200A L:46μH V_{dr}:0~15V $R_{g(on)}$=$R_{g(off)}$:5.1Ω



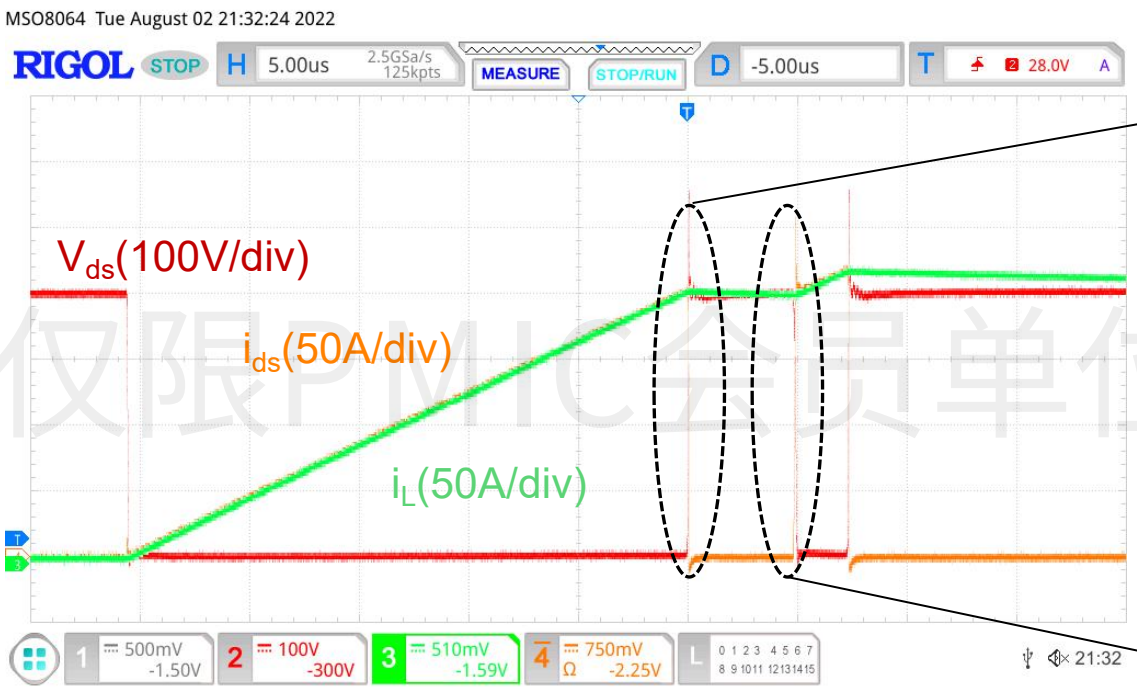


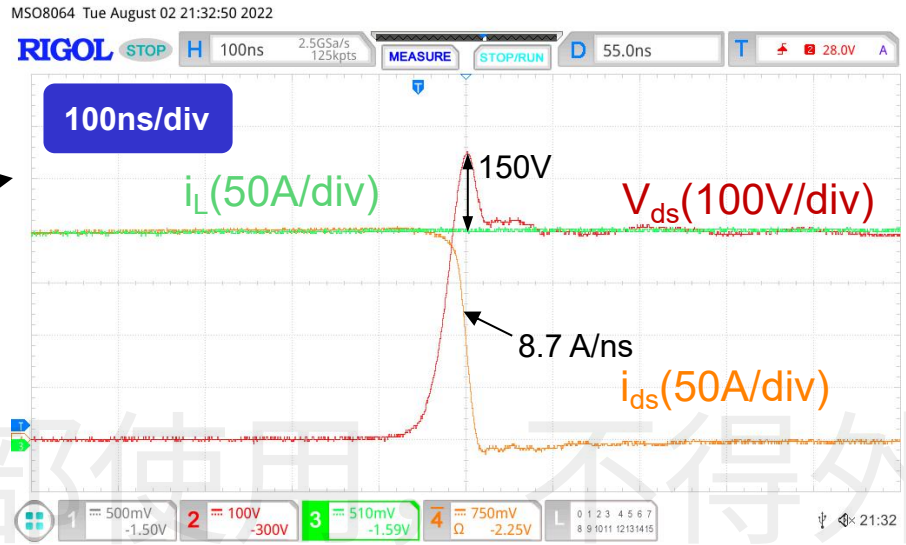


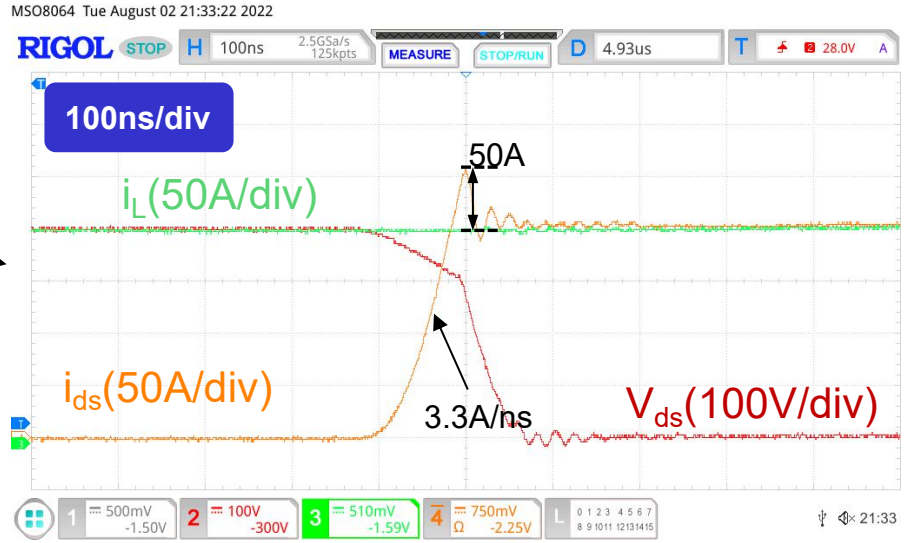
Switching Waveforms (V_{ds} & i_{ds}) of DPT

Power Management Innovation Consortium

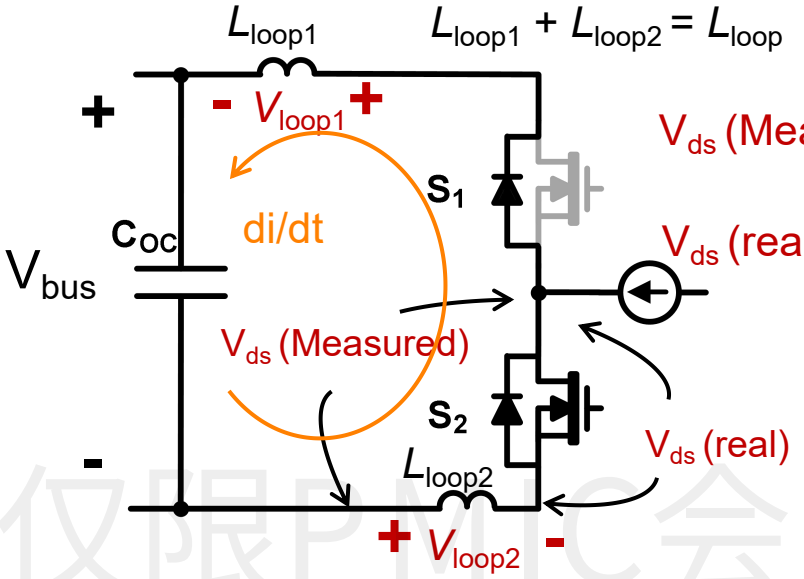
Test Condition: 400V/200A L:46μH V_{dr}:0~15V $R_{g(on)}$=$R_{g(off)}$:5.1Ω







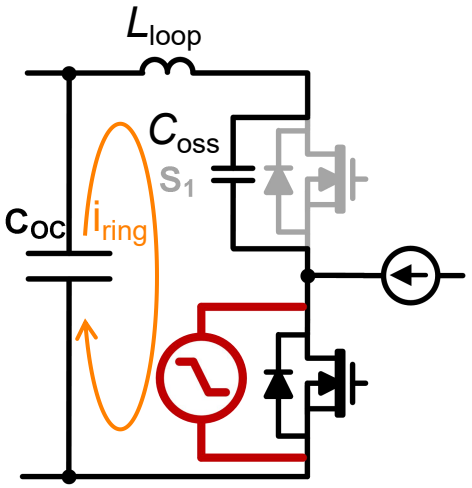
Analysis of Voltage Overshoot and Current Ringing



V_{ds} (Measured) = $\mathbf{V_{bus}}$ + V_{loop1}(150V)

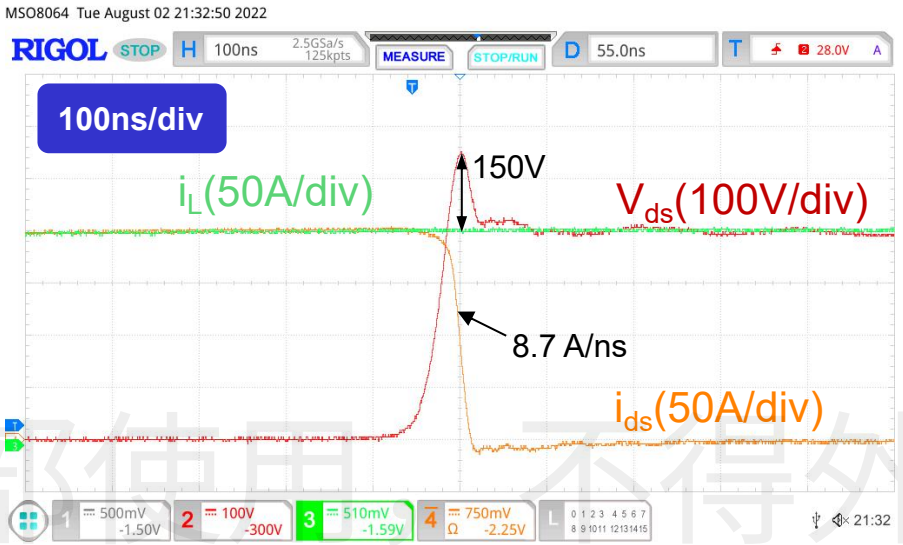
V_{ds} (real) = $\mathbf{V_{bus}}$ + L_{loop}*(di/dt) (**161V**)

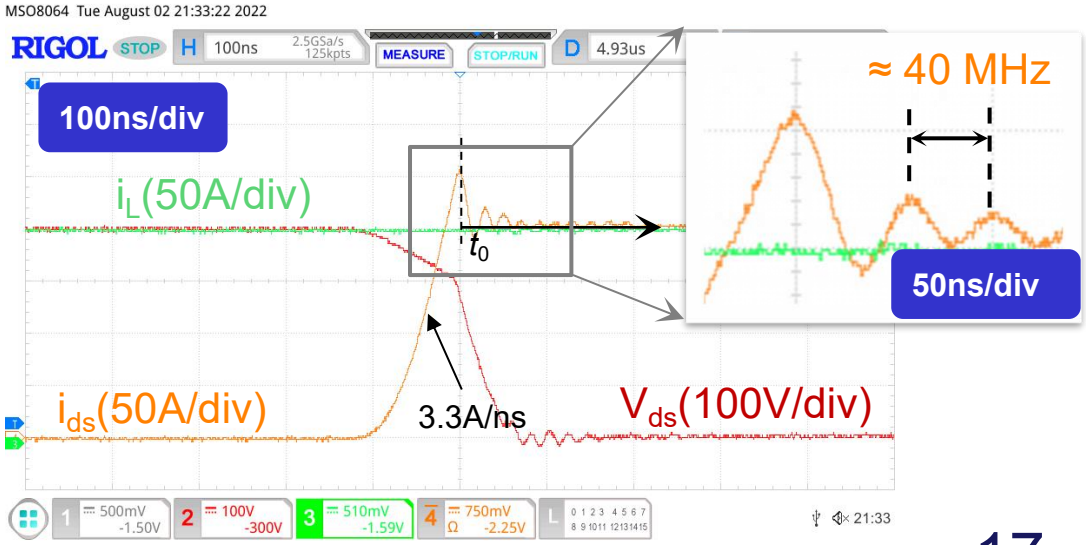
L_{loop} ↓



L_{loop} = 18.5nH C_{oss} ≈ 484pF*2 @ 200V

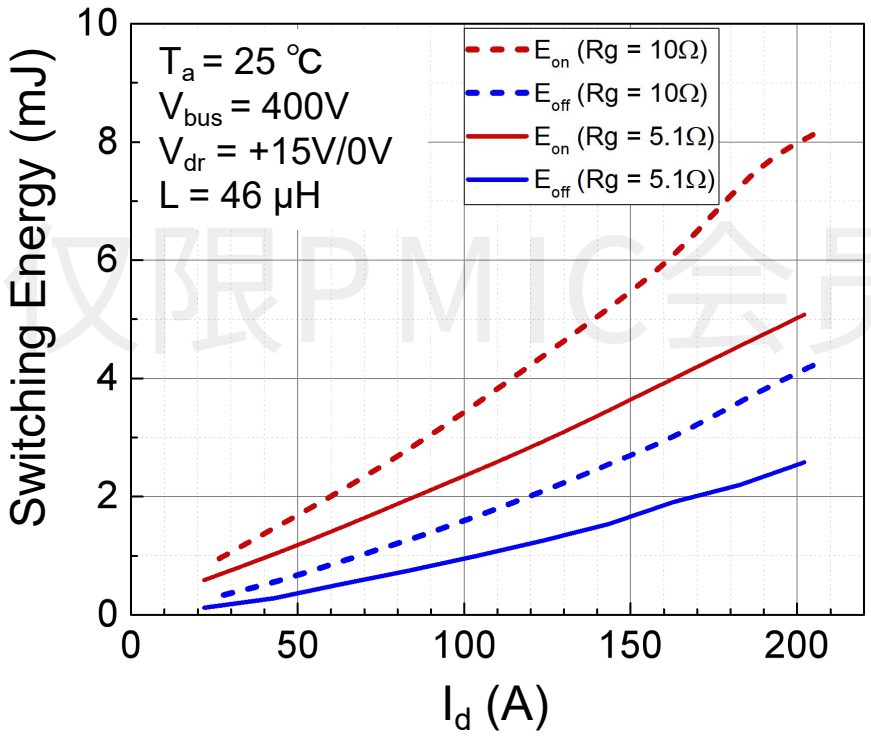
$$\frac{1}{2\cdot\pi\sqrt{L_{loop}\cdot C_{oss}}} \approx 38\ \text{MHz}$$



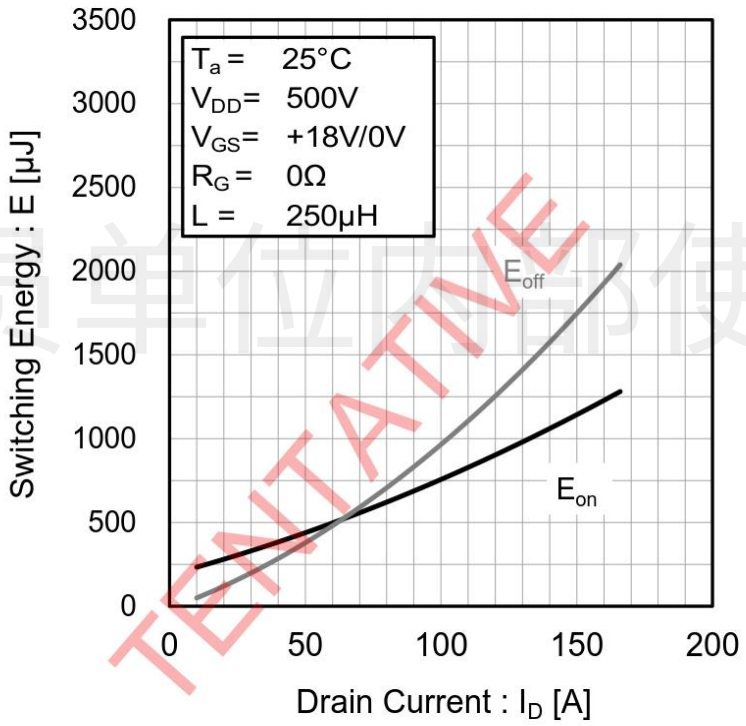


Switching Energy

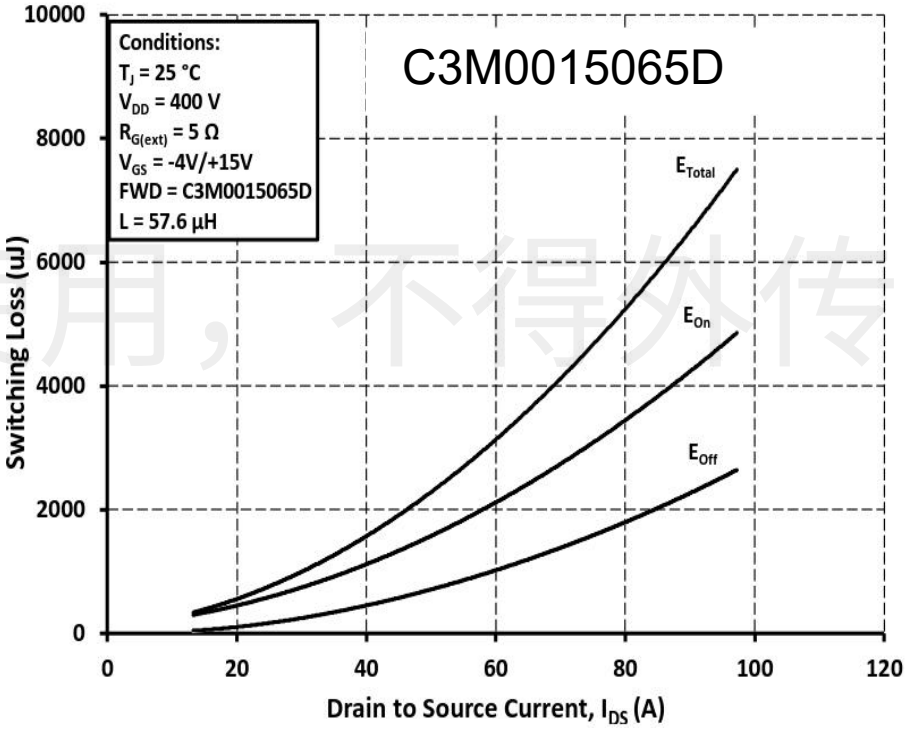
Measured



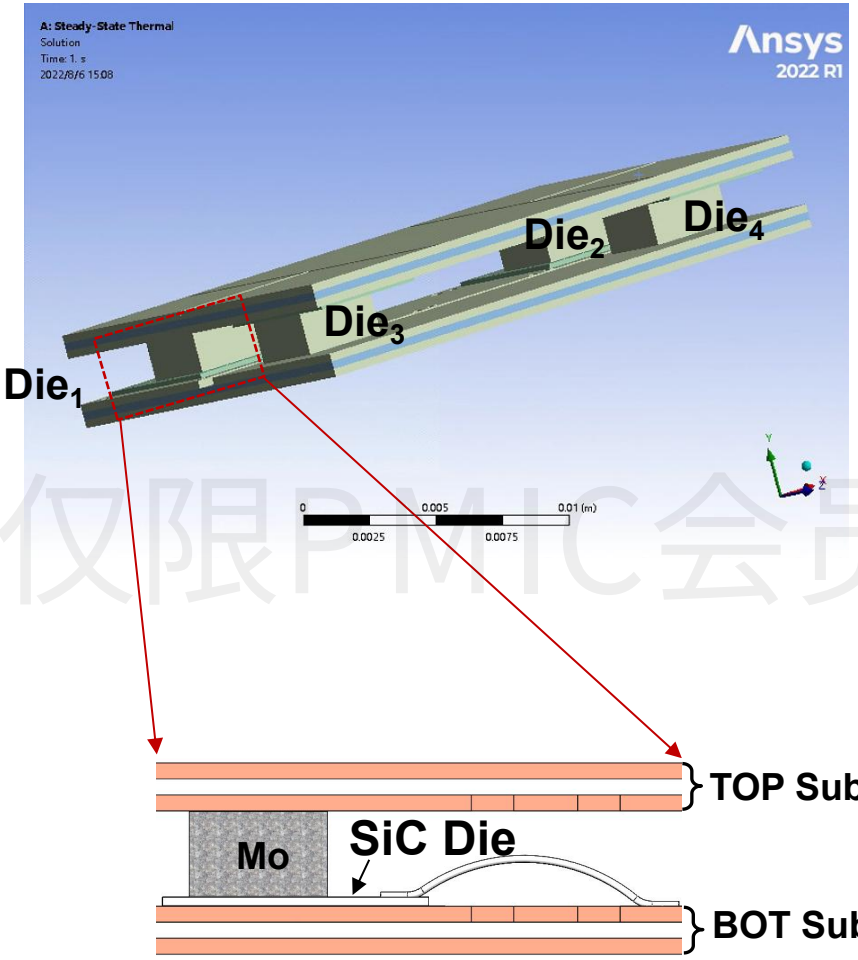
Single Die from datasheet

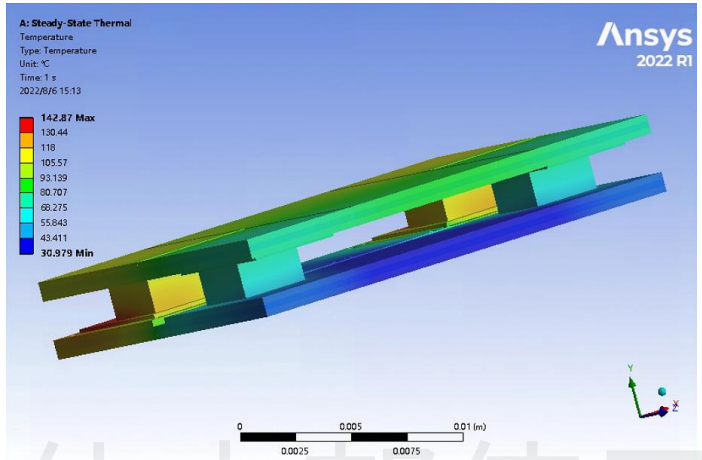


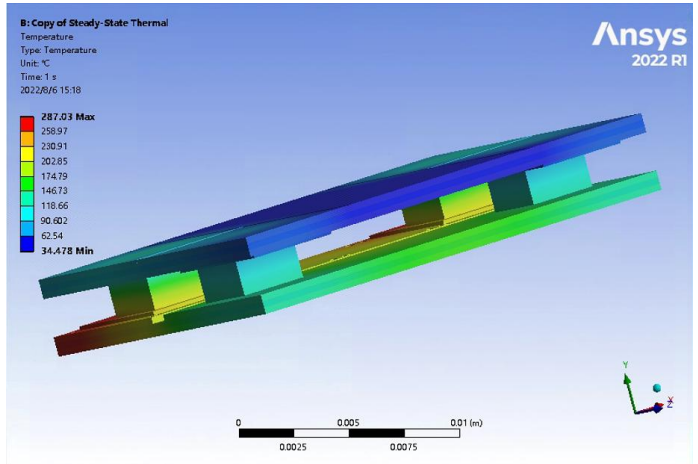
Die from another Manufacture



Thermal Resistance Evaluation by Simulation







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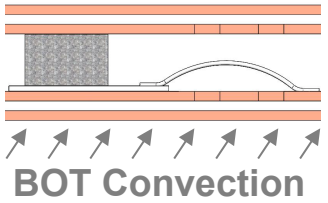
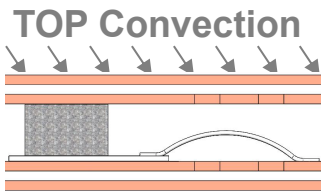


Power (Die_1+Die_2) : 300W

Die 5×5 mm²: 127℃ (Average)

Bottom 6.6×6.9 mm² : 109℃ (Average)

$R_{JC\_Die\_side}$ = 0.06 K/W



Power (Die_1+Die_2) : 300W

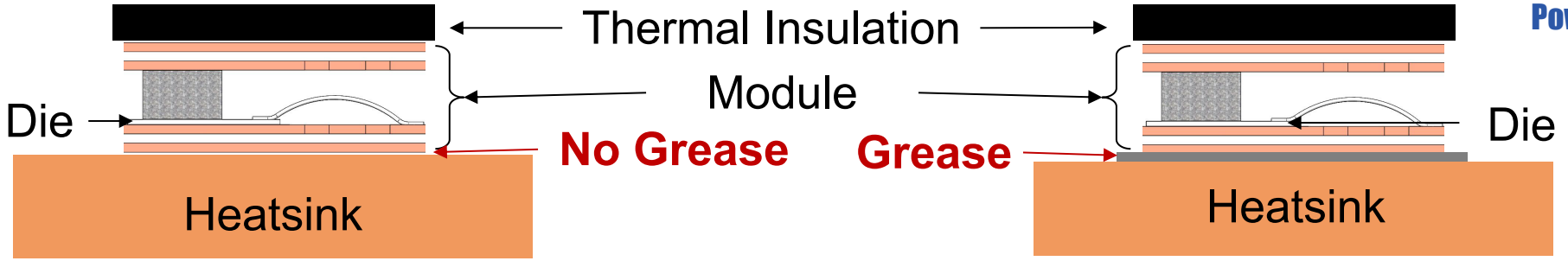
Die 5×5 mm²: 368℃ (Average)

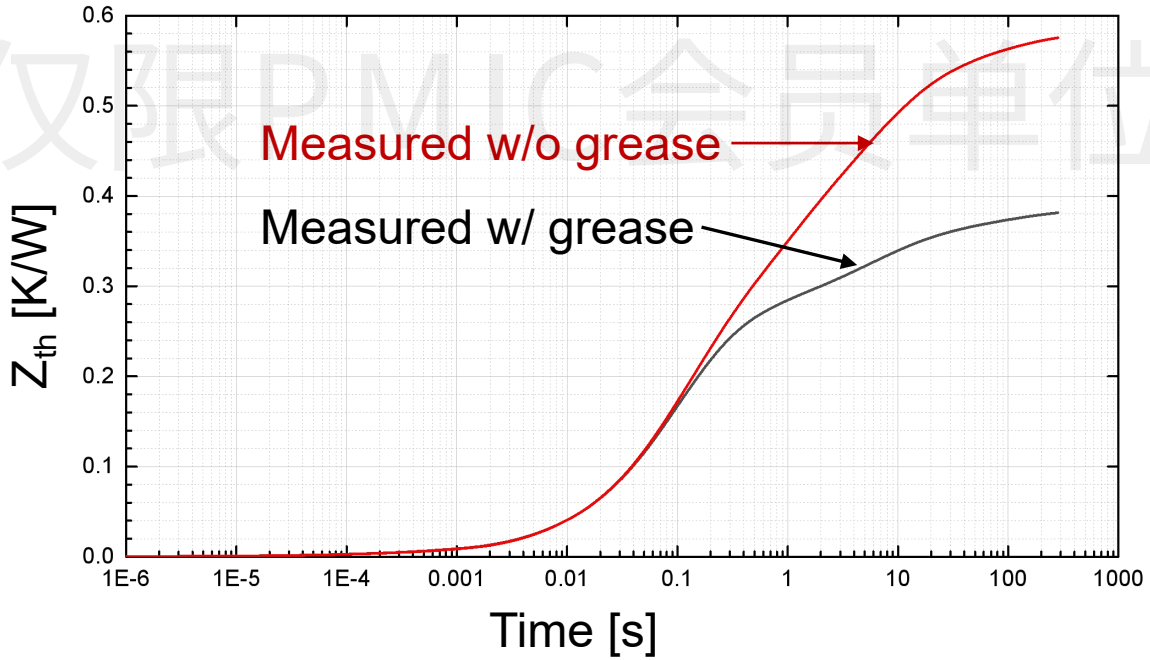
Top 6.6×6.9 mm² : 144℃ (Average)

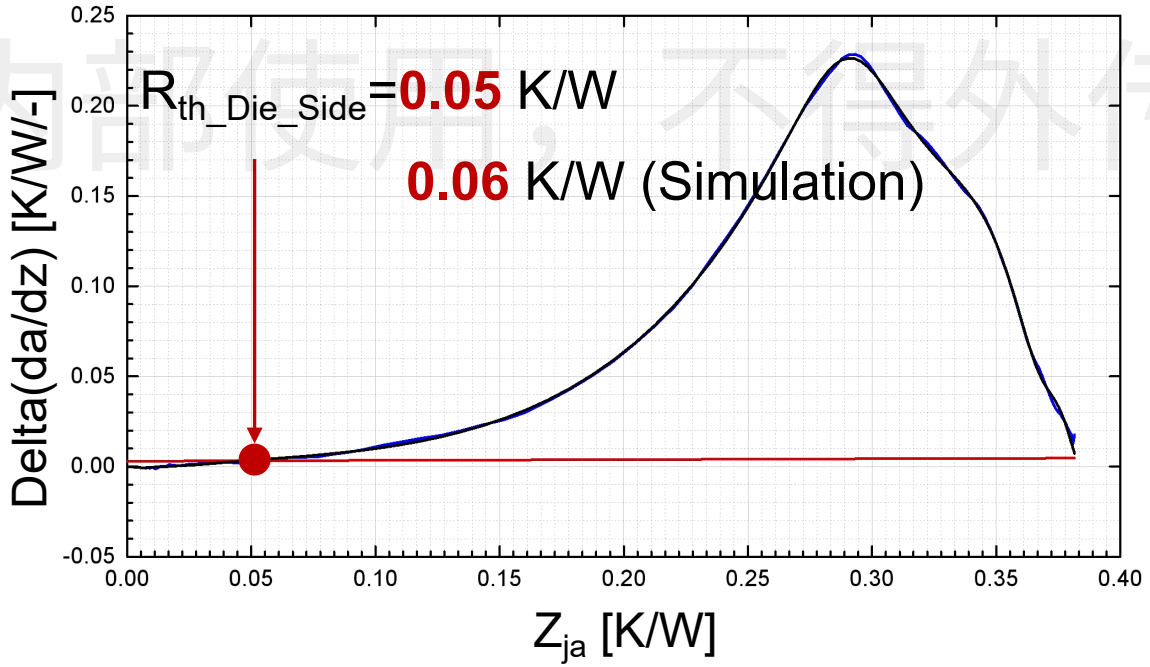
$R_{JC\_Mo\_side}$ = 0.52 K/W

R_{Mo} = 0.35 K/W

Transient Dual Interface Measurement of Die-side

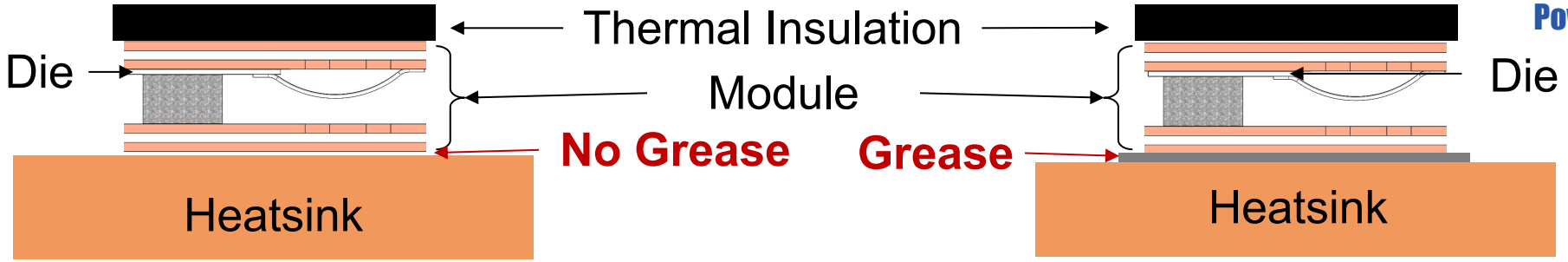


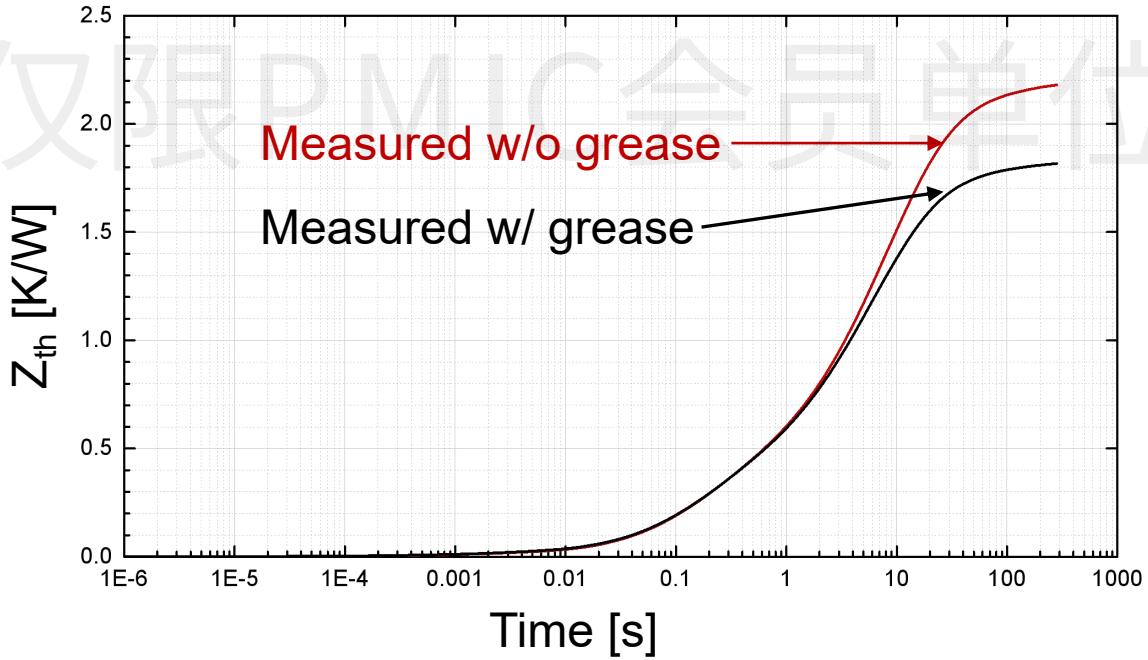


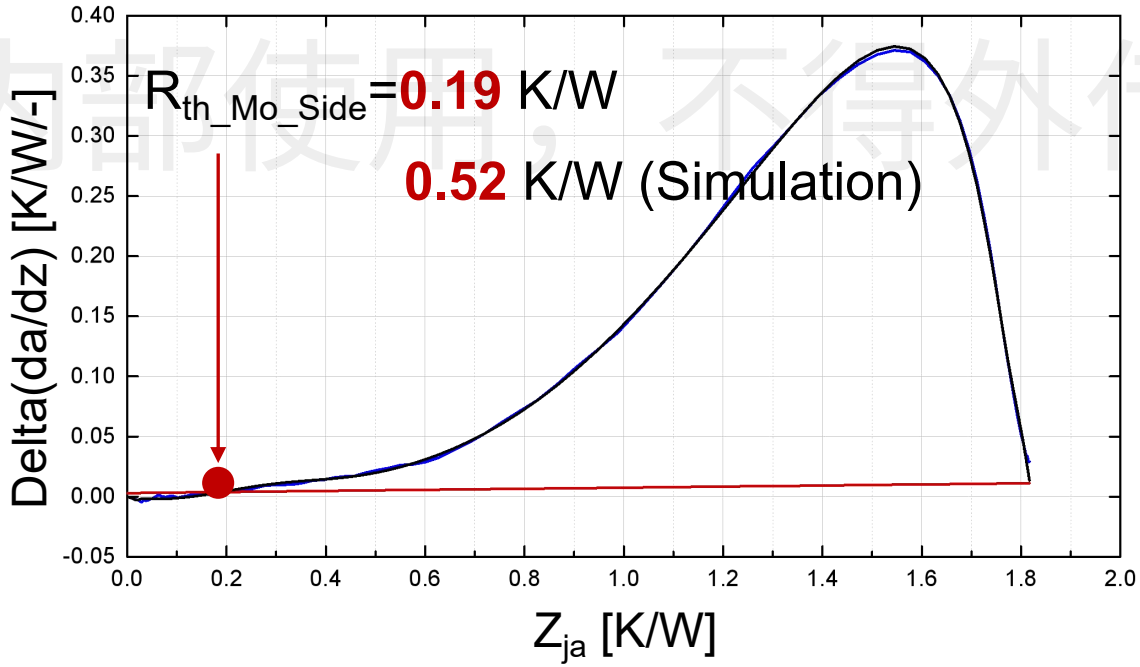


"Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction-to-Case of Semiconductor Devices with Heat
Flow Through a Single Path ." JESD51-14, Nov. 2010

Transient Dual Interface Measurement of Mo-side

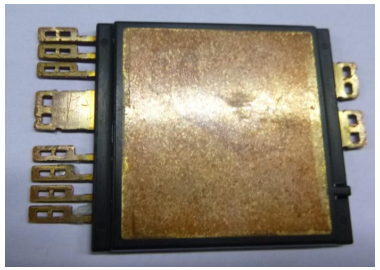






"Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction-to-Case of Semiconductor Devices with Heat
Flow Through a Single Path ." JESD51-14, Nov. 2010

Thermal Resistance Comparison among Different Modules

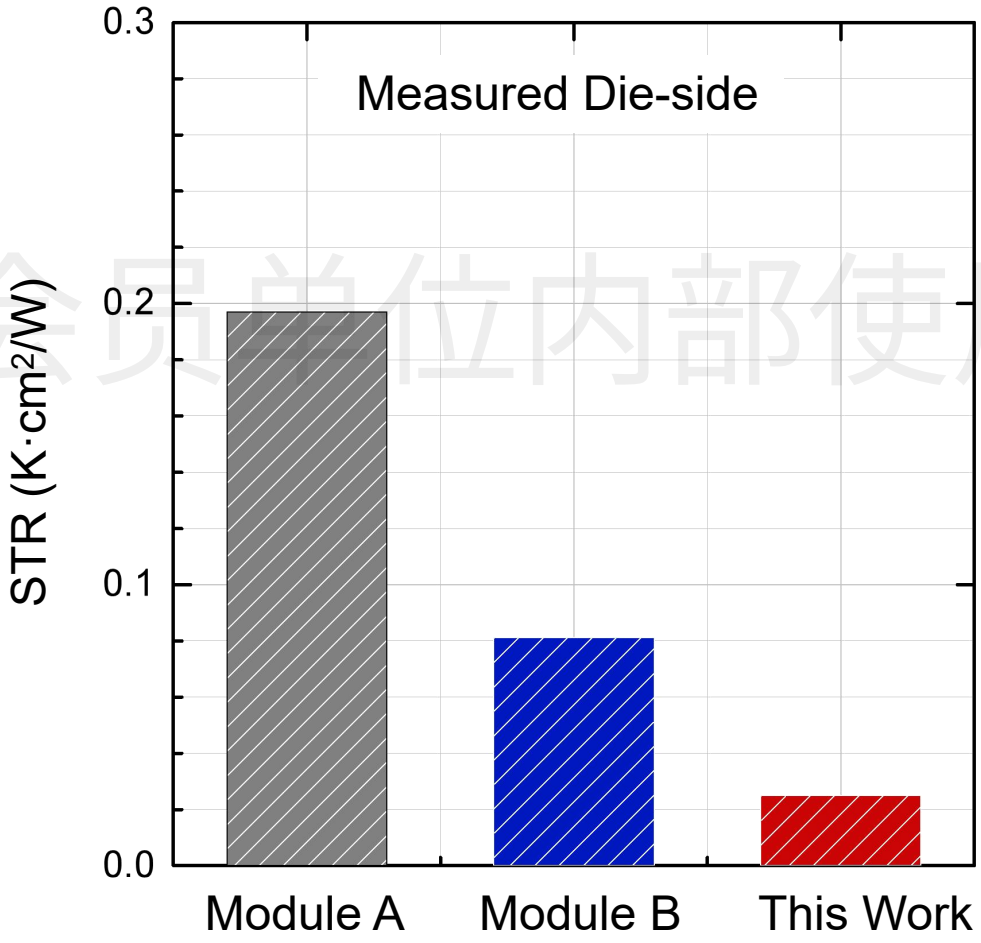


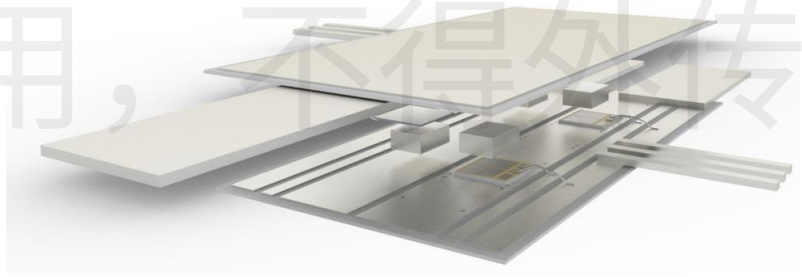
Module A (SSC)

Module B (DSC)

STR = Thermal Resistance * Die Area

(**S**pecific **T**hermal **R**esistance)





This work (DSC)

Transient Thermal Impedance of the Module

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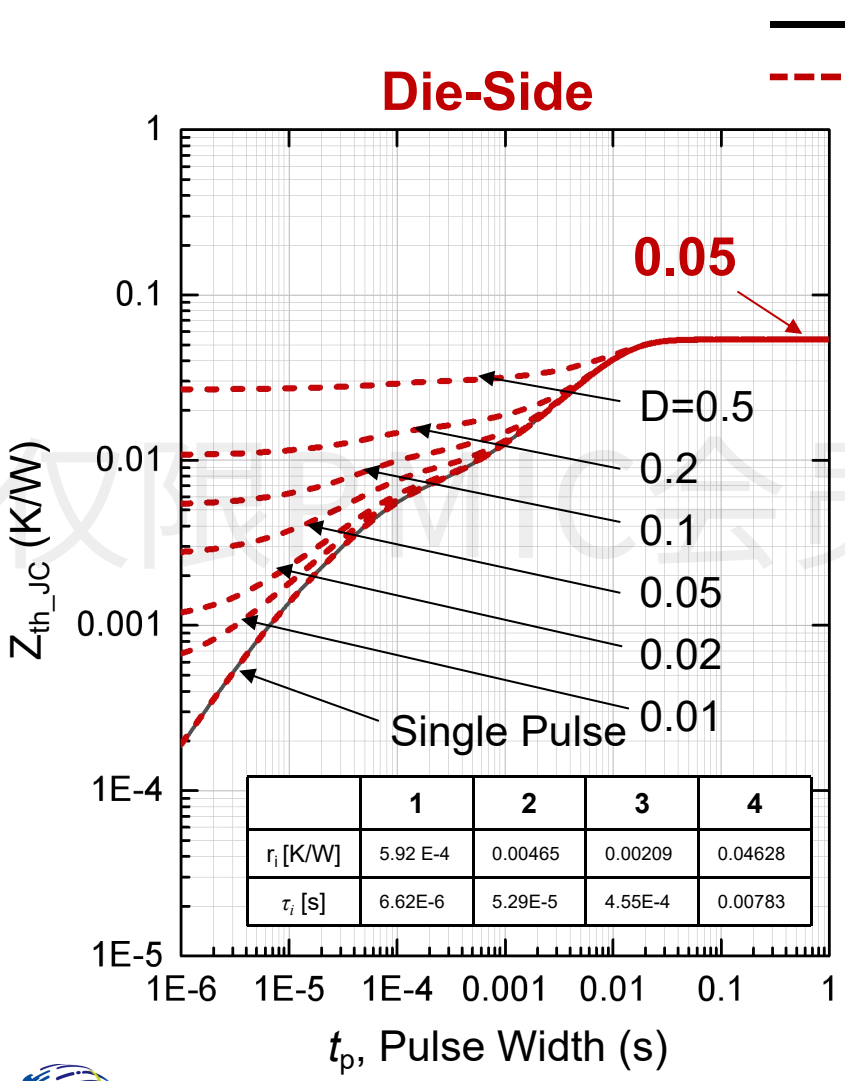
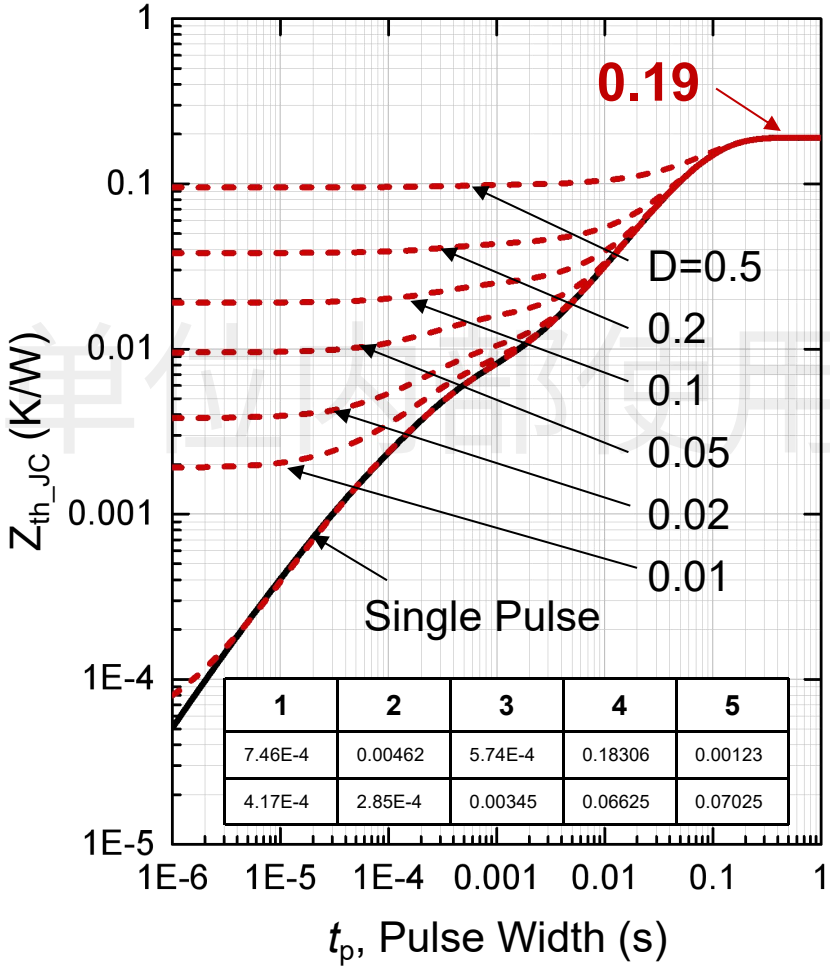
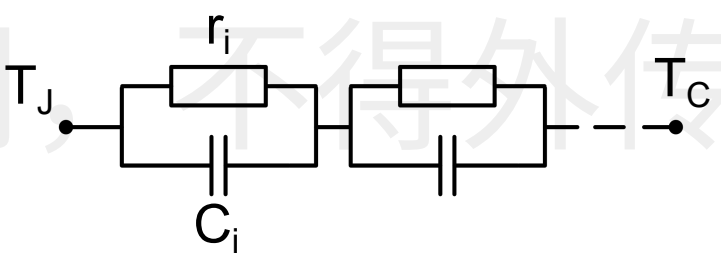


	1	2	3	4
r_i [K/W]	5.92 E-4	0.00465	0.00209	0.04628
τ_i [s]	6.62E-6	5.29E-5	4.55E-4	0.00783



1	2	3	4	5
7.46E-4	0.00462	5.74E-4	0.18306	0.00123
4.17E-4	2.85E-4	0.00345	0.06625	0.07025

Foster Model



$\tau_i = r_i \cdot C_i$

浙江大学 杭州国际科创中心
ZJU-Hangzhou Global Scientific and Technological Innovation Center

Conclusions & Future Works

结论：

- 基于银浆的薄膜转移工艺适合小批量开发
- 双面烧结工艺可靠、热阻低
- 大功率模块开关速度快，对寄生参数敏感

未来工作：

- 模块布局优化设计、散热器集成封装
- 可靠性测试分析、逆变器搭建等

关于SiC测试标准的一些思考

- 模块杂散电感的定义及测量方法（判断标准是什么）
- 双面模块的热阻测试标准

请各位专家批评指正