Active Dynamic Current Balancing Method for Parallel-Connected SiC MOSFETs in EV Applications

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Aug. 29, 2024

For PCIM Asia 2024, Shenzhen

Contents

1. Background

- **SiC MOSFET in EV applications:** replace IGBT for higher efficiency

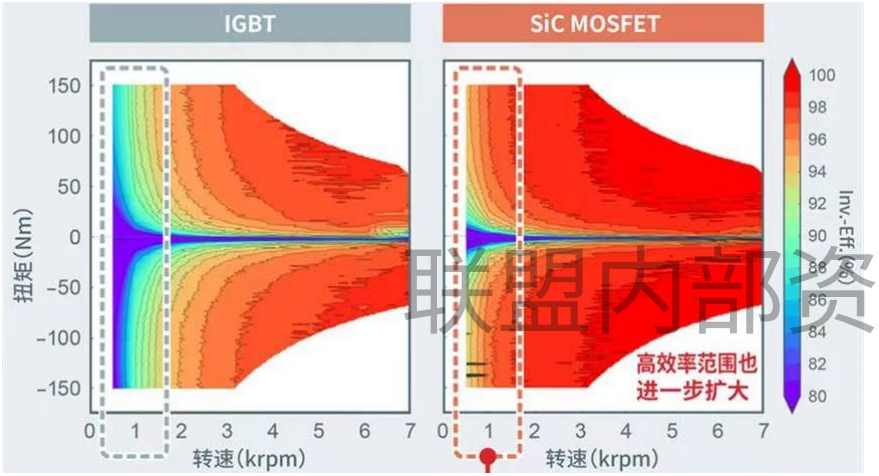
  - Limited by yield and cost, parallel operation of SiC MOSFETs is necessary

    1200V/13mΩ/153A (Cree, TO-247-4), **1200V/13mΩ/160A** (Cree, Bare Die)

EV

Traction Inv.

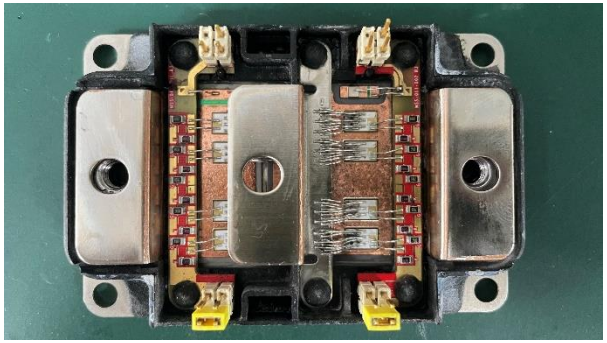
OBC/Charger

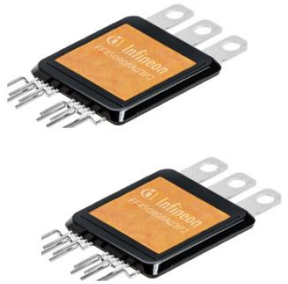


~5% Energy Efficiency Improvement

1. Background

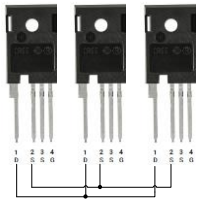
- **Parallel operation of SiC devices:**

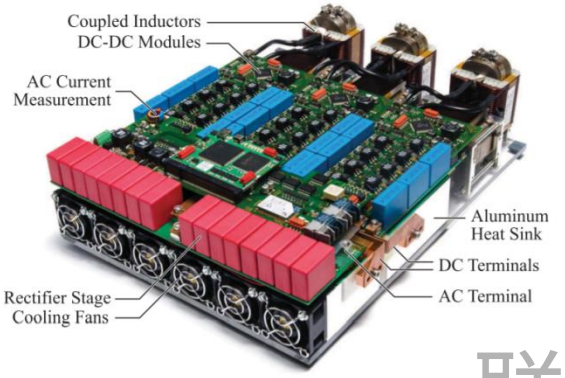


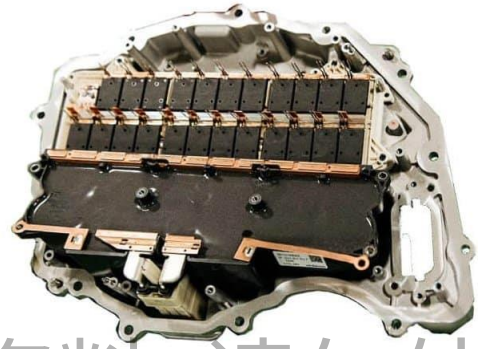


Module Parallel

Cree Wolfspeed 1.2kV/400A XM3 half bridge SiC MOSFET module: **4 paralleled dies**







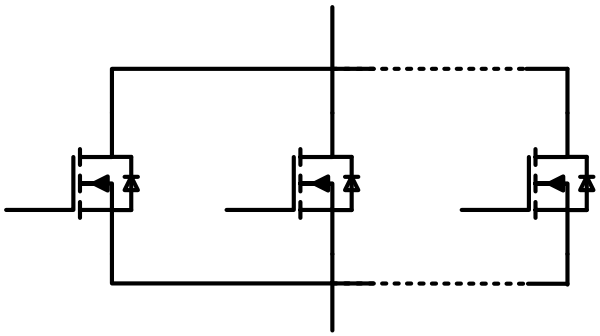
IPT system of ETH: **3 paralleled discrete devices** in half bridge topology[1]

Tesla Model 3: **4 paralleled devices** in 6 half bridges[2]

[1] R. Bosshard and J. W. Kolar, "All-SiC 9.5 kW/dm3 On-Board Power Electronics for 50 kW/85 kHz Automotive IPT System," in IEEE JESTPE, March 2017.
[2] About the SiC MOSFETs Modules in Tesla Model 3, 2021. Available: https://www.pntpower.com/tesla-model3-powered-by-st-microelectronics-sic-mosfets/

1. Background

Device lifetime



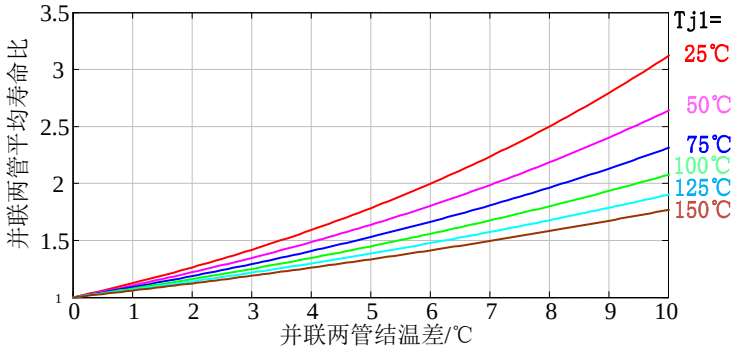
Current imbalance

↓

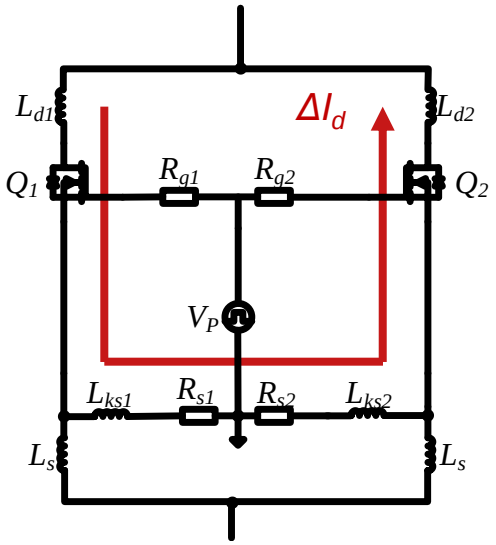
Uneven thermal distribution

↓

Mismatched device lifetime



Reliability



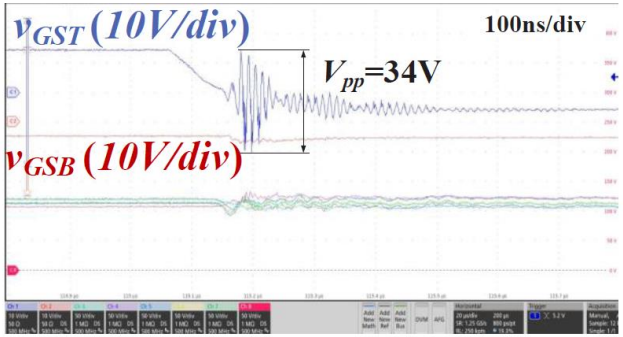
Current imbalance

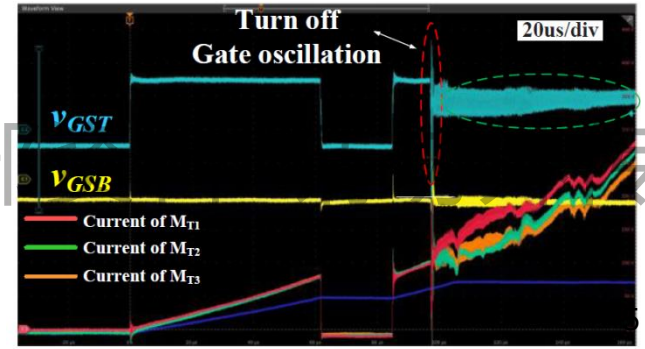
↓

Circulating current

↓

Gate oscillation





Y. Zhu , et al, "Influence of Paralleled SiC MOSFET on Turn-off Gate Voltage Oscillation," in Proc. IEEE ECCE., 2020

1. Background

■ Factors affecting current balance:

device parameters, circuit parameters, gate driver, temperature .....

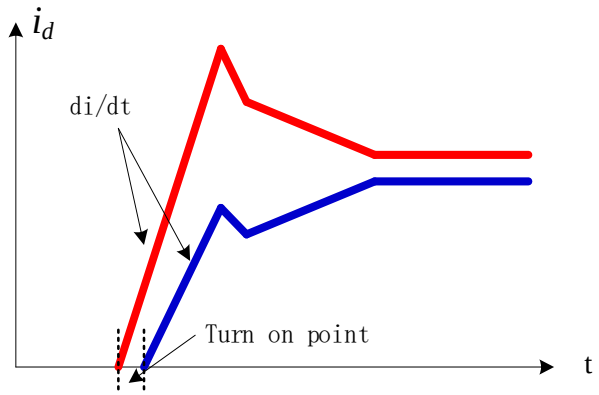
Type	Parameters	
Device parameters	R_{dson}	Static
	$R_{g(int)}$	**Dynamic**
	g_m	**Dynamic**
	V_{th}	**Dynamic**
	C_{gs}	**Dynamic**
Circuit parameters	L_d	**Both**
	L_s	**Both**
Gate Driver	$R_{g(ext)}$	**Dynamic**
	V_g	**Both**
Junction Temp.	T_j	**Both**

- Static current balancing is mostly related to stead state current
- Dynamic current balancing is more difficult for paralleled devices

1. Background

■ Devices Parameters tolerance:

key point for dynamic current balancing: turn on delay & di/dt



Dynamic Current imbalance mechanism

$$i_d = g_m \cdot (V_{gs} - V_{th}) = \beta \cdot (V_{gs} - V_{th})^2$$

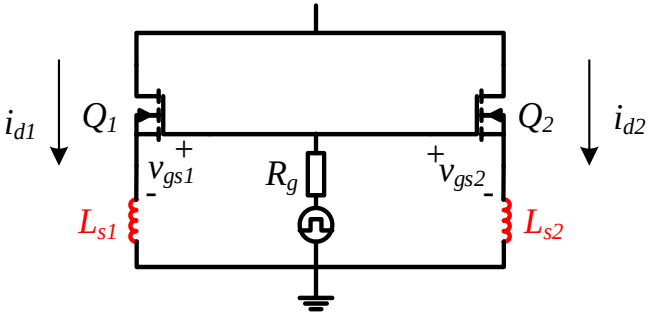
$$\Rightarrow \Delta i_d(\Delta V_{th}) = \frac{\partial i_d}{\partial V_{th}} \cdot \Delta V_{th} = -2\beta \cdot (V_{gs} - V_{th}) \cdot \Delta V_{th}$$

$$\Rightarrow \Delta i_d(\Delta g_m) = \frac{\partial i_d}{\partial g_m} \cdot \Delta g_m = (V_{gs} - V_{th}) \cdot \Delta g_m$$

- Vth & g_m: the larger the difference, the larger the current difference
- **Vth: turn on delay & di/dt**
- **g_m: di/dt only**
- Most device parameters tolerance affect both delay & di/dt
- Gate driver: usually has very small mismatch & tolerance

1. Background

- Circuit parasitic parameters: L_s、L_d
  - Source inductance Ls:

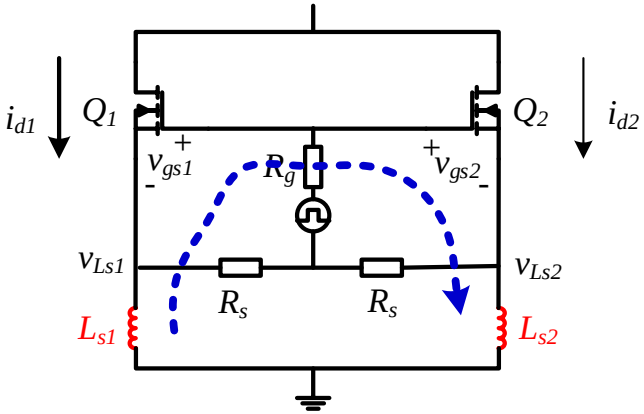


无Kelvin源极

$$v_{gs1} - v_{gs2} = v_{Ls2} - v_{Ls1} = L_{s2}\frac{di_{d2}}{dt} - L_{s1}\frac{di_{d1}}{dt}$$

$$v_{gs1} < v_{gs2}$$

$$\frac{di_{d1}}{dt} > \frac{di_{d2}}{dt}$$



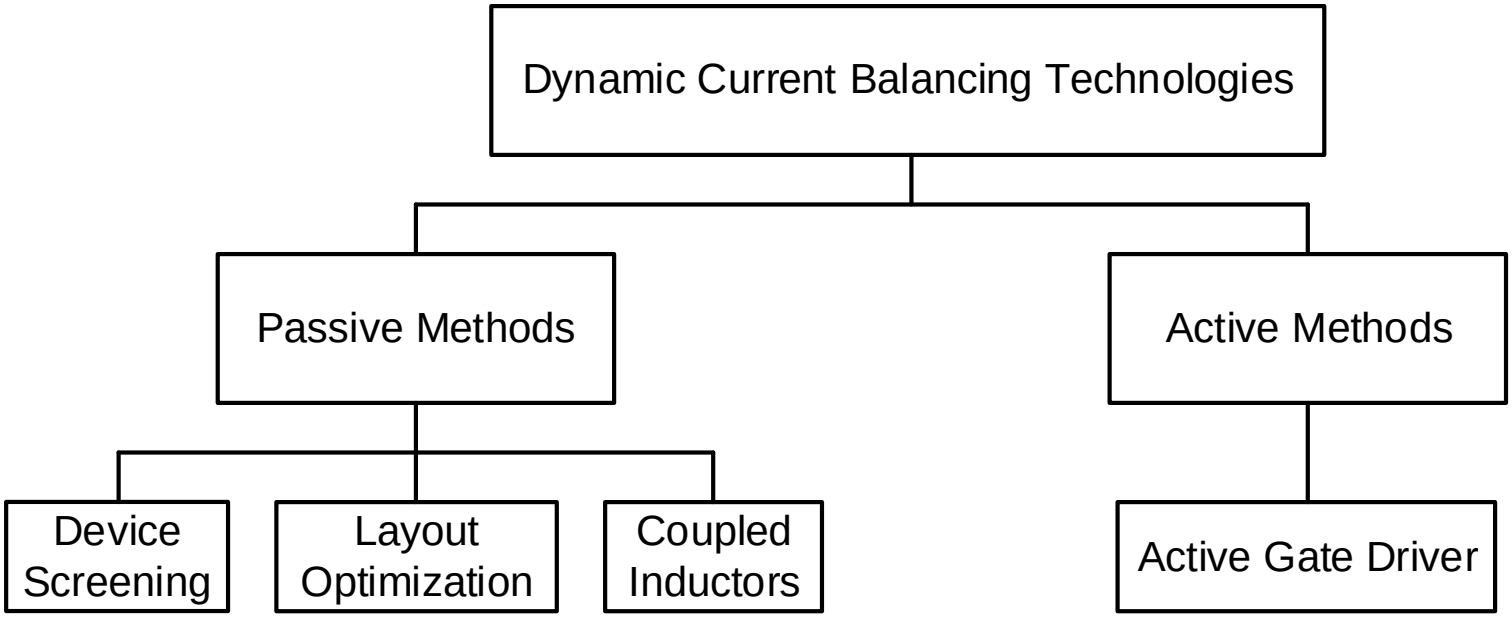
Kelvin Source

- Larger Ls difference – larger current imbalance (gate circulating current)
- The faster the switching speed, the greater the impact
- Drain inductance Ld has limited effect

Contents

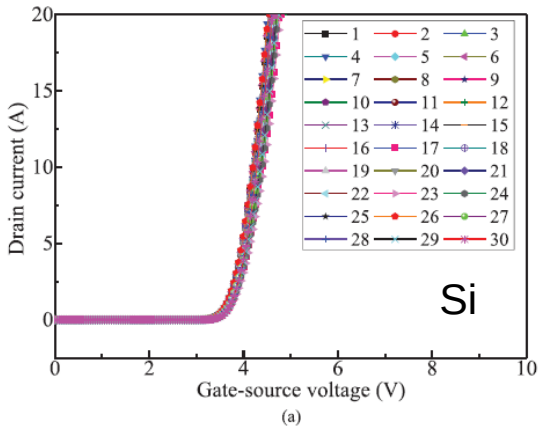
2. Challenges & Solutions

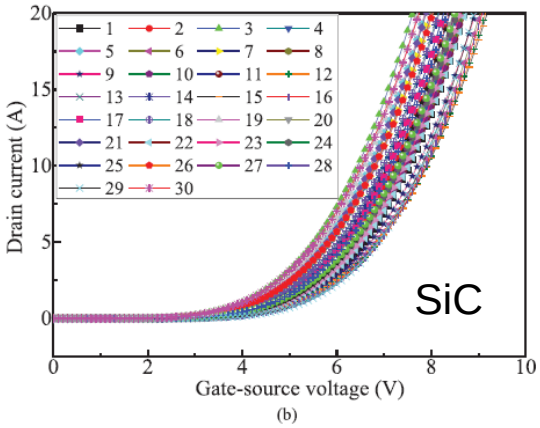
- **Existing Dynmaic Current Balancing Methods**



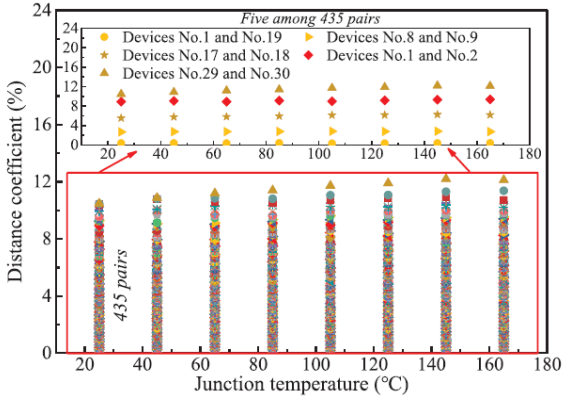
2. Challenges & Solutions

■ Device Screening: V_{th}, g_m (Transfer Curves) , time-related



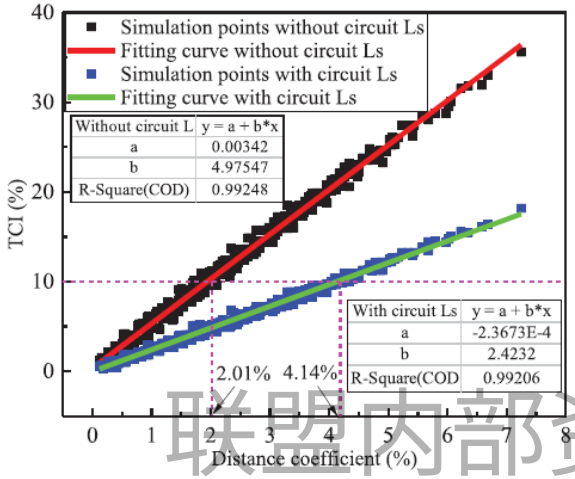


- Transfer curves of 30 devices
- SiC MOSFETs with larger dispersion



Transfer curves difference @ Tj

Differences almost not changed



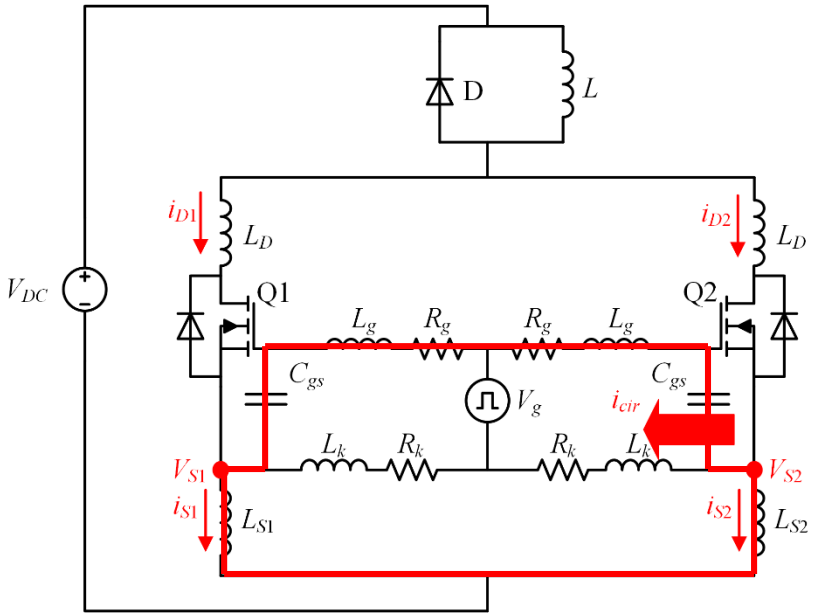
Relationship between differences of transfer curves and current imbalance

- Parameters vary with temperature but differences keep almost same
- Choose devices according to current sharing requirements
- Better current sharing with larger source inductances Ls

J. Ke, et al, "Chips Classification for Suppressing Transient Current Imbalance of Parallel-Connected Silicon Carbide MOSFETs," IEEE TPEL, Apr. 2020

2. Challenges & Solutions

■ **Influences of power loop parasitics: source inductances Ls**



If Ls1 and Ls2 are different, a circulating current flows through the gate loop (loop in the figure), and lead to gate voltage difference:

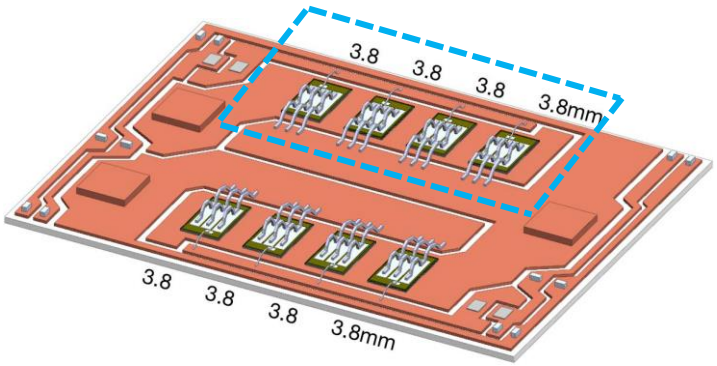
$$R_g C_{gs} \frac{d\Delta v_{gs}}{dt} + \Delta v_{gs} = L_{S2} \frac{di_{D2}}{dt} - L_{S1} \frac{di_{D1}}{dt} \qquad (\Delta v_{gs} = v_{gs1} - v_{gs2})$$

$$i_{Di} = K(v_{gsi} - V_{th})^2$$

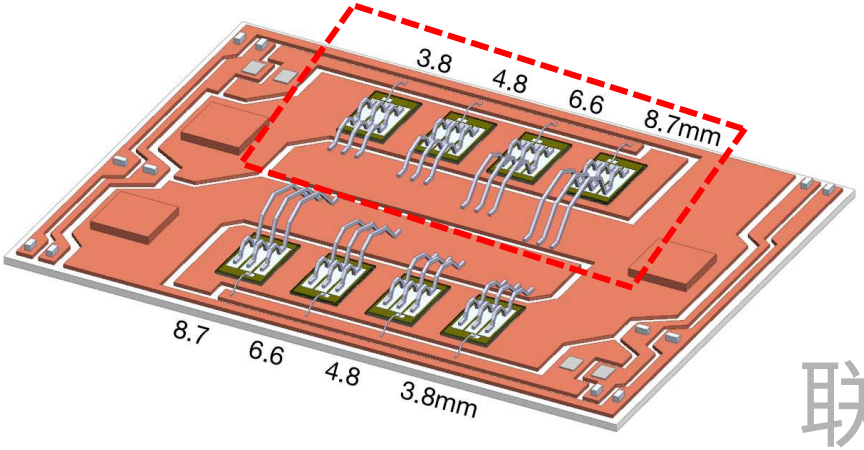
Different source potentials charge C_{gs}, and lead to **dynamic current imbalance.**

2. Challenges & Solutions

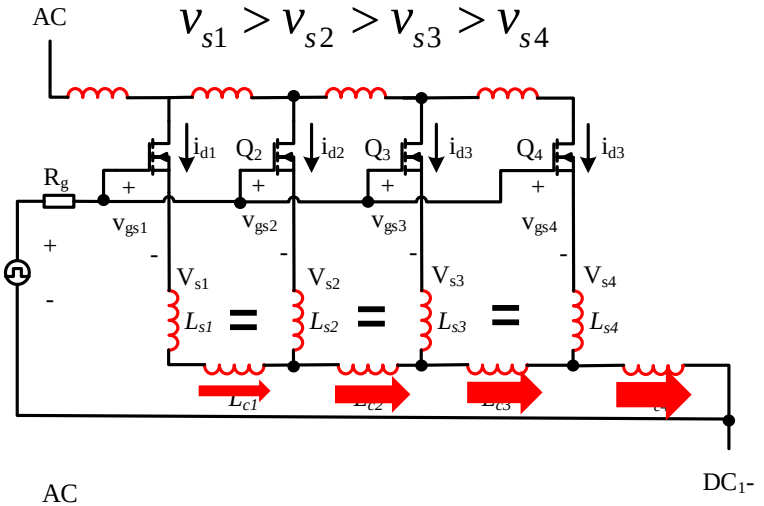
■ **Layout optimization of power module: symmetry**

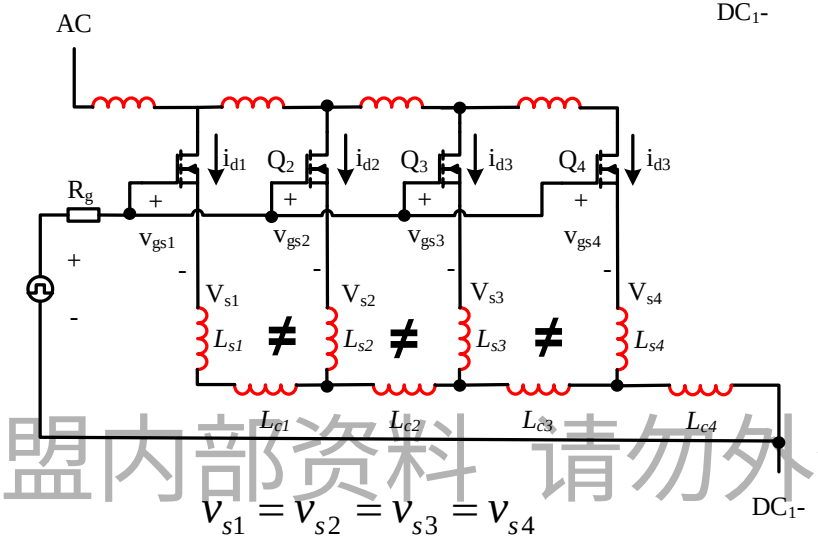


$$L_{s1} = L_{s2} = L_{s3} = L_{s4} = L_s$$



$$L_{s1} \neq L_{s2} \neq L_{s3} \neq L_{s4}$$



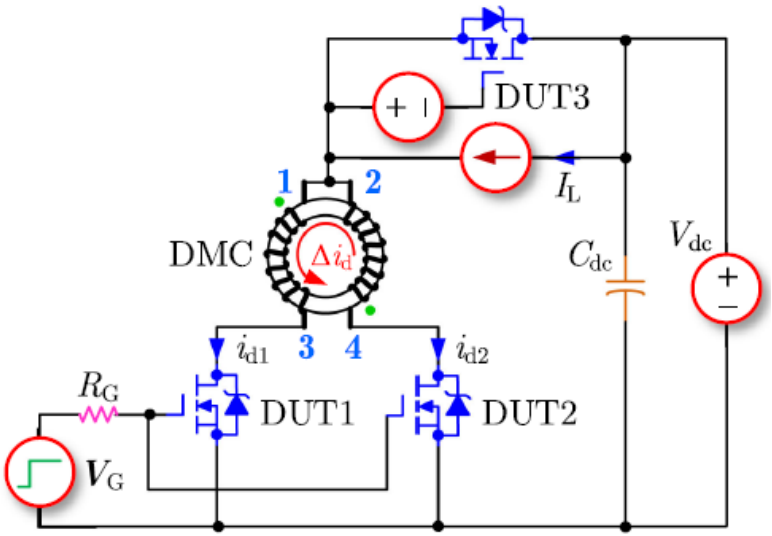


$$v_{s1} = v_{s2} = v_{s3} = v_{s4}$$

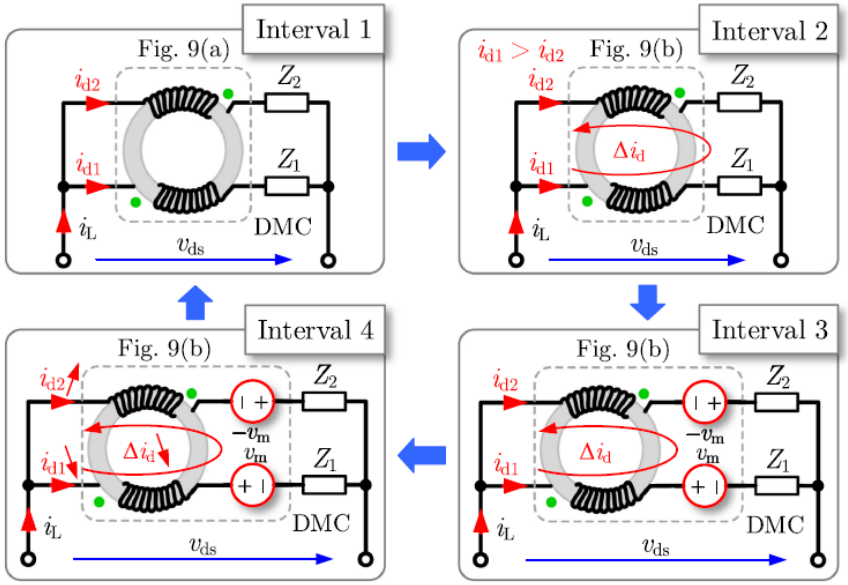
C. Zhao, et al, " A Method to Balance Dynamic Current of Paralleled SiC MOSFETs With Kelvin Connection Based on Response Surface Model and Nonlinear Optimization," IEEE TPEL, Feb. 2021

2. Challenges & Solutions

■ **Coupled drain inductors: DMC (Differential Mode Choke)**



Circuit schematic

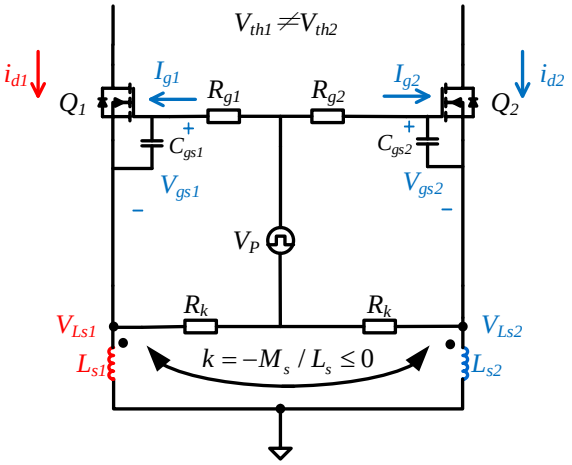


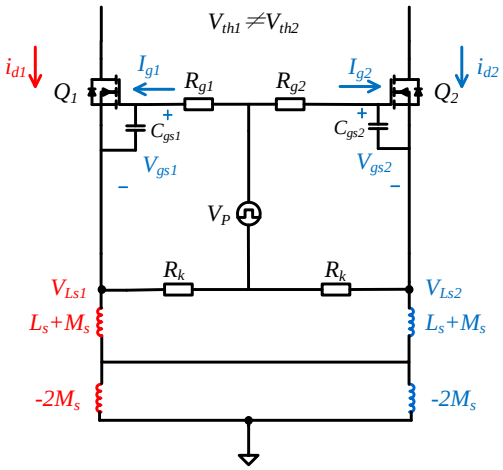
- Force currents in two coils to be equal based on magnetic coupling
- Simple but bulky size
- Large number of DMCs for multiple paralleled devices

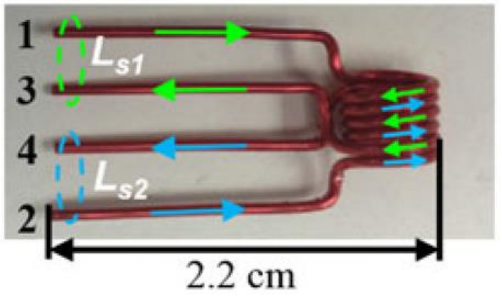
Z. Zeng, et al, "Imbalance Current Analysis and Its Suppression Methodology for Parallel SiC MOSFETs with Aid of a Differential Mode Choke," IEEE TIE, Feb. 2020

2. Challenges & Solutions

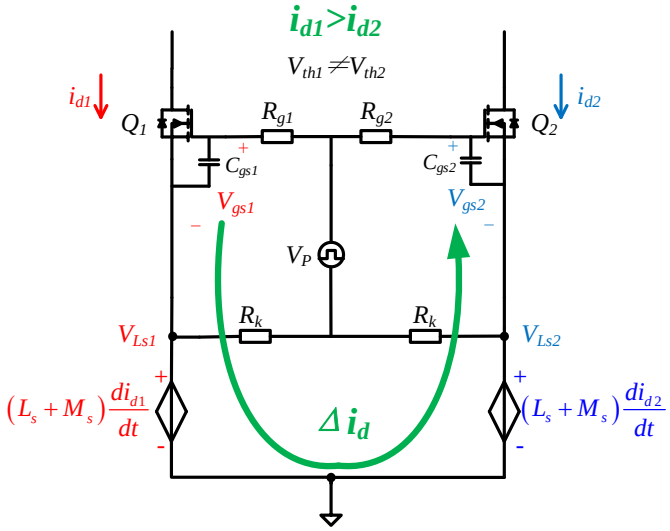
■ Coupled source inductor: **CMC (Common mode choke)**



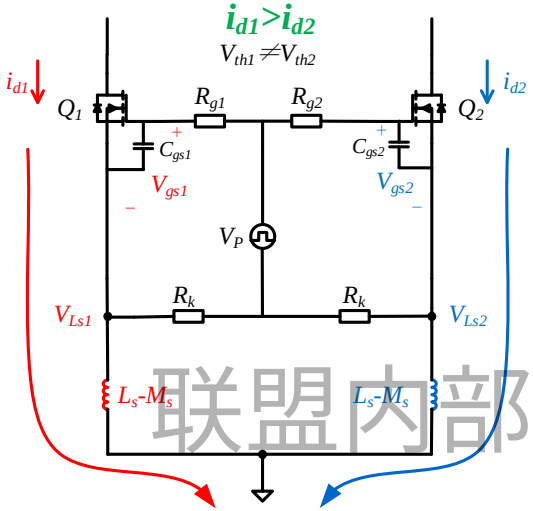




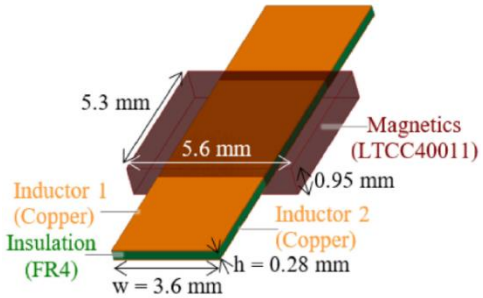
Coupled source inductor (air core)



DM equivalent circuit



CM equivalent circuit



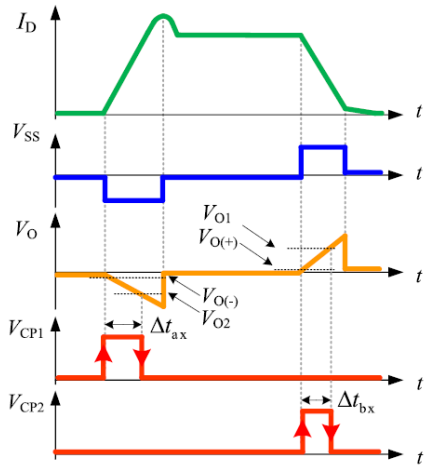
Coupled source inductor (w/ core)

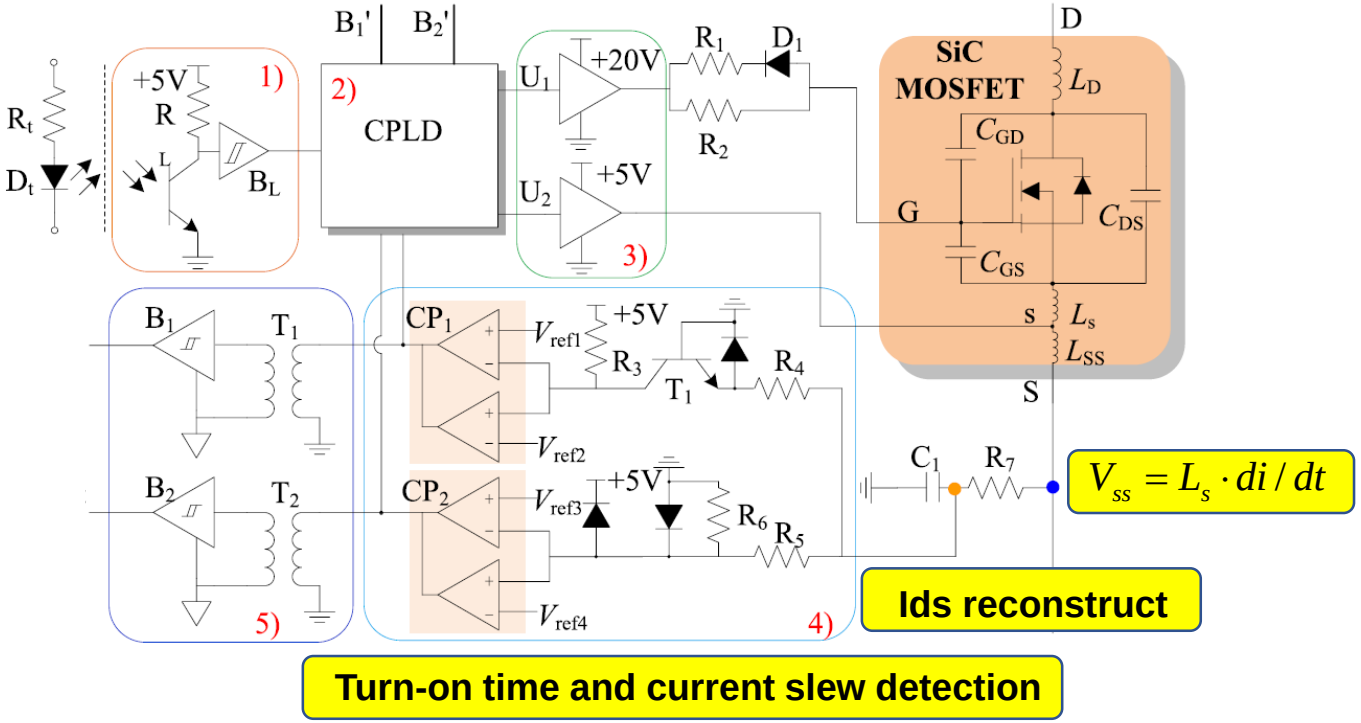
- Large Ls benefit current balancing
- Large Ls cause high voltage spike
- Coupled Ls: combined

Y. Mao, et al, "Balancing of Peak Currents Between Paralleled SiC MOSFETs by Drive-Source Resistors and Coupled Power-Source Inductors," IEEE Trans. on IE., Oct. 2017

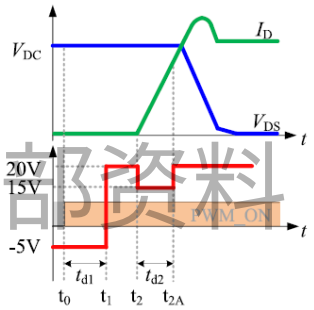
2. Challenges & Solutions

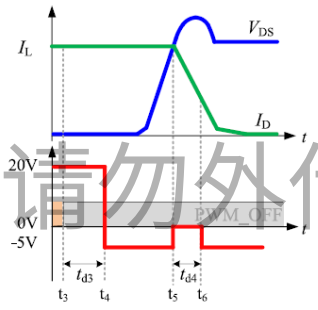
■ Digital AGD (Active Gate Driver)





- Reconstruct Ids waveform based on Ls (integration)
- Compared Ids with a fixed reference voltages
- Rising edge (turn-on time) and width (current slew rate)
- Control of slew rate w/ drive voltage (siwcthing 20V/15V)
- Control of turn-on time in multiple switching cycles by adjustment of drive signal in CPLD





Y. Wen, et al, " Active Gate Driver for Improving Current Sharing Performance of Paralleled High-Power SiC MOSFET Modules," IEEE TPEL, Feb. 2021

2. Challenges & Solutions

■ Summary of state-of-the-art methods

- ***Device Screening:***

  costly & low efficiency (parameters are temp. & time depended)

  Still affected by circuit parasitic parameters

- ***Layout optimization:***

  need device screening to achieve good current balancing

- ***Coupled inductors:***

  Bulky & introduce high parasitics (extra voltage stress)

- ***Active gate Driver:***

  high complexity (analog & digital circuit)

  low response time (multiple cycles)

Contents

3. AGD Method

- **Active gate driver**

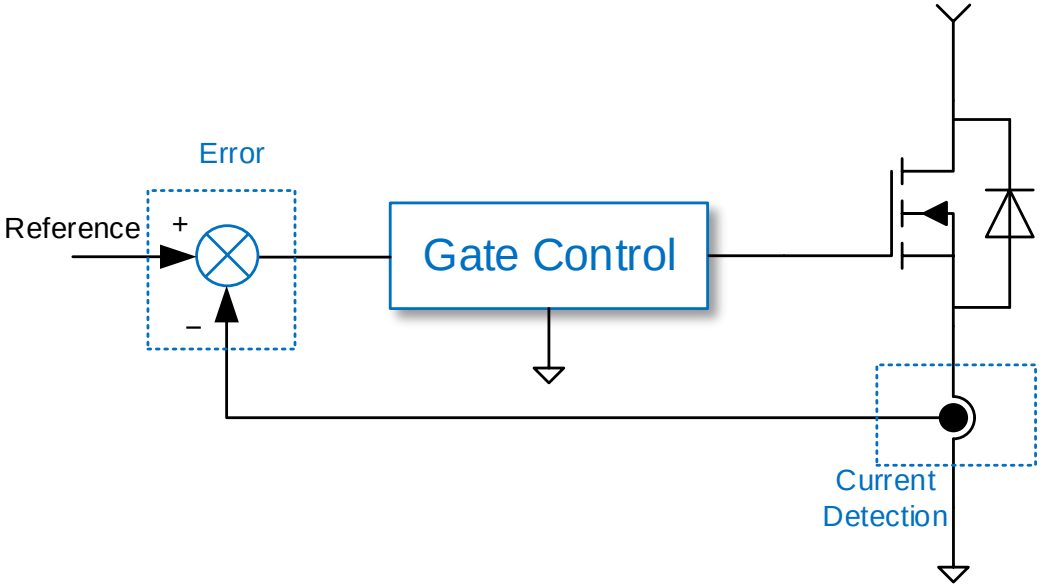


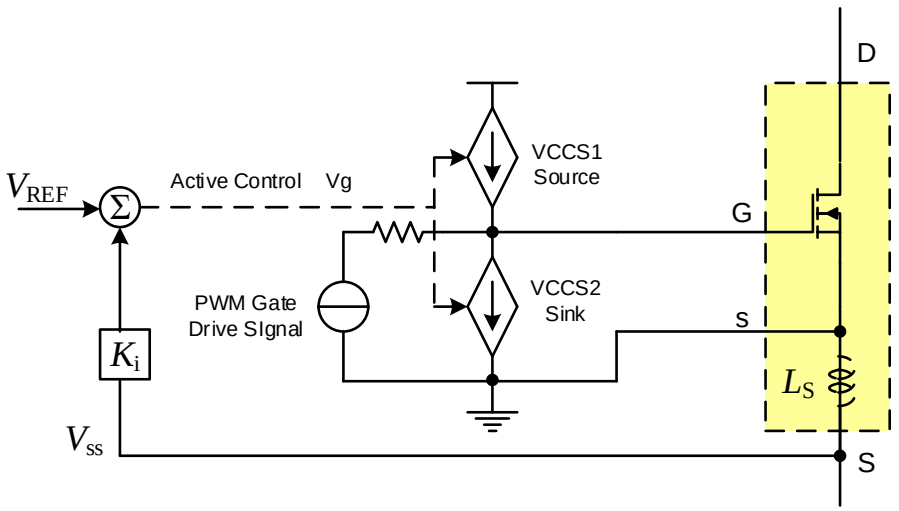
Diagram of active gate driver

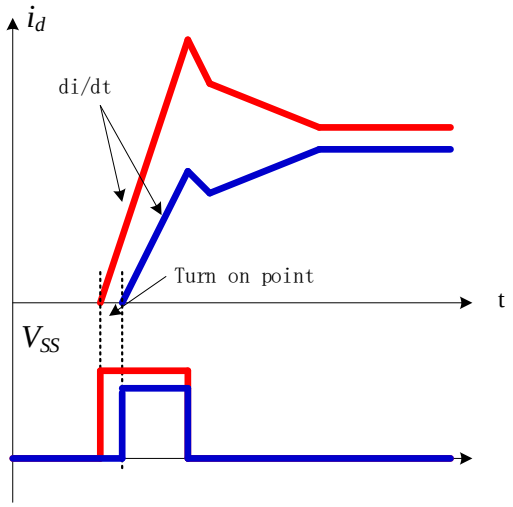
To achieve real-time dynamic current control (in single switching cycle):

- High-bandwidth current detection (**more than 10~30MHz**)
- Low delay time of control loop (**ns level**)
- Flexibility & scalability (**easily extended for multiple devices**)
- Simple, low cost & easy for integration

3. AGD Method

- **Proposed active gate driver method**





Voltage Controller Current Source:

VCCS1: source current to gate

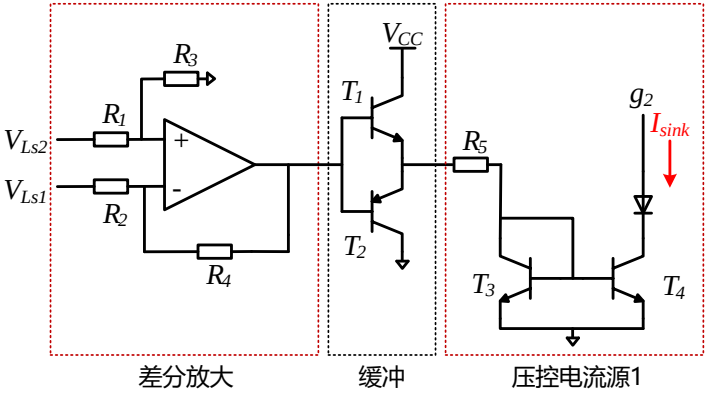
VCCS2: sink current to gate

Current sensing: Ls (Kelvin source & Power source)

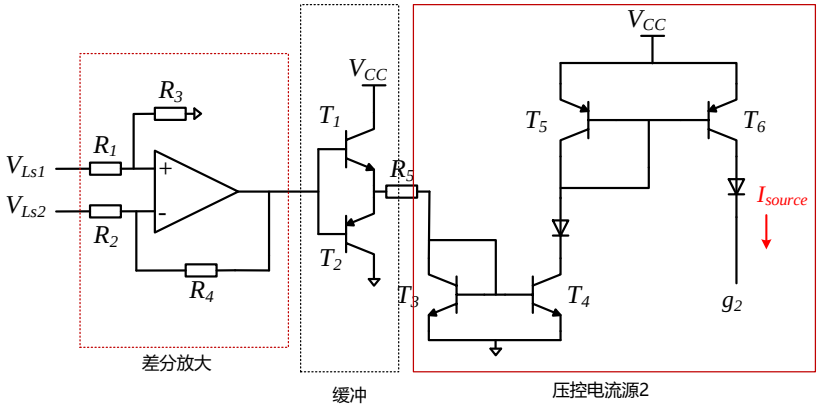
Turn on point & di/dt (amplitude)

3. AGD Method

VCCS Implementation

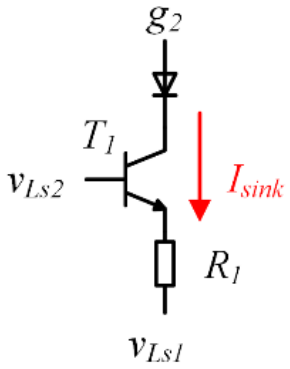


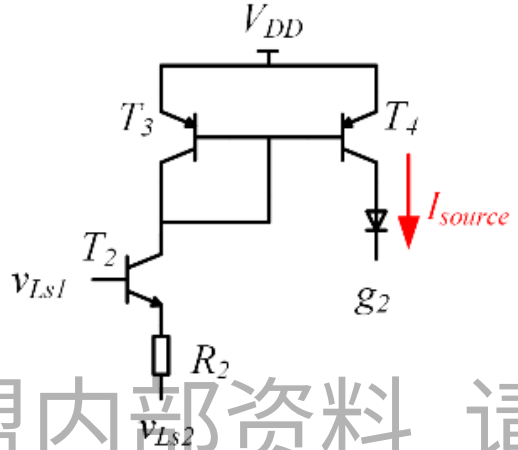
Current Sink Circuit



Current Source Circuit

BJT only
(V_{Ls} is large)



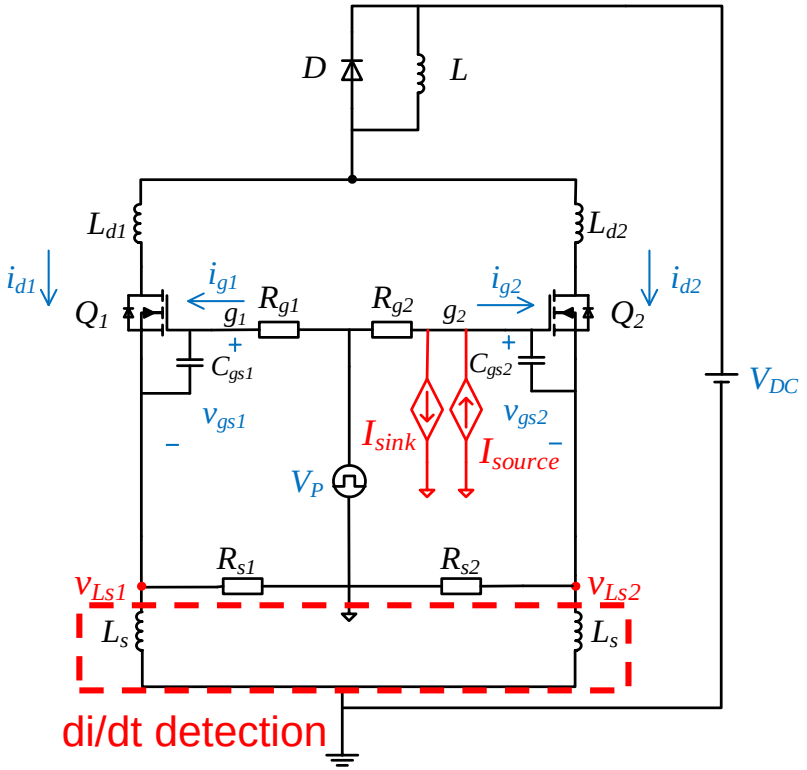


$$I_{sink} = \frac{v_{Ls2} - v_{Ls1} - V_{BE,T}}{R_1}$$

$$I_{source} = \frac{v_{Ls1} - v_{Ls2} - V_{BE,T}}{R_2}$$

3. AGD Method

■ Principle of Operation



- di/dt detection:

$$v_{Lsi} = L_s \frac{di_{di}}{dt}$$

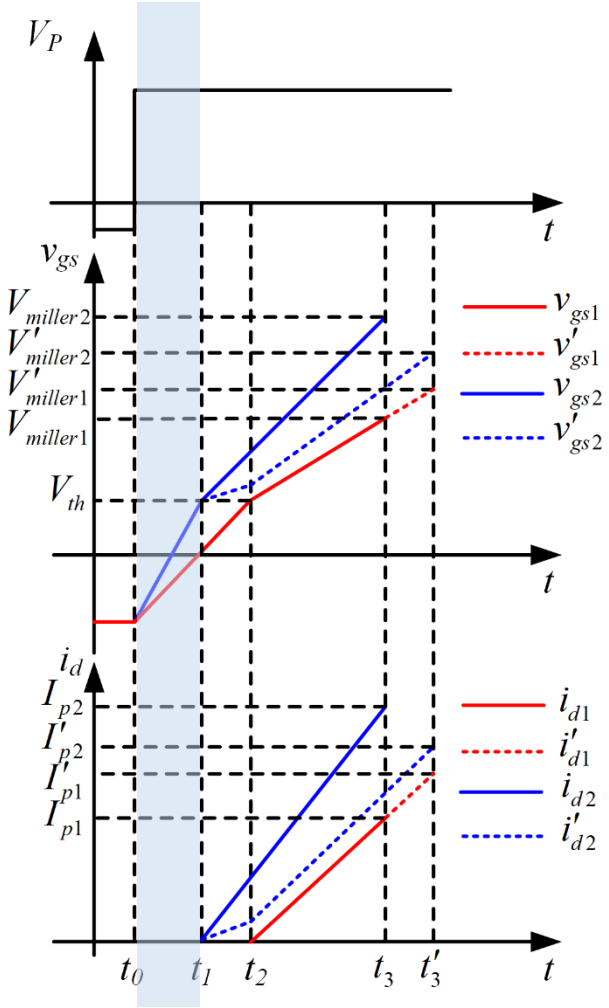
- VCCS (Voltage Controlled Current Source)
  - $v_{Ls1} > v_{Ls2}$: I_{source} is injected to i_{g2}
  - $v_{Ls1} < v_{Ls2}$: I_{sink} is extracted from i_{g2}

✓ **No complex current detection**

✓ **No high BW OPA required**

3. AGD Method

■ Principle of Operation



Take turn-on transient as an example

Assuming Vgs of device 1 reaches Vth firstly

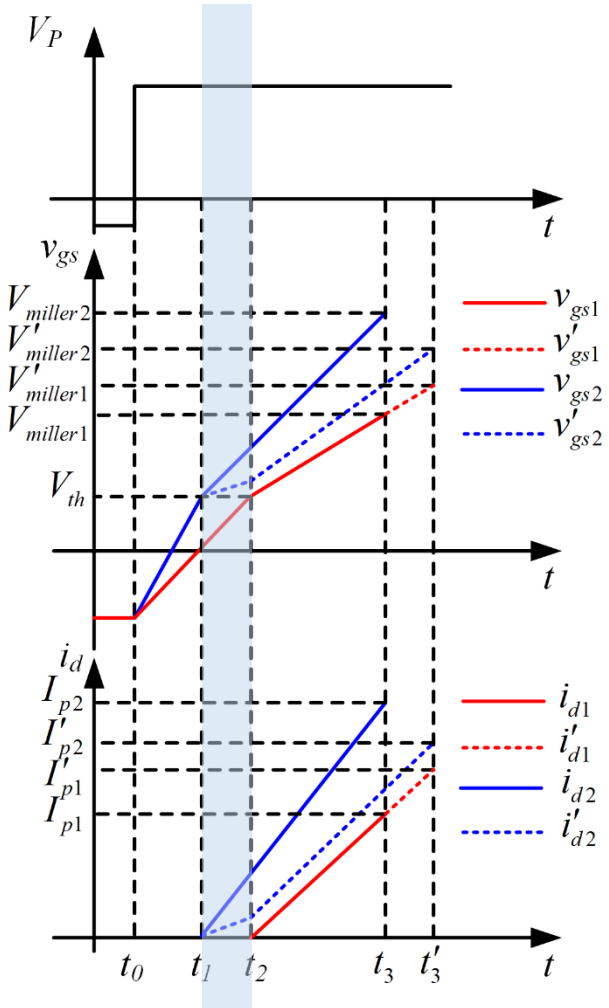
Stage 1 (t_0~t_1):

Vgs below Vth, currents keep at 0

x: parameters without AGD
x': parameters with AGD

3. AGD Method

■ Principle of Operation



x: parameters without AGD
x': parameters with AGD

Take turn-on transient as an example

Assuming Vgs of device 1 reaches Vth firstly

Stage 1 (t_0~t_1):

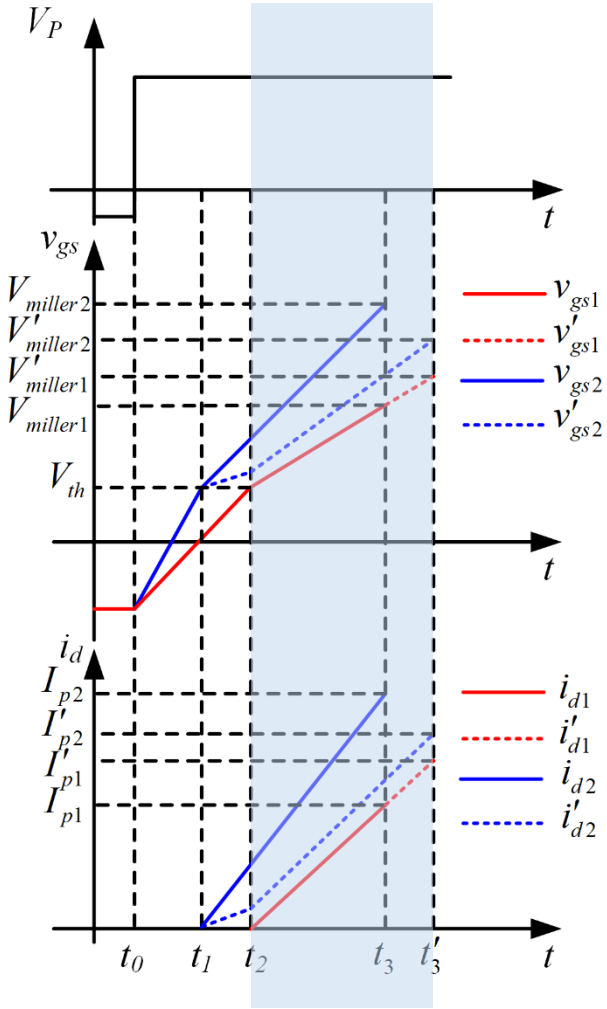
Vgs below Vth, currents keep at 0

Stage 2 (t_1~t_2):

Device 2 reaches Vth firstly, $V_{Ls2} > V_{Ls1}$, I_{sink} sinks current from Vgs2, di/dt reduced.

3. AGD Method

■ Principle of Operation



x: parameters without AGD
x': parameters with AGD

Take turn-on transient as an example

Assuming Vgs of device 1 reaches Vth firstly

Stage 1 (t_0~t_1):

Vgs below Vth, currents keep at 0

Stage 2 (t_1~t_2):

Device 2 reaches Vth firstly, $V_{Ls2} > V_{Ls1}$, I_{sink} sinks current from Vgs2, di/dt reduced.

Stage 3' (t_2~t'_3):

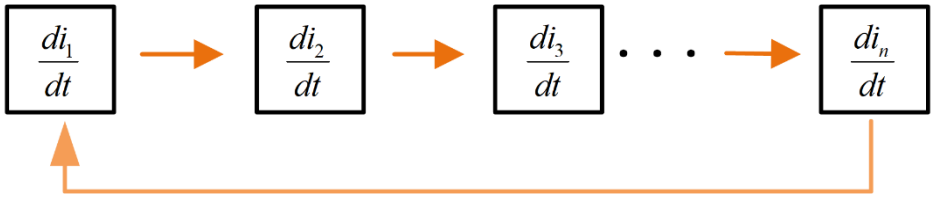
Device 1 reaches Vth at t2, current rising.

If di/dt(2) ≠ di/dt(1), VCCS will source/sink current

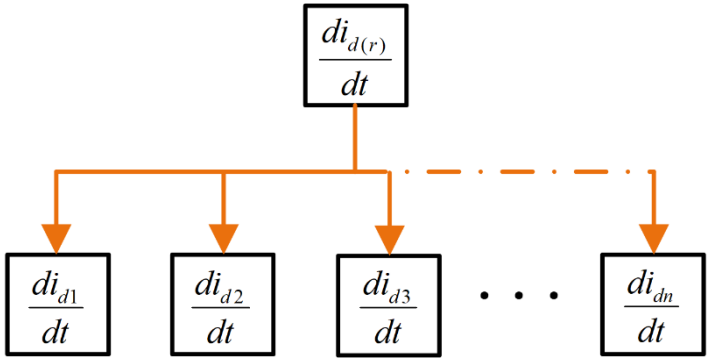
from Device 2 to keep same di/dt

3. Operation Principle of Proposed AGD

- **Scalability for multiple paralleled devices**



Daisy-chain structure

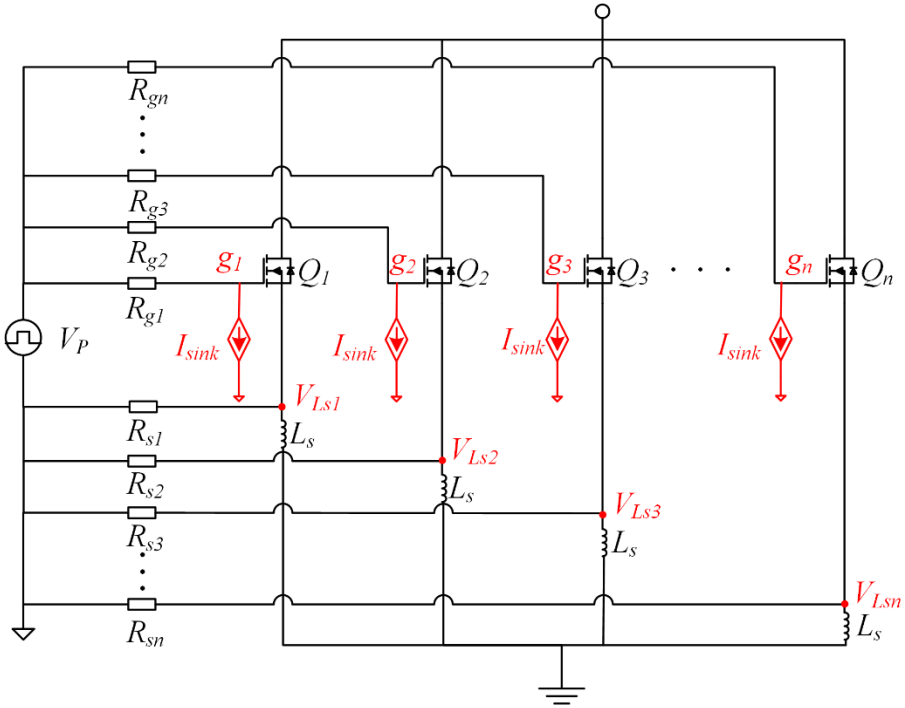


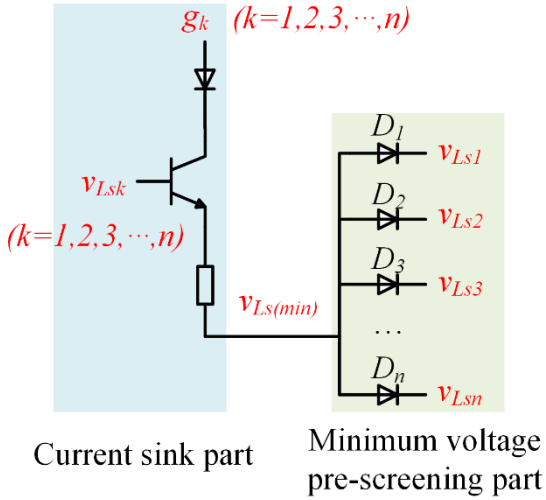
Master-slave structure

3. Operation Principle of Proposed AGD

■ Control scheme 1: democracy master-slave

The determination of master device: automatic





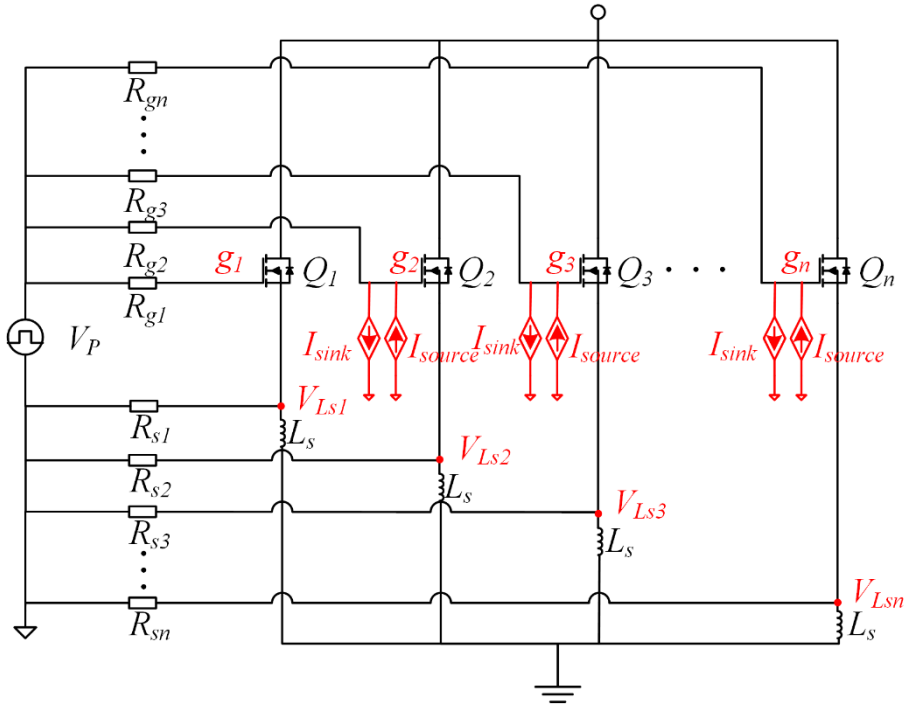
Using AND/OR gate, the slowest/fastest device is automatically selected as reference

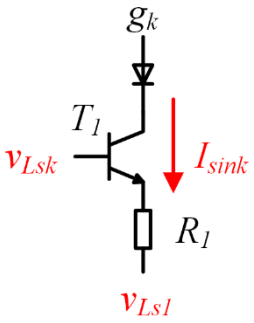
- Feedback circuit is simplified (only sink or source is reugired)
- The voltage drop of AND/OR gate will affect the current balancing accuracy

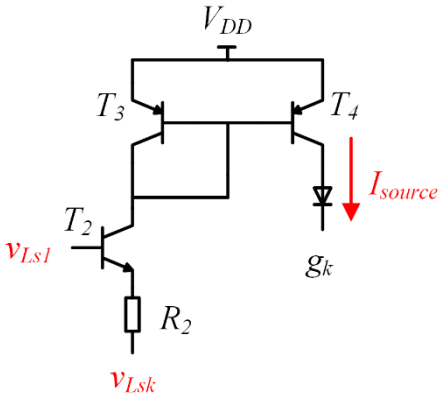
3. Operation Principle of Proposed AGD

■ Control scheme 2: dedicated master-slave

The determination of master device: dedicated







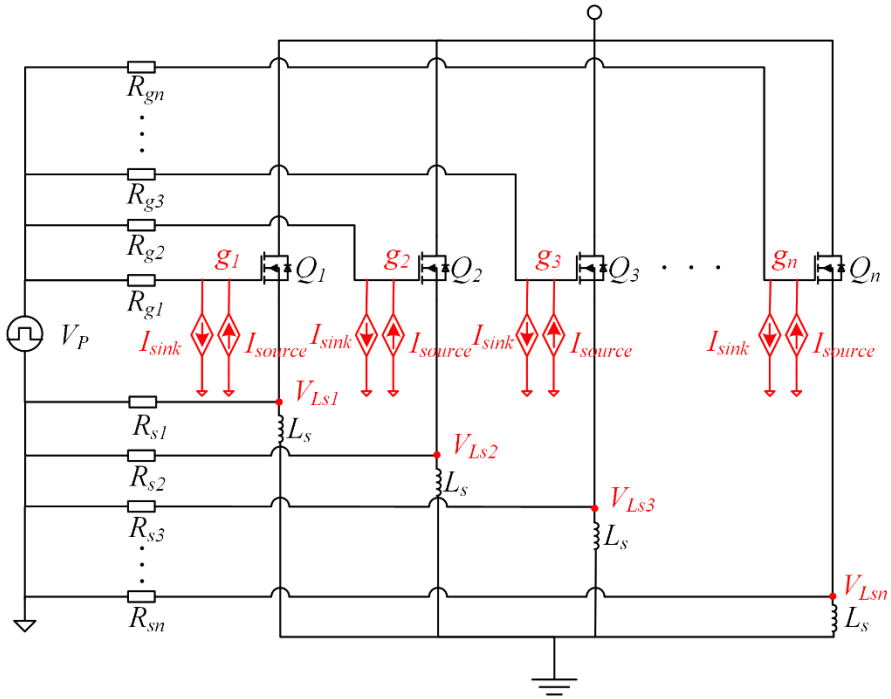
Any device can be chosen as the master device

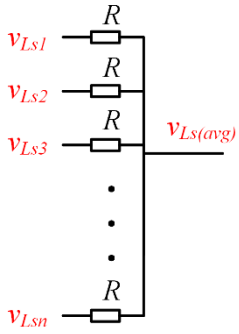
- Both sink and source current is required
- No extra circuit for master device selection

3. Operation Principle of Proposed AGD

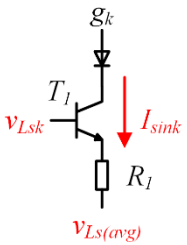
■ Control scheme 3: average method

The determination of master device: average

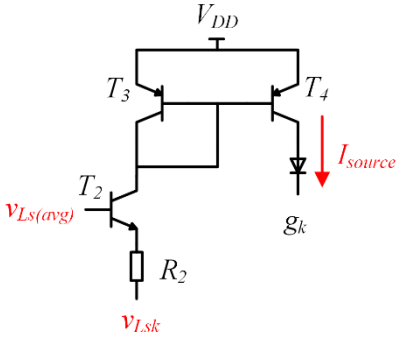




Voltage average calculation part



Current sink part



Current source part

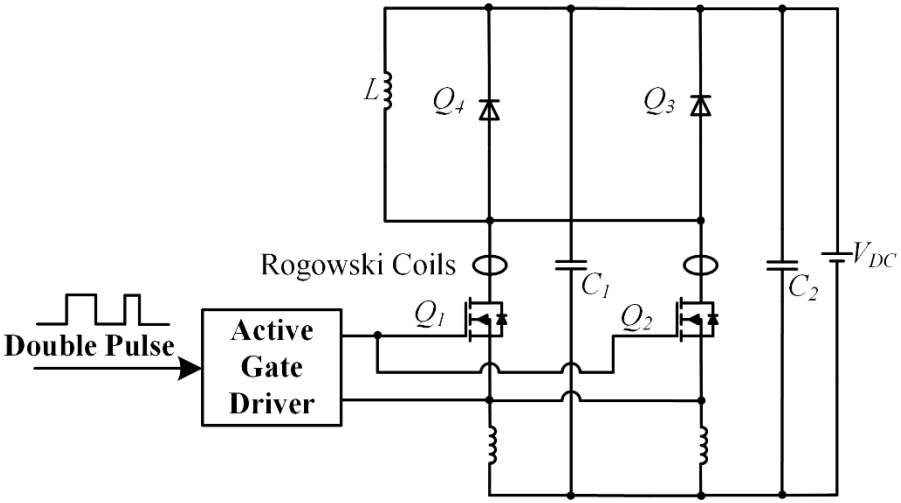
the average di/dt is used as the reference with a resistor network

- Both sink and source current is required
- No voltage drop causing voltage balancing accuracy

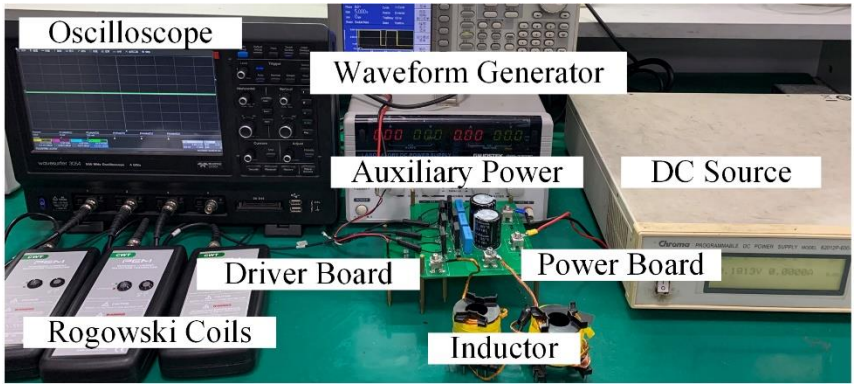
Contents

4. Experimental Results

■ Experimental platform



DPT (double pulse test) circuit

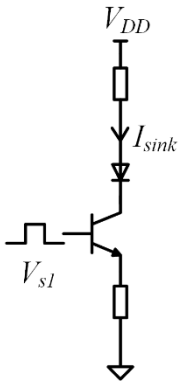


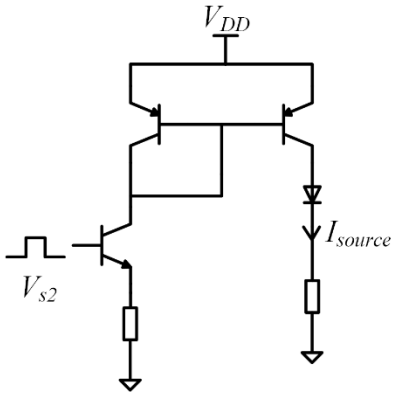
Hardware platform

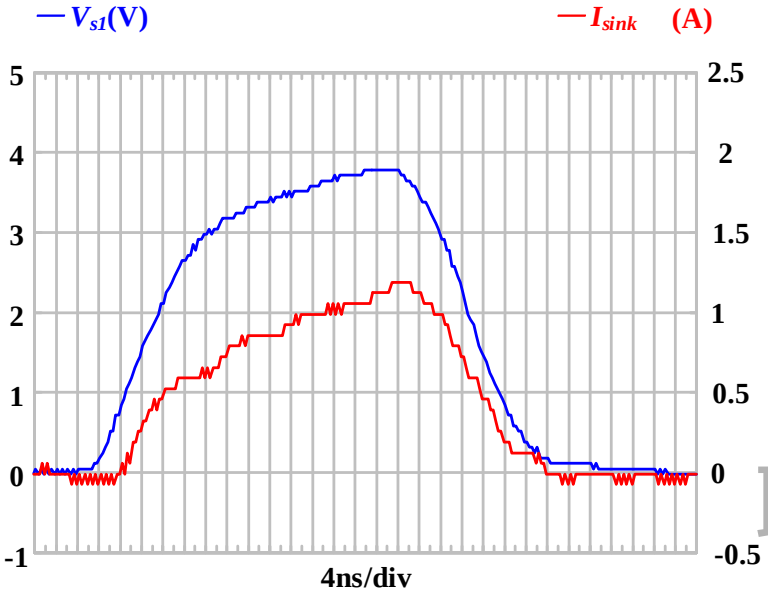
Components	Parameters
T_1, T_2 (NPN, CPH3215)	30V/3A/500MHz
T_3, T_4 (PNP, CPH3115)	30V/3A/450MHz
R_1, R_2	1Ω
SiC MOSFET (C3M0032120K)	1.2kV/63A/32mΩ

4. Experimental Results

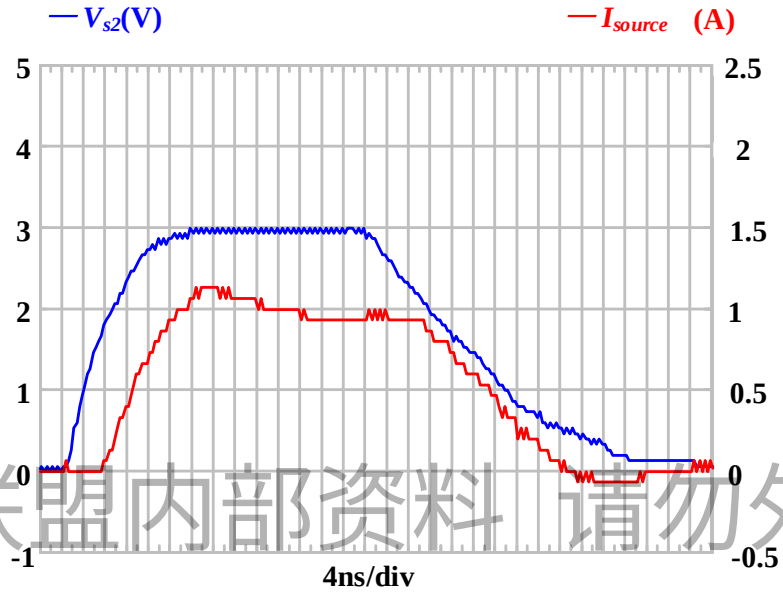
- **Response time of VCCSs**







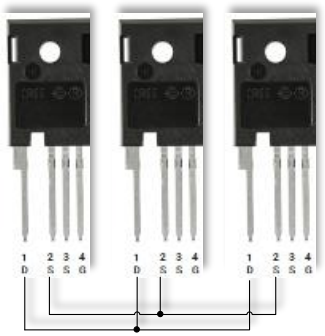
VCCS (sink): **~4ns**



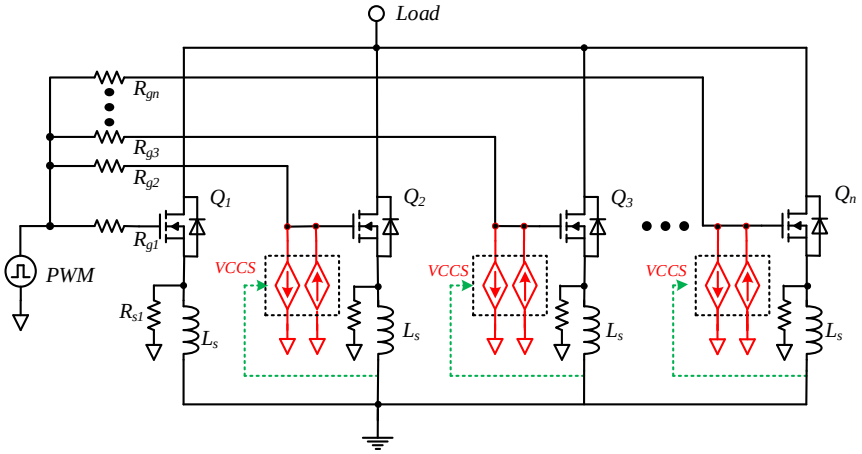
VCCS (source): **~7ns**

4. Experimental Results

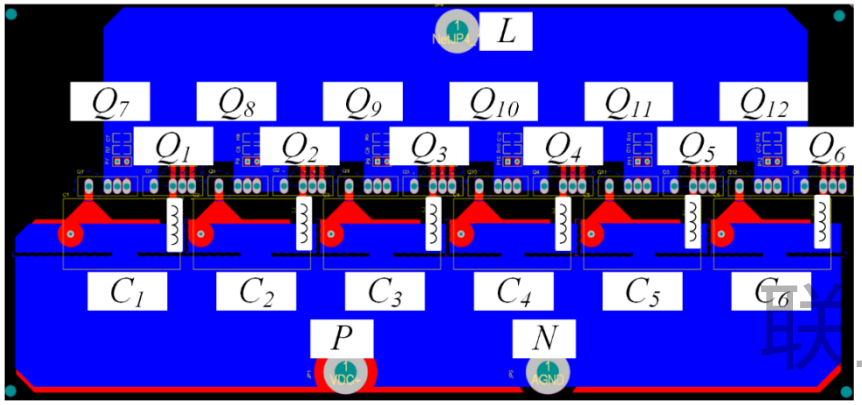
- **6pcs parallel example:**



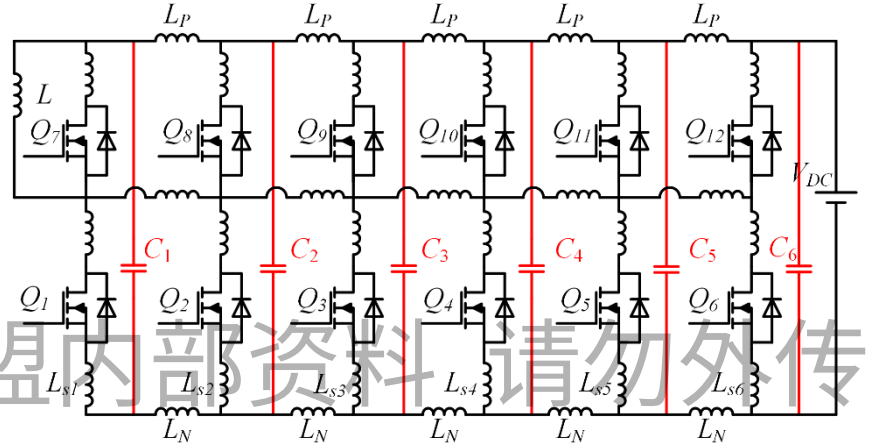
6*C3M0032120K



Dedicated master-slave structure



PCB Layout

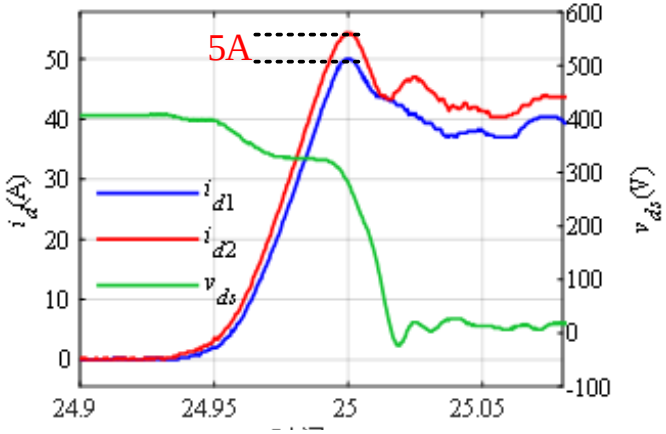


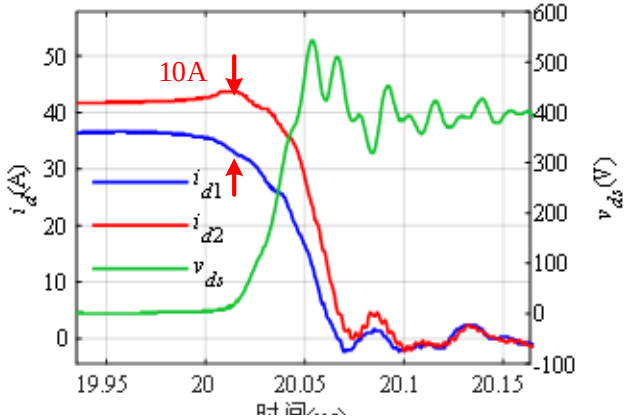
Schematic

4. Experimental Results

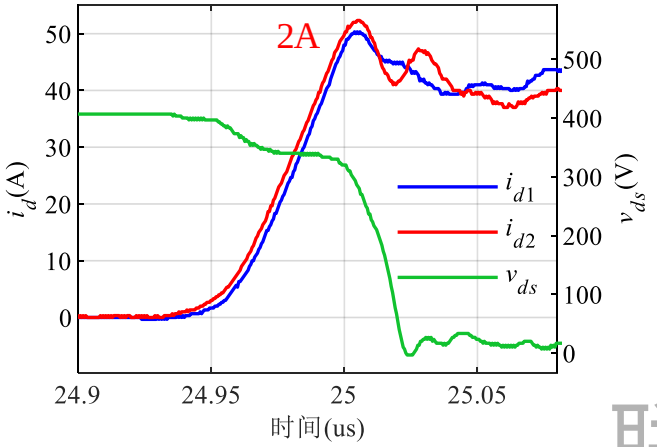
- **Experimental waveforms: 2pcs parallel**

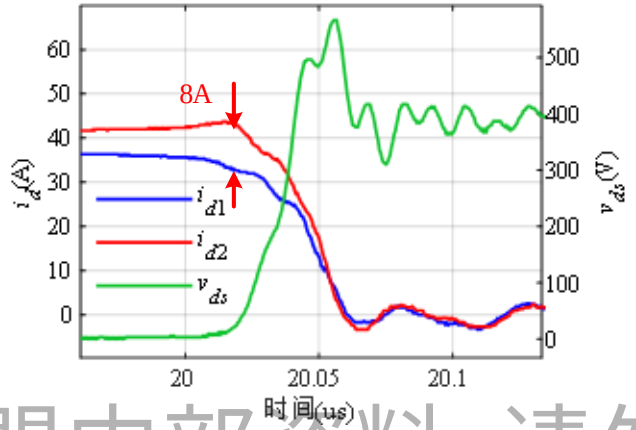
CGD





AGD





Eon: **~37% improvement**

CGD: 509/512uJ, 13.8%

AGD: 578/631uJ, 8.8%

Eoff: **~75% improvement**

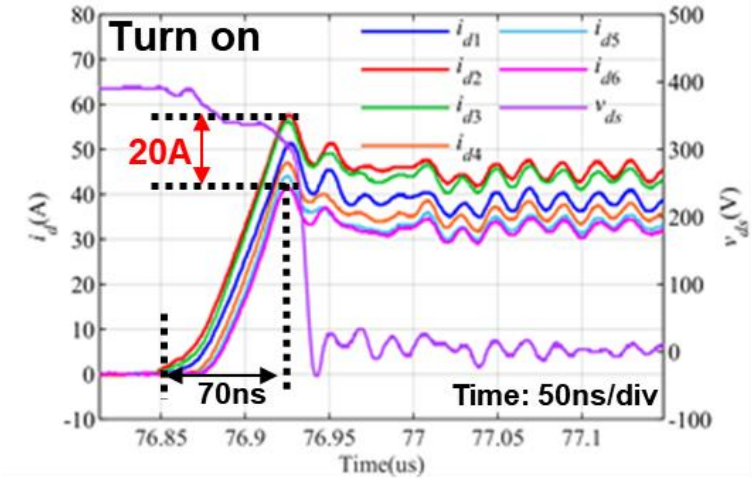
CGD: 233/414uJ, 56%

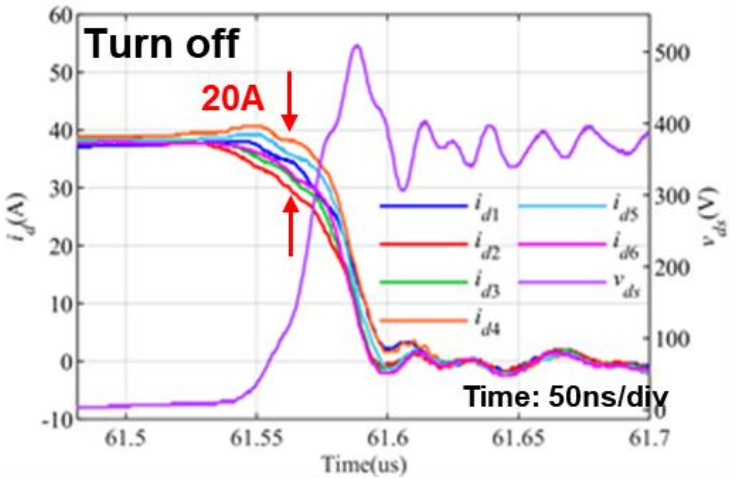
AGD: 211/246uJ, 13.8%

4. Experimental Results

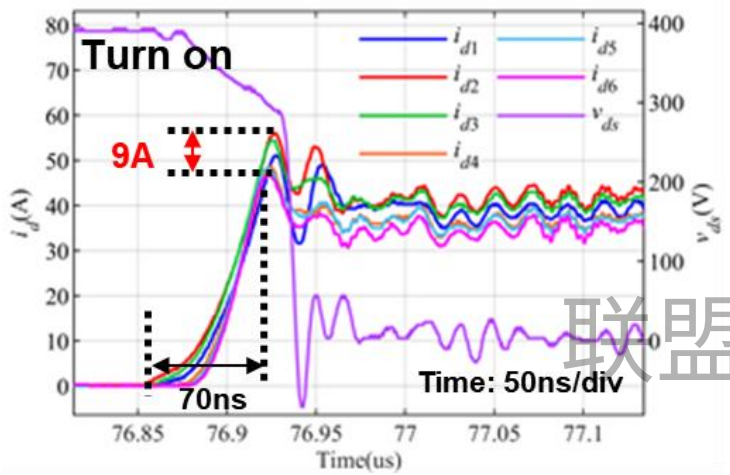
■ **Experimental waveforms:**

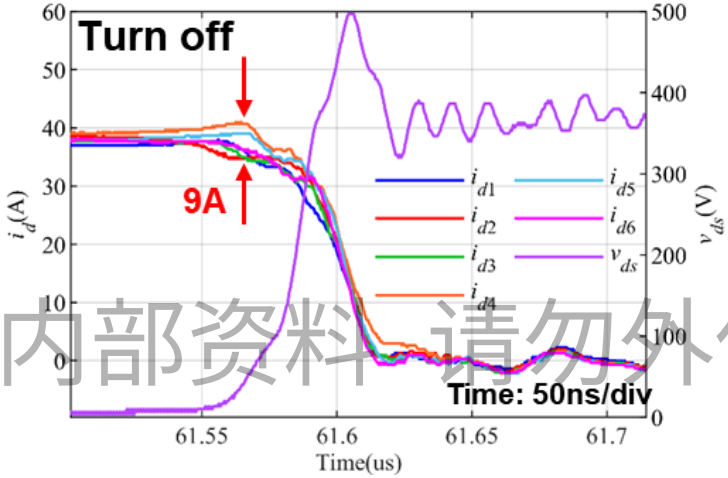
CGD





AGD

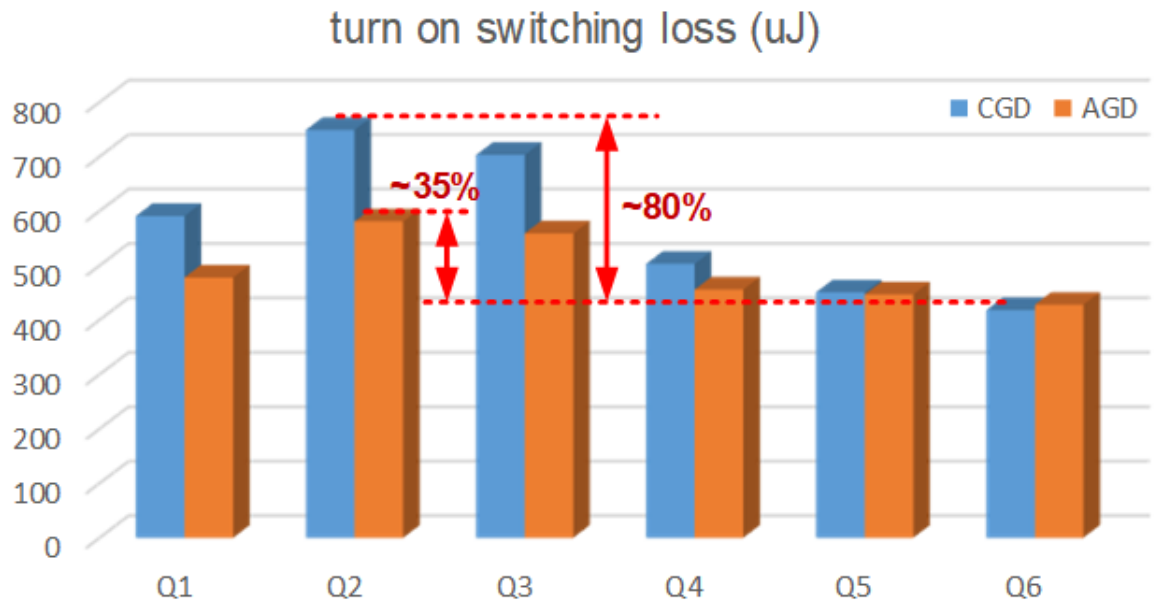




Dynamic current sharing performance: **~50% improvement**

4. Experimental Results

- **Experimental waveforms:**



Turn on loss deviation: **~55% improvement**

		Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	σ%
CGD	Turn-on (μJ)	591	749	703	503	451	418	21.8%
	Turn-off (μJ)	311	226	241	353	297	244	16.1%
AGD	Turn-on (μJ)	478	581	559	456	447	428	11.8%
	Turn-off (μJ)	283	302	293	357	311	291	7.8%

standard deviation: **~50% improvement**

Contents

5. Conclusion

- Parallel operation of SiC MOSFET is very common for high power applications （die, discrete, even power module)
- SiC devices have large parameters tolerance, some of them is temperature & time depended (device screen cannot guarantee a good match in the lifetime & operation conditions)
- Circuit parasitic also affect current balancing of paralleled devices
- Active gate drive is a promising way for dynamic current balancing

Thank you!

联盟内部资料 请勿外传