Dual Sequence PSPWM Strategies for Five-Level FCML Totem-pole PFC to Suppress Dynamic Voltage Ringing across Flying Capacitors

Linyi Bao, Yanqing Wu, Xinke Wu

***Abstract*—Flying capacitor multilevel totem-pole PFC (FCML TPPFC) significantly enhances the power density and efficiency of converters. However, in practical applications, AC voltage drop transient is unavoidable during grid operation, leading to an initial voltage imbalance across the flying capacitors. This imbalance induces dynamic voltage ringings in the flying capacitors, posing an overvoltage risk for the switching devices. Therefore, a mathematical model of the voltage ringings in the flying capacitors during the recovery stage is established. To address this issue, a dual sequence PSPWM modulation method is proposed to suppress dynamic ringing and achieve voltage balancing during bus voltage transients. A five-level PFC prototype was built to experimentally validate the proposed dual sequence PSPWM control strategy.**

***Index Terms*—Flying capacitor multilevel converter, totem-pole PFC, transient cancellation**

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I. INTRODUCTION

ADVANCES in artificial intelligence are driving a substantial increase in the power supply requirements of data centers, creating an urgent demand for power supply units (PSUs) with higher power density and efficiency. Extensive research indicates that multilevel converters enable significant improvements in power density compared to traditional two-level converters [1]-[3]. Among multilevel converter topologies, the Flying Capacitor Multilevel (FCML) converter has gained considerable attention due to its straightforward topology and control strategy [4]-[5]. However, in the FCML converter, the voltage across each switching device is clamped by the voltage of the flying capacitors. Therefore, ensuring voltage balance across the flying capacitors under all operating conditions is critical for proper converter operation. Phase shifted pulse width modulation (PSPWM) is commonly adopted in FCML converters and is recognized to provide a slow voltage balancing capability [6]-[9]. However, experimental observations indicate that the flying capacitors cannot always be guaranteed under practical operating conditions due to various non-ideal factors [10]. The mechanisms underlying successful natural balancing in some cases and its failure in others have therefore become a key focus of analysis. This understanding has motivated targeted improvements to ensure voltage balance under steady state operation. The proposed strategies can be broadly categorized into two main approaches.

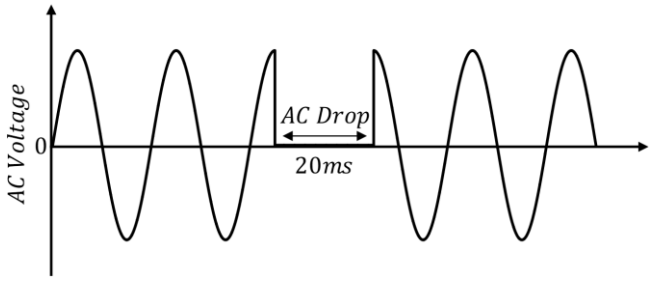
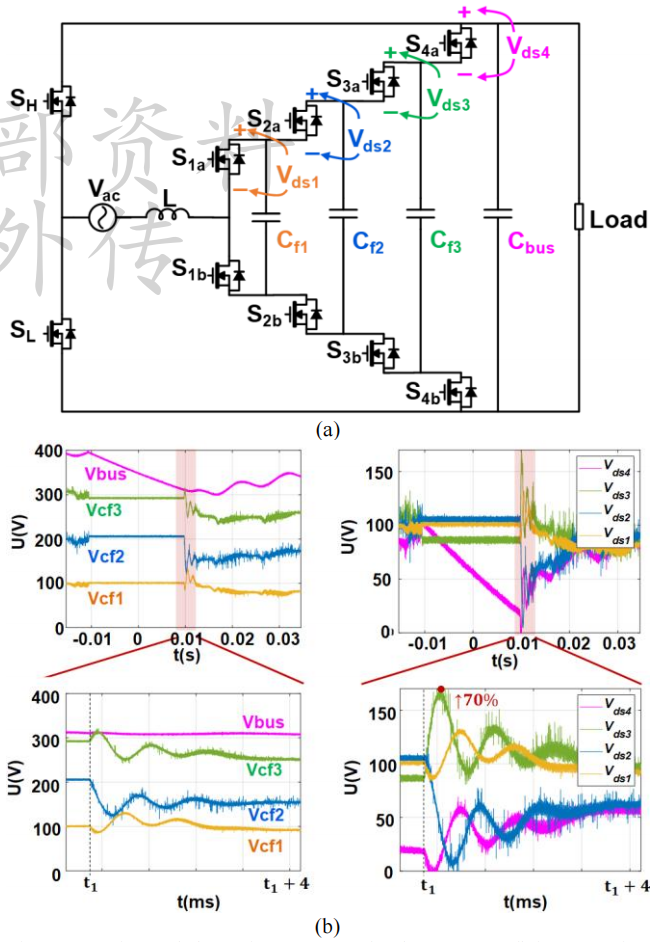


Fig. 1 Typical AC drop transient in grid side.



(a)

(b)

Fig. 2 Experimental dynamic response of voltage across flying capacitor subjected a 20ms AC Drop@90° in a five-level FCML PFC. (a) Topology of a five-level FCML. (b) Voltage across flying capacitors(left) and devices(right).

In the first approach, the flying capacitor voltages are regulated through direct sampling and closed loop feedback control [11]-

[14]. In the second approach, the inherent voltage balancing capability of the flying capacitor topology is enhanced [15][17], thereby reducing or eliminating the reliance on voltage sensors.

However, the majority of existing balancing methods are predominantly designed for steady state operation. Achieving voltage balance during dynamic conditions remains a critical challenge for the practical deployment of this topology. In particular, start-up transients and grid-side voltage fluctuations in PFC applications have received insufficient attention in the current literature. According to IEC 61000-4-11, grid-tied converters are required to withstand a 20 ms AC voltage drop transient which can be caused by lightning strikes, as shown in Fig. 1. When supplying power to a data center load, continuous power delivery is required, and the bus voltage continues to decline during this interval. Throughout the hold-up time, the converter operates in an over-current protection state triggered by the AC drop. Consequently, no current flows through the flying capacitors, and their voltages remain unchanged [16]. As a result, when the PFC resumes operation, the voltages across the flying capacitors and the bus voltage begin from an unbalanced initial state. To achieve a new balanced condition, the flying capacitor voltages undergo ringing, which can induce overvoltage across the switching devices and potentially compromise the power integrity of the converter [17]-[18]. Fig. 2 depicts the topology of a five level FCML converter, along with the ringing observed in the flying capacitor voltages and device voltages during restart following an AC voltage drop.

In DC-DC applications, the high bandwidth of active balancing control enables the flying capacitor voltages to rapidly balance with the output voltage transients [13]. In DC-AC inverter applications, increasing the resistive load can effectively suppress such high-frequency voltage ringing [18]. In AC-DC applications, however, the active balancing control loop for the flying capacitors must be designed with a bandwidth lower than that of the bus voltage control loop. The latter is itself constrained to a bandwidth below the double-line-frequency ripple present on the bus voltage which arises from the double-line-frequency power pulsation inherent to single-phase PFC [19]-[20]. Consequently, the high frequency voltage ringing across the flying capacitors shown in Fig. 2 cannot be suppressed by simply increasing the balancing loop bandwidth. Moreover, since the PFC inductor is located on the AC input side, introducing additional resistance in this path to dampen voltage ringing would result in unacceptable efficiency losses.

In order to suppress the dynamic ringing across the flying capacitors at ac dropping, a Model of the high frequency voltage ringing across the flying capacitors is first developed, from which it is shown that the magnitude of ringing is related to the DC bus voltage drop and the phase-shift sequence of PSPWM. After that, it is found that the voltage ringing dynamics can be suppressed by applying opposite phase shift sequences.

This article substantially extends our previously published conference paper [21]. The main new contributions are summarized as follows. In Section II, to improve the accuracy of the mathematical model and provide a clearer interpretation of the proposed method, the flying capacitor voltage ripple is incorporated as an additional model variable. To clarify the physical mechanism underlying the voltage ringing, a physics based analysis is added, and the maximum voltage stress on the switching devices is analytically derived for different initial bus voltage conditions. In Section III, to explain the slow low frequency variation in the flying capacitor voltages after the high frequency ringing is suppressed, a detailed charge imbalance analysis is provided. In Section IV, to more comprehensively validate the proposed method under different operating conditions, additional experimental waveforms are presented for grid voltage levels of 110 V and 220 V and for AC voltage drop events occurring at phase angles of 45° and 90°.

The remainder of this article is organized as follows: Section II introduces a mathematical model of high frequency flying capacitor voltage ringing that accounts for the voltage ripple of the flying capacitor, and presents the relationship between the maximum voltage stress across the switching devices and the degree of bus voltage sag. Section III presents the proposed dual sequence PSPWM modulation strategy, establishes a mathematical model of its mechanism for suppressing high frequency ringing, and explains the cause of the slow variation in the flying capacitor voltage after the high frequency ringing are suppressed. Section IV presents experimental waveforms demonstrating the suppression of high frequency flying capacitor voltage ringing using the dual sequence PSPWM approach under various grid voltage conditions and grid voltage sag angles. Finally, Section V concludes the article.

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II. Analysis of Flying Capacitor Voltage Dynamic Ringing During AC Drop Recovery Stage

To analyze the flying capacitor voltage ringing, the ampere-second balance of the flying capacitors and the volt-second balance of the PFC inductor current are essential. A large signal model of the FCML converter can be derived by calculating the variations in these state variables over one switching period. For instance, in Fig. 3, critical waveforms of PSPWM signal of a 5L FCML TPPFC within the range of $D \in [0,0.25]$ is depicted, along with the related inductor current shape i_L and flying capacitor current shape i_{Cfx} during 1 switching period (T_s) just after the recovery time t_1. For the mathematical simplicity reason, we make the following hypotheses:

(1) The grid side voltage is in the positive half cycle($v_{ac} > 0$, S_H off and S_L on).
(2) parasitic parameters such as ESR and ESL in the circuit are neglected.
(3) Input voltage v_{ac} is defined as v_{in} when analyzed on the time scale of switching cycles, bus voltage v_{bus} and input voltage v_{in} remain invariant within one switching period because v_{in} and v_{bus} vary at 50Hz and 100Hz respectively. Under a switching frequency of 60 kHz, the variation of v_{in} and v_{bus} within one switching cycle is less than 0.1% and 0.2% respectively.
(4) Capacitance of different flying capacitor stage is the same(Use film capacitors as flying capacitors).
(5) The switching devices of 5L FCML are controlled by

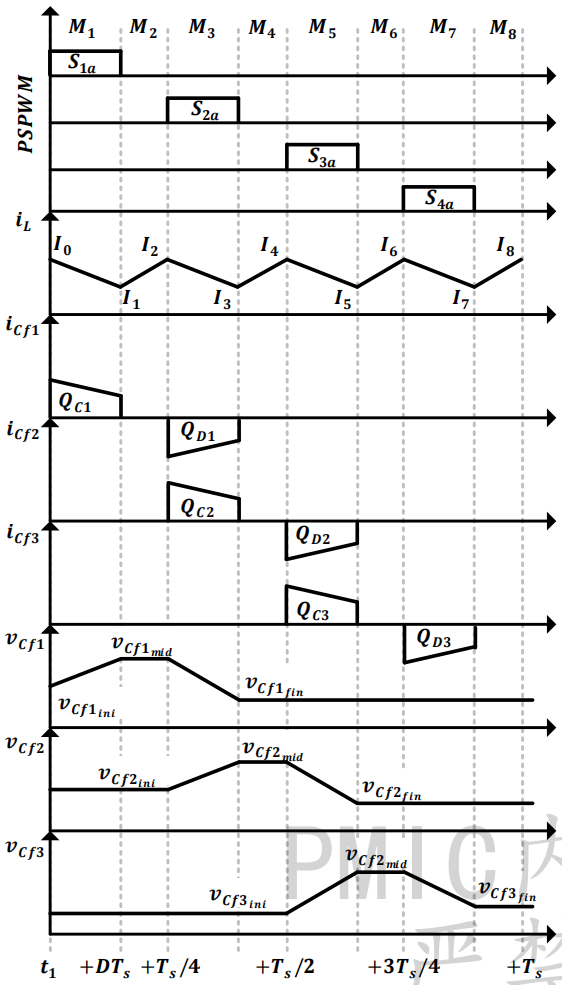

Fig. 3 Critical driving signals, current and voltage waveforms of 5L FCML in 1 switching period, D∈[0,0.25]

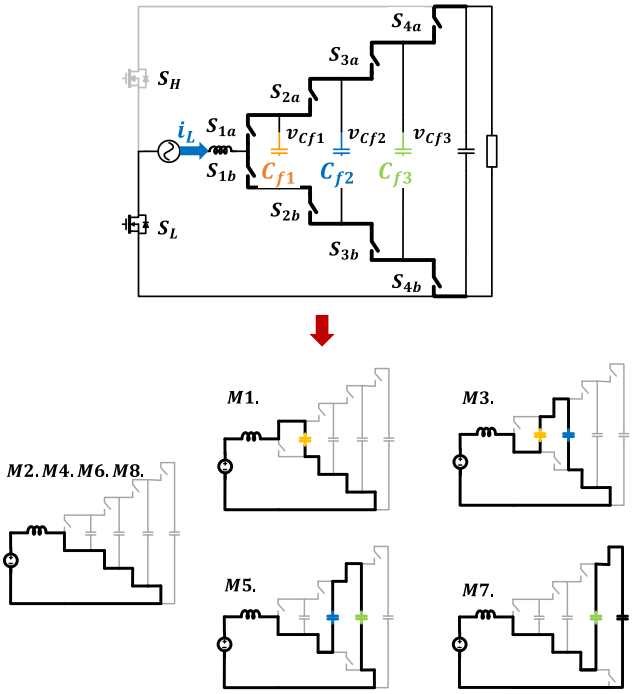

Fig. 4. Circuit and Equivalent operating modes of 5L FCML in 1 switching period, $D \in [0,0.25]$

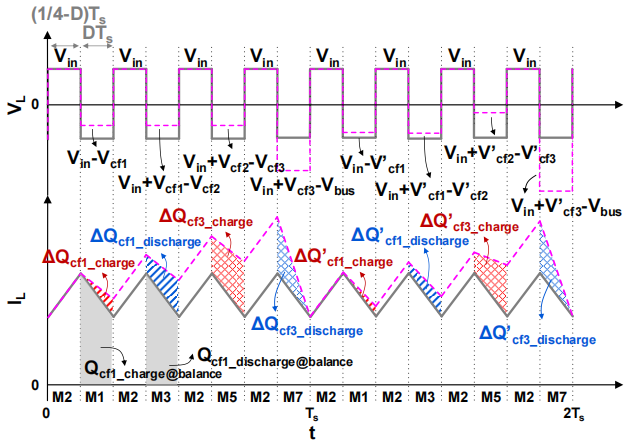

Fig. 5 Inductor volatge and current waveforms at restart.

common duty cycle, and the phase shift sequence is $S_{1a} \rightarrow S_{2a} \rightarrow S_{3a} \rightarrow S_{4a}$.

(6) In order to avoid over-current during recovery stage, we need to match the input and output voltage at the beginning of recovery time t_1, thus the initial duty cycle needs to be set to:

$$v_{in} = Dv_{bus} \quad (1)$$

Therefore, this switching period is divided into 8 modes and the related circuit modes is shown in Fig. 4. Fig. 5 presents the inductor voltage and inductor current waveforms after the restart instant t_1. At this moment, the bus voltage has dropped to v_{bus0}, and the duty cycle is $D = \frac{v_{in}}{v_{bus0}}$. If the flying capacitor voltages v_{Cf1}, v_{Cf2} and v_{Cf3} are distributed as $\frac{v_{bus0}}{4}$, $\frac{2v_{bus0}}{4}$ and $\frac{3v_{bus0}}{4}$ respectively, the inductor voltage exhibits the waveform shown by the upper gray curve. Owing to the balanced flying capacitor voltages, the inductor voltage amplitude remains equal during Modes M_1, M_3, M_5 and M_7. The corresponding inductor current, shown by the lower gray curve, exhibits identical current variations during these four modes. During the AC drop, however, all switching devices are turned off for protection, and the flying capacitor voltages are therefore preserved. Defining the steady state bus voltage as $V_{BUS0}(V_{BUS0} > v_{bus0})$ and the flying capacitor voltages as $\frac{V_{BUS0}}{4}$, $\frac{2V_{BUS0}}{4}$ and $\frac{3V_{BUS0}}{4}$, the inductor voltage and current waveforms after t_1 are shown by the purple dashed curves. Since the flying capacitor voltages are now higher than their steady state values corresponding to v_{bus0}, the inductor voltage amplitude is reduced during Modes M_1, M_3, and M_5, and elevated during Mode M_7. Because the total volt-second applied across the inductor over one switching cycle remains unchanged, the inductor current rises progressively throughout the switching cycle and finally returns to its initial value at the end of Mode M_7. Due to this progressive rise in inductor current, the discharge variation of flying capacitors C_{f1} and C_{f2} always exceeds their charge variation, causing v_{Cf1} and v_{Cf2} to decrease continuously. Conversely, the charge variation of C_{f3} always exceeds its discharge variation, causing v_{Cf3} to increase continuously. As a result, when v_{Cf1} and v_{Cf2} return to their steady state values, v_{Cf3} still remains above its steady state value. This prevents v_{Cf1} and v_{Cf2}

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from settling at their steady state levels and causes them to continue decreasing, thereby giving rise to the observed ringing phenomenon.

In order to quantitatively analyze the ringing of the flying capacitor voltages, a mathematical model is developed:

- In M_1, C_{f1} is charged and i_L decreases, so the charge of C_{f1} and change in inductor current are:

$$\begin{cases} Q_{C1} = \dfrac{(I_0 + I_1)DT_s}{2} \\ I_1 - I_0 = \dfrac{DT_s}{L}\left(v_{in} - \dfrac{v_{Cf1_{ini}} + v_{Cf1_{mid}}}{2}\right) \end{cases} \tag{2}$$

- In M_2, no FC is charged and i_L increases, so the change in inductor current is:

$$I_2 - I_1 = \frac{v_{in}\left(\frac{1}{4} - D\right)T_s}{L} \tag{3}$$

- In M_3, C_{f1} is discharged, meanwhile C_{f2} is charged and i_L decreases, so the discharge of C_{f1} ,charge of C_{f2} and change in inductor current are:

$$\begin{cases} Q_{D1} = Q_{C2} = \dfrac{(I_2 + I_3)DT_s}{2} \\ I_3 - I_2 = \dfrac{DT_s}{L}\left(v_{in} + \dfrac{v_{Cf1_{mid}} + v_{Cf1_{fin}}}{2} - \dfrac{v_{Cf2_{ini}} + v_{Cf2_{mid}}}{2}\right) \end{cases} \tag{4}$$

- In M_4, same to M_2, no FC is charged and i_L increases, so the change in inductor current is:

$$I_2 - I_1 = \frac{v_{in}\left(\frac{1}{4} - D\right)T_s}{L} \tag{5}$$

- In M_5, C_{f2} is discharged, meanwhile C_{f3} is charged and i_L decreases, so the discharge of C_{f1} ,charge of C_{f2} and change in inductor current are:

$$\begin{cases} Q_{D2} = Q_{C3} = \dfrac{(I_4 + I_5)DT_s}{2} \\ I_5 - I_4 = \dfrac{DT_s}{L}\left(v_{in} + \dfrac{v_{Cf2_{mid}} + v_{Cf2_{fin}}}{2} - \dfrac{v_{Cf3_{ini}} + v_{Cf3_{mid}}}{2}\right) \end{cases} \tag{6}$$

- In M_6, same to M_2, no FC is charged and i_L increases, so the change in inductor current is:

$$I_6 - I_5 = \frac{v_{in}\left(\frac{1}{4} - D\right)T_s}{L} \tag{7}$$

- In M_7, C_{f3} is discharged, meanwhile bus is charged and i_L decreases, so the discharge of C_{f3} and change in inductor current are:

$$\begin{cases} Q_{D3} = \dfrac{(I_6 + I_7)DT_s}{2} \\ I_7 - I_6 = \dfrac{DT_s}{L}\left(v_{in} + \dfrac{v_{Cf3_{mid}} + v_{Cf3_{fin}}}{2} - v_{bus}\right) \end{cases} \tag{8}$$

- In M_8, same to M_2, no FC is charged and i_L increases, so the change in inductor current is:

$$I_8 - I_7 = \frac{v_{in}\left(\frac{1}{4} - D\right)T_s}{L} \tag{9}$$

Thus, the voltage variation of flying capacitor voltages during 1 switching period can be calculated by subtracting the related discharges from charges:

$$\begin{cases} \Delta v_{Cf1} = \dfrac{1}{1 + \frac{4LC_f}{D^2T_s^2}}\left(2\overline{v_{Cf2}} - \dfrac{v_{in}}{D}\right) \\ \Delta v_{Cf2} = \dfrac{1}{1 + \frac{4LC_f}{D^2T_s^2}}\left(2\overline{v_{Cf1}} - 2\overline{v_{Cf3}} + \dfrac{v_{in}}{D}\right) \\ \Delta v_{Cf3} = \dfrac{1}{1 + \frac{4LC_f}{D^2T_s^2}}\left(2\overline{v_{Cf2}} - 2v_{bus} + \dfrac{v_{in}}{D}\right) \end{cases} \tag{10}$$

Where $k_1 = \frac{1}{T_s + \frac{4LC_f}{D^2T_s}}$, $\overline{v_{Cfx}}$ represents for average of different flying capacitor voltages like $\frac{v_{Cfx_{ini}} + v_{Cfx_{mid}}}{2}$ or $\frac{v_{Cfx_{mid}} + v_{Cfx_{fin}}}{2}$.

Subsequently, substituting (1) into (10), voltage dynamics of each flying capacitor can be calculated and organized into state space matrix form (11).

$$\begin{bmatrix} \dot{v_{Cf1}} \\ \dot{v_{Cf2}} \\ \dot{v_{Cf3}} \end{bmatrix} = k_1\left(\begin{bmatrix} 0 & -2 & 0 \\ 2 & 0 & -2 \\ 0 & 2 & 0 \end{bmatrix}\begin{bmatrix} \overline{v_{Cf1}} \\ \overline{v_{Cf2}} \\ \overline{v_{Cf3}} \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ -1 \end{bmatrix} v_{bus}\right) \tag{11}$$

Where $\dot{v_{Cfx}}$ represents for varying speed of different flying capacitor voltages and equals to $\frac{\Delta v_{Cfx}}{T_s}$, v_{bus} is the bus voltage, D is the duty cycle, T_s is the switching frequency, L is the inductance of PFC inductor, C_f is the capacitance of flying capacitors. From this model, it could be noticed that if $v_{bus} \neq 2(\overline{v_{Cf3}} - \overline{v_{Cf1}})$ or $v_{bus} \neq 2\overline{v_{Cf2}}$, there would be dynamics in flying capacitor voltages , which could explain the ringing reason when FCML TPPFC recovers from an unbalanced initial state. The state space matrix structures in other duty cycle intervals are also shown in (12) and (13).

- $D \in [0.25, 0.75]$:

$$\begin{bmatrix} \dot{v_{Cf1}} \\ \dot{v_{Cf2}} \\ \dot{v_{Cf3}} \end{bmatrix} = k_2\left(\begin{bmatrix} 0 & -2 & 0 \\ 2 & 0 & -2 \\ 0 & 2 & 0 \end{bmatrix}\begin{bmatrix} \overline{v_{Cf1}} \\ \overline{v_{Cf2}} \\ \overline{v_{Cf3}} \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ -1 \end{bmatrix} v_{bus}\right), \quad k_2 = \frac{1}{T_s + \frac{32LC_f}{(8(1-D)D - 1)T_s}} \tag{12}$$

- $D \in [0.75, 1]$:

$$\begin{bmatrix} \dot{v_{Cf1}} \\ \dot{v_{Cf2}} \\ \dot{v_{Cf3}} \end{bmatrix} = k_3\left(\begin{bmatrix} 0 & -2 & 0 \\ 2 & 0 & -2 \\ 0 & 2 & 0 \end{bmatrix}\begin{bmatrix} \overline{v_{Cf1}} \\ \overline{v_{Cf2}} \\ \overline{v_{Cf3}} \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ -1 \end{bmatrix} v_{bus}\right), \quad k_3 = \frac{1}{T_s + \frac{4LC_f}{(1-D)^2T_s}} \tag{13}$$

Therefore, the matrix structures of the state space models for different duty cycle intervals remain identical in a five level FCML converter. This invariance implies that, for a given initial flying capacitor voltage and bus voltage, the amplitude of the voltage ringing is consistent across different duty cycles. Consequently, the worst case overvoltage condition calculated for a specific duty cycle can also be applied to other duty cycle conditions under the same initial bus voltage. Since the flying capacitor voltages remain unchanged during the hold-up time, the magnitude of the bus

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voltage drop becomes the critical factor in determining the ringing amplitude of the flying capacitor voltages and, consequently, the safe operating threshold. In order to determine the ringing magnitude of flying capacitor voltages, the time domain expression of v_{Cf} ringing in $D \in [0,0.25]$ can then be calculated as:

$$\begin{cases} v_{Cf1}(t) = \frac{1}{4}[-v_{bus0} + 2v_{Cf10} + 2v_{Cf30} \\ \qquad +A\sin(\omega t + \varphi)] \\ v_{Cf2}(t) = \frac{1}{4}[2v_{bus0} + \sqrt{2}A\sin(\omega t - \varphi)] \\ v_{Cf3}(t) = \frac{1}{4}[v_{bus0} + 2v_{Cf10} + 2v_{Cf30} \\ \qquad -A\sin(\omega t + \varphi)] \end{cases} \quad (14)$$

$$A = \sqrt{\left(v_{bus0} + 2v_{Cf10} - 2v_{Cf30}\right)^2 + 2\left(v_{bus0} - 2v_{Cf20}\right)^2} \quad (15)$$

$$\omega = \frac{D^2 T_s}{\sqrt{2}LC_f} \quad (16)$$

$$\varphi = \tan^{-1}\frac{v_{bus0} + 2v_{Cf10} - 2v_{Cf30}}{\sqrt{2}\left(v_{bus0} - 2v_{Cf20}\right)} \quad (17)$$

Where v_{Cfx0} and v_{bus0} represent the initial voltage of C_{fx} and initial bus voltage respectively. The amplitude of the oscillatory component A is positively correlated with the bus voltage dip magnitude, and the ringing frequency ω is determined by the switching frequency f_s, the gain at that instant, the power inductor L and the flying capacitor C_f. Moreover, if the flying capacitor voltages remain unchanged before the restart, the initial phase angle of the ringing is a fixed value $\varphi \approx \tan^{-1}\frac{1}{\sqrt{2}}$, because $2v_{Cf10} - 2v_{Cf30} \approx -2v_{Cf20}$.

The calculation results are then compared with experiment by a simple calculation case shown in Fig. 6, and achieved a good match with each other. The error of flying capacitor voltage between experiment and calculation is defined as $\Delta v_{cfx} = \frac{v_{cf_{Cal}} - v_{cf_{Exp}}}{v_{cf_{Exp}}}$, Δv_{cf1}, Δv_{cf2} and Δv_{cf3} in Fig. 4 are approximately 2%, 15%, and 11% respectively and the error continues to increase over time. This is largely due to the fact that the ringing has already undergone a damping attenuation(including the effects of inductor DCR, device R_{dson}, which are not accounted for in the mathematical model). Therefore, this time domain model is suitable for us to determine the safe operation threshold of FCML PFC under ideal condition.

Equation (15) reveals that the lower v_{bus0}, the larger the ringing amplitude of the flying capacitor voltages. To intuitively relate v_{bus0} to the device voltage stress v_{ds}, the latter is expressed as the voltage difference between two adjacent flying capacitors($v_{dsx} = v_{cfx+1} - v_{cfx}$). Then, the max voltage stress across switching devices could be calculated by the max voltage difference between adjacent flying capacitor stages(18)(Assume $v_{Cf10} = 100V$, $v_{Cf20} = 200V$, $v_{Cf30} = 300V$ and $v_{bus0} \in [300,400]V$, which is reasonable since v_{Cfx} remains invariant while the bus voltage keeps dropping during the protection stage).

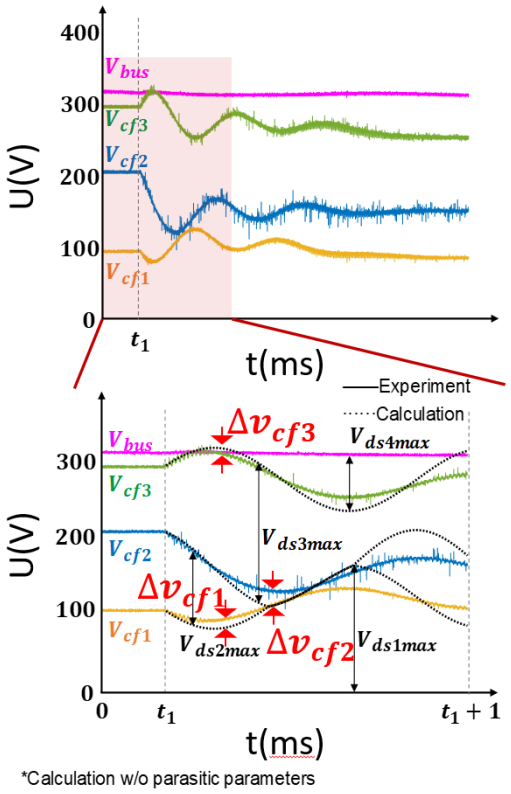

Fig.6 Comparison between experiment and calculation ringing waveform with same initial condition(L=29nH,$C_{f1,2,3}$=8uF,f_s=60kHz).

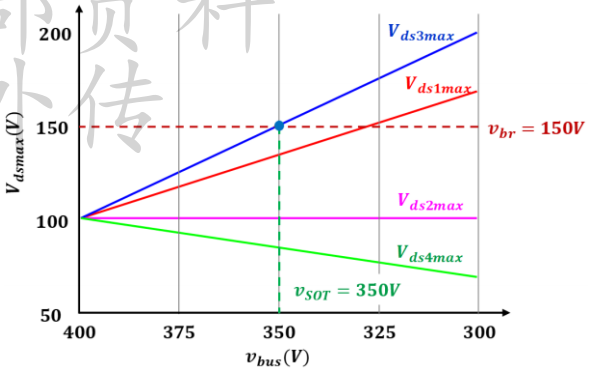

Fig. 7 v_{bus} safe operation threshold determined of switching device.

$$\begin{cases} v_{ds1max} = (200 + 100\sqrt{3}) - (1 + \sqrt{3})\frac{v_{bus0}}{4} \\ v_{ds2max} = 100 \\ v_{ds3max} = 500 - v_{bus0} \\ v_{ds4max} = (-200 + 100\sqrt{3}) + (3 - \sqrt{3})\frac{v_{bus0}}{4} \end{cases} \quad (18)$$

From equations (18), it is noticed that v_{dsmax} is determined by initial bus voltage v_{bus0}, whose relationship is also shown in Fig. 7. For a 5L FCML TPPFC, switching device with the breakdown voltage of 150V is selected($v_{dsxmax} < 150$):

$$\begin{cases} v_{ds1max} < 150V: v_{bus0} > 500 - 100\sqrt{3} \\ v_{ds2max} < 150V: independent\ of\ v_{bus0} \\ v_{ds3max} < 150V: v_{bus0} > 350 \\ v_{ds4max} < 150V: v_{bus0} < 500 + \frac{100}{3}\sqrt{3} \end{cases} \quad (19)$$

From Fig. 7 and (19), it can be concluded that, bus voltage should not drop to lower than 350V, otherwise, the voltage

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stress across S_{3a} and S_{3b} may surpass the breakdown voltage. This bus voltage, referred to as the safe operation threshold voltage v_{SOT}, is defined as the minimum bus voltage level below which ringings can cause device damage. Furthermore, Fig. 7 and (19) indicate that the voltage stress v_{ds3max} across S_{3a} and S_{3b} is consistently the highest. This phenomenon is determined by the phase term φ in (17). Since the phase value is constant $\varphi \approx \tan^{-1}\frac{1}{\sqrt{2}}(2v_{Cf10}-2v_{Cf30} \approx -2v_{Cf20})$, v_{Cf3} always increases initially, whereas v_{Cf1} and v_{Cf2} always decrease initially. As a result, v_{ds3} is simultaneously enlarged by v_{Cf2} and v_{Cf3}, making it always the largest among the devices.

However, during the hold-up time, the bus voltage normally could be allowed to drop to about 311V. Thus, S_{3a},S_{3b}, S_{1a},S_{1b} all have damage risk under the severe flying capacitor voltage ringing condition. Considering the risk, this article further investigates how to cancel the flying capacitor voltage ringing cause by traditional PSPWM.

III. Proposed Dual Sequence PSPWM for Cancelling Flying Capacitor Voltage Ringing

Section II explains the mechanism of the flying capacitor voltage variation during the restart stage, with reference to Fig. 5. It is shown that the voltage imbalance among the flying capacitors leads to asymmetry in the inductor voltage, which in turn causes asymmetry in the inductor current and consequently results in imbalanced charge and discharge of the flying capacitors. In addition, the analysis presented in Section II demonstrates that the flying capacitor voltage imbalance has no effect on the total inductor volt-second, and therefore does not affect the voltage gain. Under this premise, the inductor voltage waveform shown in Fig. 8(c) can be constructed over two adjacent switching cycles. The sequence of commutation modes in the second switching cycle is arranged in reverse order relative to that in the first switching cycle. Specifically, Mode 7, which is the last mode in the first switching cycle and causes a rapid decrease in the inductor current, is advanced to the first mode position in the second switching cycle.

Taking flying capacitor C_{f1} as an example, the inductor current rises progressively in both switching cycles. The difference lies in the charge behavior: in the first switching cycle, C_{f1} is first charged and then discharged after the inductor current has increased, resulting in a net decrease of charge($\Delta Q_{cf1_charge} < \Delta Q_{cf1_discharge}$). In the second switching cycle, C_{f1} is first discharged and then charged after the inductor current has increased, resulting in a net increase of charge($\Delta Q'_{cf1_charge} > \Delta Q'_{cf1_discharge}$). Over the two switching cycles, the net charge variation of C_{f1} is cancelled; consequently, the voltage of flying capacitor can be regarded as essentially constant on the time scale of two switching cycles.

To achieve this symmetric charge and discharge characteristic for every flying capacitor, the mode distribution shown in Fig. 8(c) is constructed. Fig. 8(a) illustrates the PWM waveforms under traditional PSPWM modulation. To operate the converter according to the mode sequence illustrated in Fig. 8(c), a dual sequence PSPWM modulation strategy is proposed

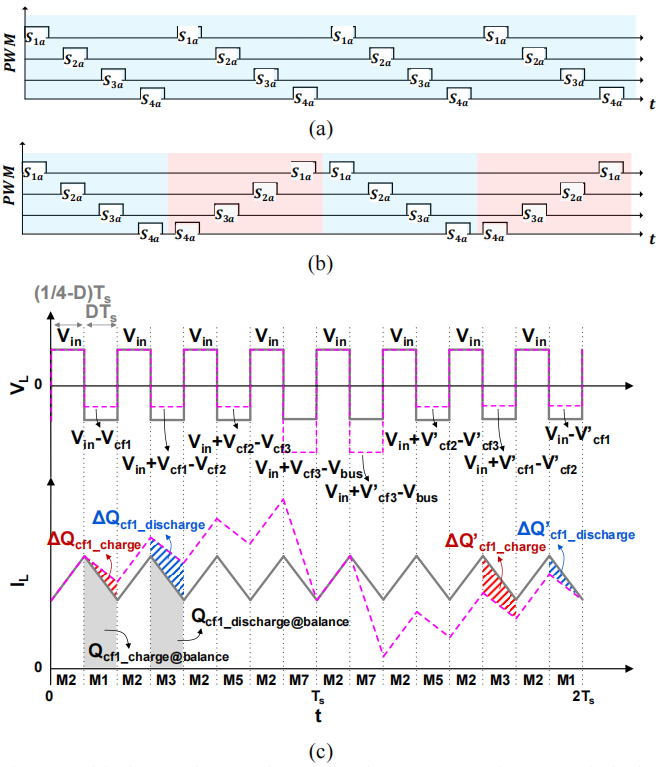


Fig. 8 Critical waveforms of traditional PSPWM and proposed dual sequence PSPWM and inductor voltage. (a) Traditional PSPWM of Seq. 12341234. (b) Proposed dual sequence PSPWM of Seq. 12344321. (c) Voltage and current waveforms of inductor with proposed dual sequence PSPWM of Seq. 12344321.

in this paper. The PWM waveforms under this proposed modulation strategy are shown in Fig. 8(b).

From a mathematical perspective, this article analyzes the state space model with the phase shift sequence of $S_{4a} \rightarrow S_{3a} \rightarrow S_{2a} \rightarrow S_{1a}$ (20) which is opposite to the previously analyzed $S_{1a} \rightarrow S_{2a} \rightarrow S_{3a} \rightarrow S_{4a}$ sequence (11):

$$\begin{bmatrix} \dot{v_{Cf1}} \\ \dot{v_{Cf2}} \\ \dot{v_{Cf3}} \end{bmatrix} = k_1 \left(\begin{bmatrix} 0 & 2 & 0 \\ -2 & 0 & 2 \\ 0 & -2 & 0 \end{bmatrix} \begin{bmatrix} \overline{v_{Cf1}} \\ \overline{v_{Cf2}} \\ \overline{v_{Cf3}} \end{bmatrix} + \begin{bmatrix} -1 \\ -1 \\ 1 \end{bmatrix} V_{bus} \right) \tag{20}$$

Whose elements in matrix are all opposite to elements in state space matrix of $S_{1a} \rightarrow S_{2a} \rightarrow S_{3a} \rightarrow S_{4a}$ sequence (11), which means dynamics of all flying capacitor voltage could be cancelled by switching these two dual sequences cycle by cycle.

As shown in Fig. 9(a), the change in flying capacitor voltage during $2T_s$ under traditional PSPWM modulation can be calculated as:

$$\begin{cases} v_{Cf1_{fin}} - v_{Cf1_{ini}} = -(\Delta v_{cf1} + \Delta v'_{cf1}) \\ v_{Cf2_{fin}} - v_{Cf2_{ini}} = -(\Delta v_{cf2} + \Delta v'_{cf2}) \\ v_{Cf3_{fin}} - v_{Cf3_{ini}} = (\Delta v_{cf3} + \Delta v'_{cf3}) \end{cases} \tag{21}$$

Both $\Delta v_{cf1,2,3}$ and $\Delta v'_{cf1,2,3}$ can be derived from equation (10). In Fig. 9(b), the change in flying capacitor voltage during $2T_s$ under proposed dual sequence PSPWM modulation can be calculated as:

$$\begin{cases} v_{Cf1_{fin}} - v_{Cf1_{ini}} = -(\Delta v_{cf1} - \Delta v''_{cf1}) \\ v_{Cf2_{fin}} - v_{Cf2_{ini}} = -(\Delta v_{cf2} - \Delta v''_{cf2}) \\ v_{Cf3_{fin}} - v_{Cf3_{ini}} = \Delta v_{cf3} - \Delta v''_{cf3} \end{cases} \quad (22)$$

Since no abrupt change occurs in the circuit over $2T_s$, $\Delta v_{cf1} \approx \Delta v'_{cf1} \approx \Delta v''_{cf1}$, $\Delta v_{cf2} \approx \Delta v'_{cf2} \approx \Delta v''_{cf2}$ and $\Delta v_{cf3} \approx \Delta v'_{cf3} \approx \Delta v''_{cf3}$. Thus, the voltage variation over the time scale of $2T_s$ under traditional PSPWM modulation can be regarded as twice that of a single T_s. While under proposed dual sequence PSPWM, the voltage variation over the time scale of $2T_s$ is the respective difference between Δv_{cf1} and $\Delta v''_{cf1}$, Δv_{cf2} and $\Delta v''_{cf2}$, Δv_{cf3} and $\Delta v''_{cf3}$.

Based on the above discussion, if the bus voltage drops below the safe operating threshold for a 5L FCML TPPFC during an AC voltage drop transient, the proposed dual sequence PSPWM modulation strategy can be applied to further cancel the ringing in the flying capacitor voltages. Therefore, it is appropriate to activate this strategy only during the recovery stage of the FCML PFC for a short duration. Whether to activate dual sequence PSPWM can be determined by evaluating whether the initial bus voltage falls below the aforementioned safe operating threshold v_{SOT}. The corresponding logic diagram for activation is presented in Fig. 10. Fig. 11 presents a case that demonstrates the application of dual sequence PSPWM for 5ms, and the maximum voltage across the switching devices was reduced from 155V to 110V. It can be seen that high frequency ringing of flying capacitor voltage is cancelled. However, a slow voltage variation in the flying capacitor voltages is still observed. Nevertheless, the slow variation in the flying capacitor voltages is negligible as shown in Fig. 11. This residual deviation arises because the flying capacitor voltages have already changed by the end of the first switching cycle in Fig. 9(b). Consequently, the inductor voltage waveform in the second switching cycle cannot be perfectly symmetrical to that in the first cycle, and the charging and discharging variations over the two cycles do not completely cancel as shown in Fig.8(c)($Q_{cfx_charge} - Q_{cfx_discharge} \neq Q'_{cfx_discharge} - Q'_{cfx_charge}$). However, this residual charge imbalance is much smaller than the total two cycle charge deviation produced by traditional PSPWM, as illustrated in Fig. 9($|\Delta v_{cfx} + \Delta v'_{cfx}| \gg |\Delta v_{cfx} - \Delta v''_{cfx}|$). Therefore, the small flying capacitor voltage variation caused by the imperfect cycle-to-cycle symmetry can be safely neglected.

IV. Experimental Verification

We performed the AC Drop test on a 6L FCML TPPFC converter which is configured for 5L FCML as shown in Fig. 12(a). The experiment waveforms of v_{sw}, v_{in}, i_L at AC Drop is shown in Fig. 12(b), and the AC Drop occurs when v_{in} at 90° for 20ms. Fig. 12(c) presents the shows the measured efficiency curves. The key parameters of the prototype is shown in Table I.

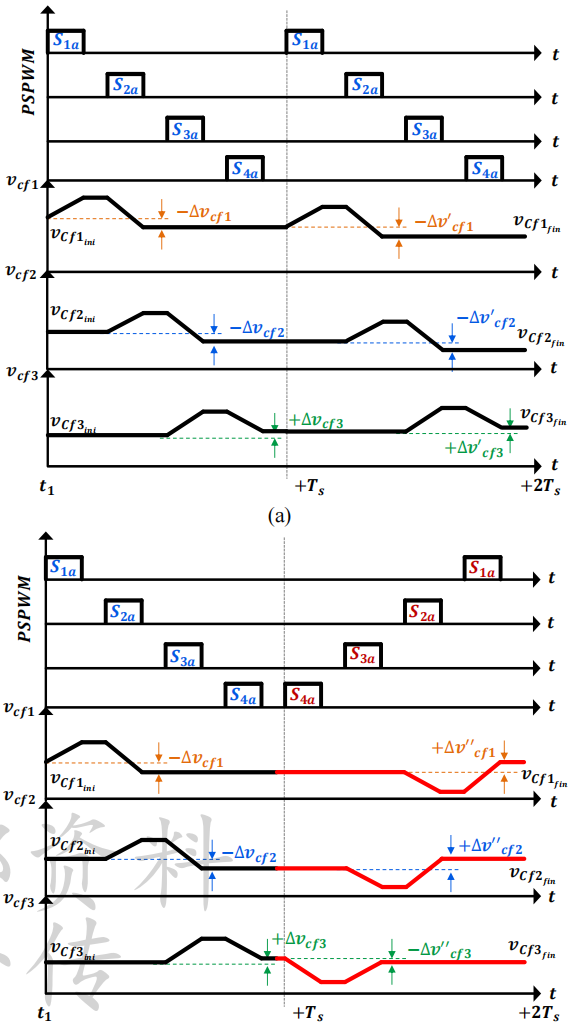


Fig. 9 Comparison of critical waveforms between traditional PSPWM and proposed dual sequence PSPWM. (a) Traditional PSPWM of Seq. 12341234. (b) Proposed dual sequence PSPWM of Seq. 12344321.

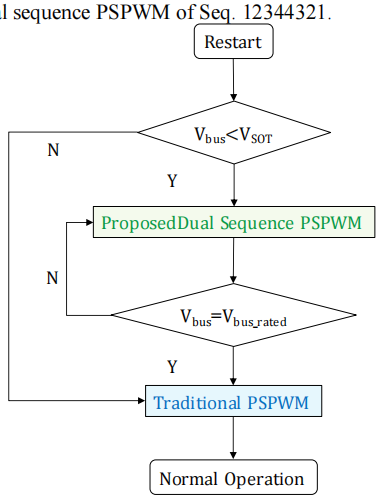


Fig. 10 Flow diagram of activating dual sequence PSPWM

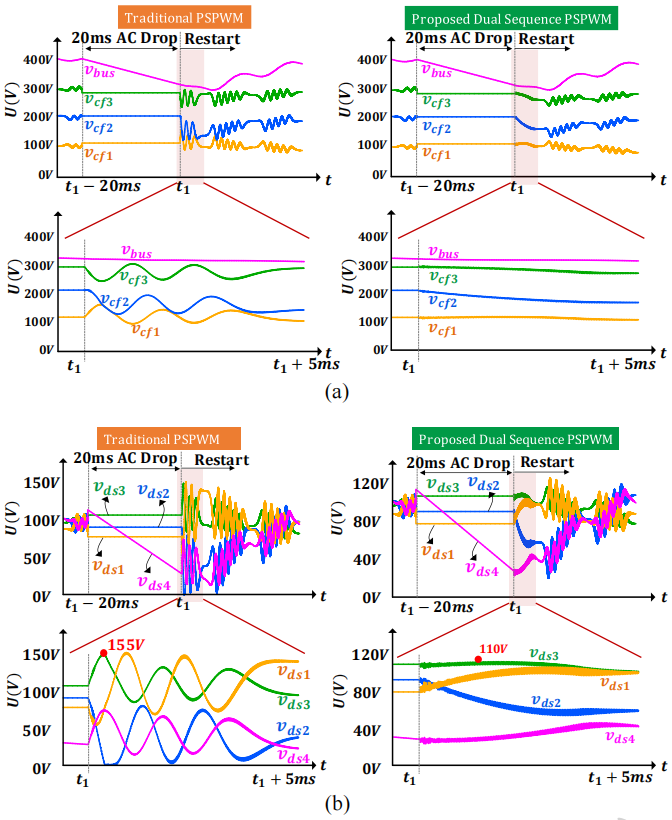


Fig. 11 Simulation validation of ringing suppress under propoesd dual sequence PSPWM(Seq.12344321) during recovery stage after 20ms AC Drop@90°. (a) Critical waveforms under PSPWM(Seq.12341234). (b) Critical waveforms under dual sequence PSPWM(Seq.12341234) continue 5ms.

Fig. 13 presents the flying capacitor voltage waveforms and the voltage stress waveforms of the devices under a 600W operating condition, with 110V AC Drop@90 ° durations of 10 ms and 20 ms, respectively. Fig. 13(a) shows that under a 10 ms AC drop, the bus voltage drops from 400V to approximately 360V. As indicated by Equation (15), the ringing amplitude of the flying capacitor voltage is small under this condition, as shown in the left plot of Fig. 13(a), and the fluctuation of the device voltage stress is also small, as shown in Fig. 13(b). When the AC drop duration is extended to 20 ms, the bus voltage drops to approximately 320V, as illustrated in the left plot of Fig. 13(b). Under this condition, a significant oscillation is observed in the flying capacitor voltages, and the maximum device voltage stress exceeds 150V, which poses an overvoltage threat to the devices. As the power is increased to 800 W, after 20ms 110V AC Drop@90 ° and the converter resumed operation, the flying capacitor voltages started from a more unbalanced initial state as presented in Fig. 14. The v_{bus} drops from 400V drop to 310V while the voltage across flying capacitors remain unchanged compared to their steady state. Consequently, dynamic voltage ringing occurred as analyzed in Section II, and this ringing continues about 5ms.

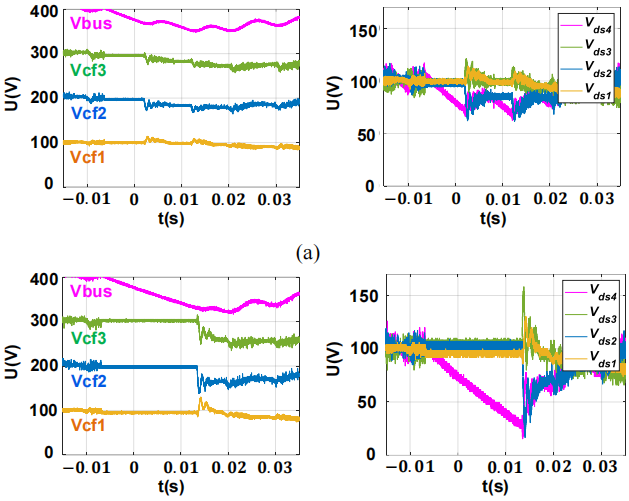
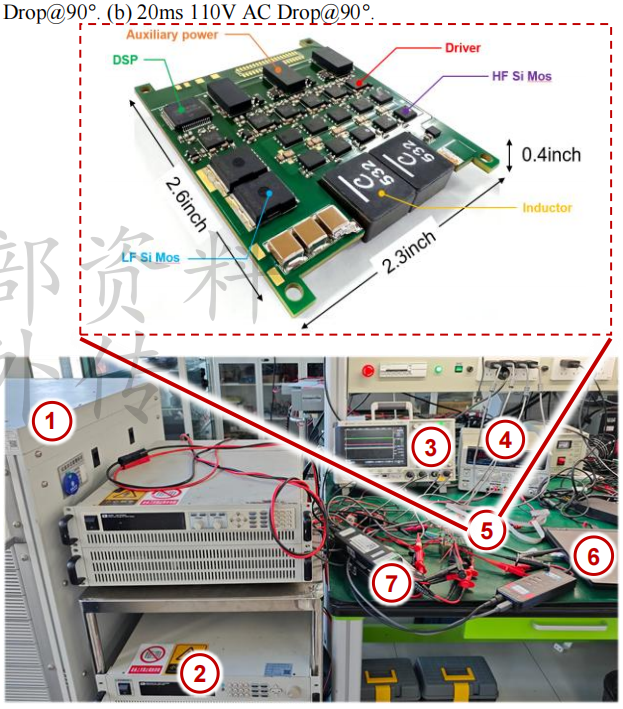
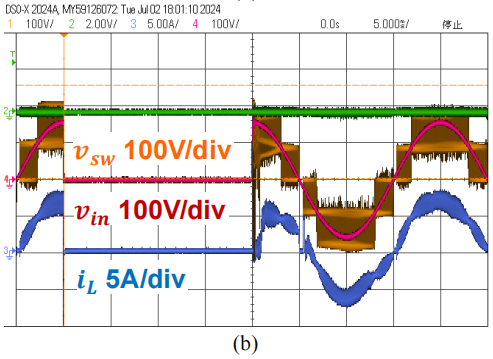


Fig. 13 600W experimental waveforms of voltages across flying capacitors and devices under traditional PSPWM (a) 10ms 110V AC Drop@90°. (b) 20ms 110V AC Drop@90°.





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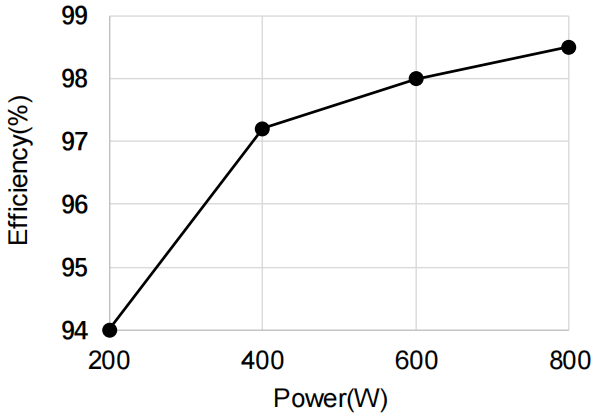

(c)

Fig. 12 Prototype and test waveforms during AC Drop. (a) Hardware and experimental setup. ① Chroma 61511 AC source. ② ITECH IT8902E-600-140 DC electronic load. ③ KEYSIGHT DSOX2024A. ④ GWINSTEK Auxiliary power supply. ⑤ Prototype. ⑥Host computer. ⑦ Differential probe CYBERTEK DP6150B (b) Voltage and inductor current waveforms during AC Drop. (c) Without the driver and controller loss @220Vac and 400Vdc.

TABLE I

KEY PARAMETERS OF THE PROTOTYPE

Description	Parameters	Description	Parameters
HF Devices	BSC093N15NS5	v_{in}	110/220V_{ac}
LF Devices	IPT60R028G7	v_{bus}	400V_{dc}
Inductors	XAL1510-153	P_{load}	600/800W
FCs	C5750X6S2W225K250KA	C_{bus}	450uF
Driver	2EDF7275B	f_s	60kHz

For the 5L FCML TPPFC converter with a 400V DC bus voltage, the voltage stress across the switching devices during steady state operation is 100V. Therefore, we selected devices with a 150V voltage rating. However, under traditional PSPWM (Seq.12341234), when the converter resumes operation, the voltage ringing reached 170V as shown in Fig. 14(b), exceeding the withstand voltage of the switching devices. By adopting proposed dual sequence PSPWM (Seq.12344321), the voltage ringing was mitigated, and the maximum voltage across the switching devices was reduced from 170V to 125V as shown in Fig.14(b). In addition, Fig. 14(c) presents the flying capacitor voltage and device voltage stress waveforms during the transition from the proposed dual sequence PSPWM back to traditional PSPWM. At the instant of modulation back, the flying capacitor voltages still remain in an unbalanced initial state. Consequently, a voltage ringing in the flying capacitors is observed once again after the return to traditional PSPWM. However, owing to the preceding dual sequence PSPWM modulation period, the degree of voltage imbalance among the flying capacitors has been substantially reduced. As a result, the amplitude of this second ringing is considerably smaller, and the threat of overvoltage stress imposed on the devices is greatly weakened. The experimental waveforms for the AC Drop events occurring at phase angles of 45° is propoesd in Fig. 15. The maximum voltage across the

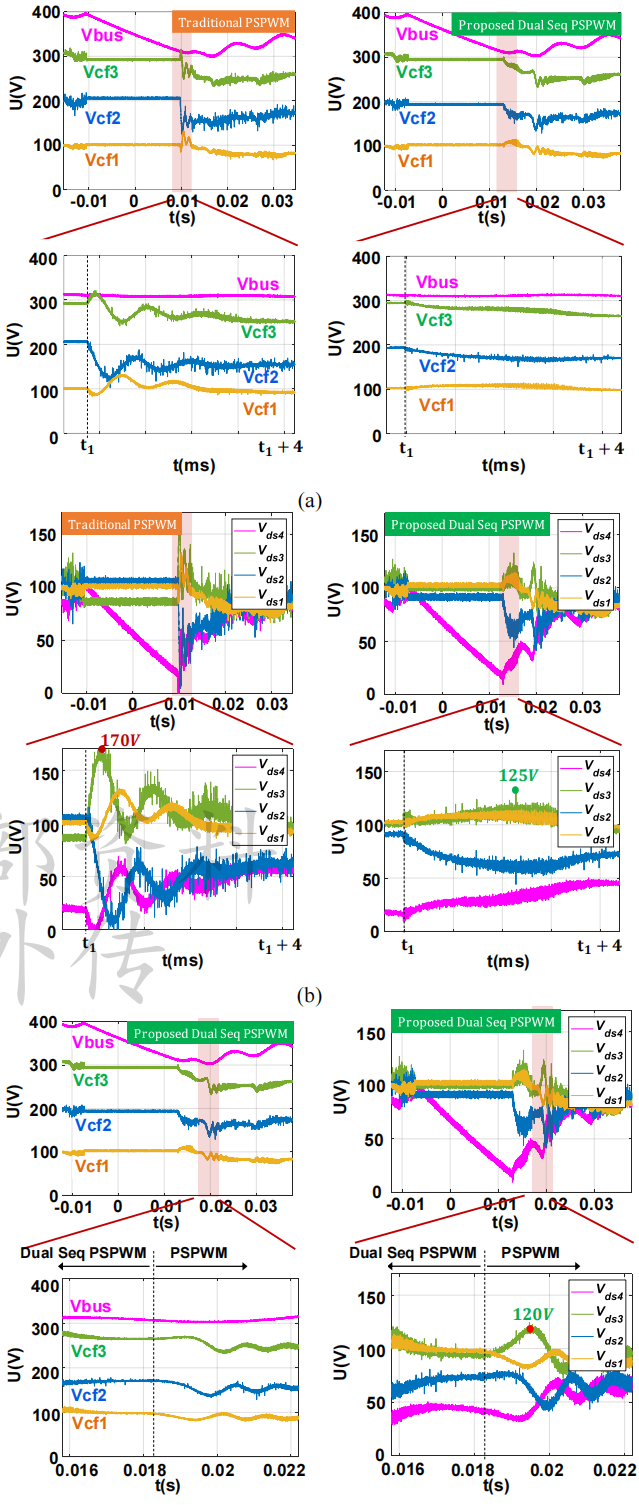

Fig. 14 800W experimental validation of ringing suppress under propoesd dual sequence PSPWM during recovery stage after 20ms 110V AC Drop@90°. (a) Voltage across flying capacitor. (b) Voltage across device. (c) Voltage across flying capacitor and device during the transition from proposed dual Seq PSPWM back to traditional PSPWM.

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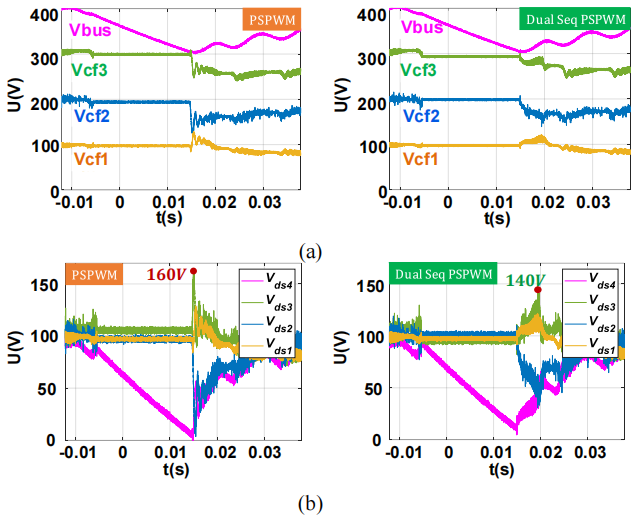

Fig. 15 800W experimental validation of ringing suppress under propoesd dual sequence PSPWM during recovery stage after 20ms 110V AC Drop@45°. (a) Voltage across flying capacitor. (b) Voltage across device.

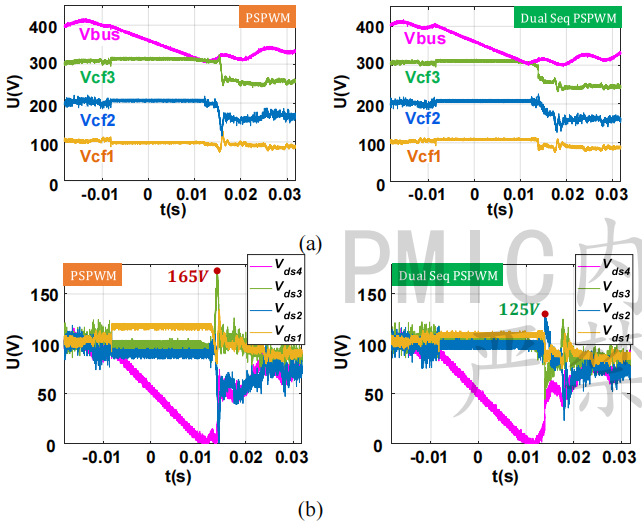

Fig. 16 800W experimental validation of ringing suppress under propoesd dual sequence PSPWM during recovery stage after 20ms 220V AC Drop@90°. (a) Voltage across flying capacitor. (b) Voltage across device.

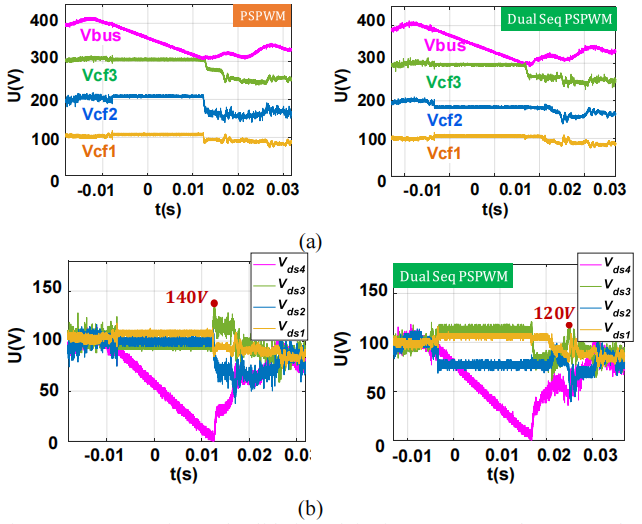

Fig. 17 800W experimental validation of ringing suppress under propoesd dual sequence PSPWM during recovery stage after 20ms 220V AC Drop@45°. (a) Voltage across flying capacitor. (b) Voltage across device.

switching devices was reduced from 160V to 140V. This maximum voltage of 140V because v_{cf3} exhibits an upward deviation, while v_{cf2} continues to decrease. These opposing voltage variations amplify the voltage stress across the switching transistors clamped by these two capacitors. Nevertheless, due to the elimination of high frequency ringings, the overall voltage stress is still reduced.

Furthermore, when the converter resumed operation after 20ms 220V AC Drop@90° and 45°, Fig. 16 and Fig. 17 show the voltage ringing across flying capacitors. It should be noted that the proposed dual sequence PSPWM modulation strategy is only employed during the converter restart stage and requires no additional hardware. Therefore, it does not compromise the steady state operational efficiency or the overall power density of the system.

V. Conclusion

This article elucidates the mechanism underlying voltage ringings in flying capacitors when the converter starts from an unbalanced initial voltage state. A mathematical model of the ringing process is developed, enabling prediction of the ringing magnitude. Furthermore, the article explains the influence of different PSPWM phase shift modulation sequences on the direction of voltage ringing and leverages this characteristic to suppress the ringing. A dual sequence PSPWM method is proposed, which effectively mitigates the resulting voltage ringing across the switching devices. Under traditional PSPWM, this voltage ringing risks overvoltage damage to the switching devices. In contrast, the proposed control method ensures device safety without compromising efficiency or power density. In addition, a limitation of this dual sequence method is that it doubles the flying capacitor voltage ripple compared with traditional PSPWM, which in turn doubles the impact of the voltage ripple on the device voltage stress. Consequently, the flying capacitors must be sized sufficiently large during the steady state design to accommodate this increased ripple.

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